High rate fast timing RPC

-A high rate RPC (> 1 kHz/cm^2) has been developed both with Bakelite and low resistivity glass as electrode.

-Excellent timing FEE (PETIROC) is developed and being upgraded

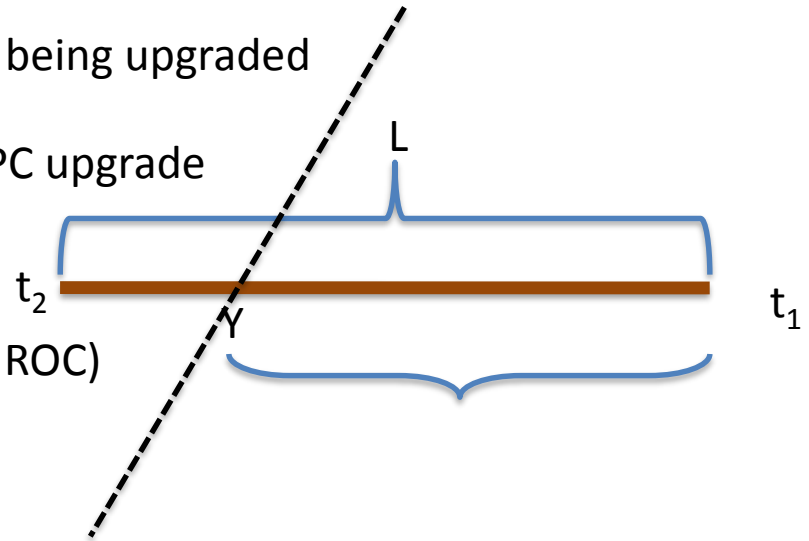The following scheme is proposed for the CMS RPC upgrade

Principle:
To use the 2D readout with good timing FEE (PETIROC)
Motivation
1) Better Y determination

$Y= L/2-v*(t_2-t_1)/2 \rightarrow \sigma(Y) = v* \sigma(T_2-T_1)/2$

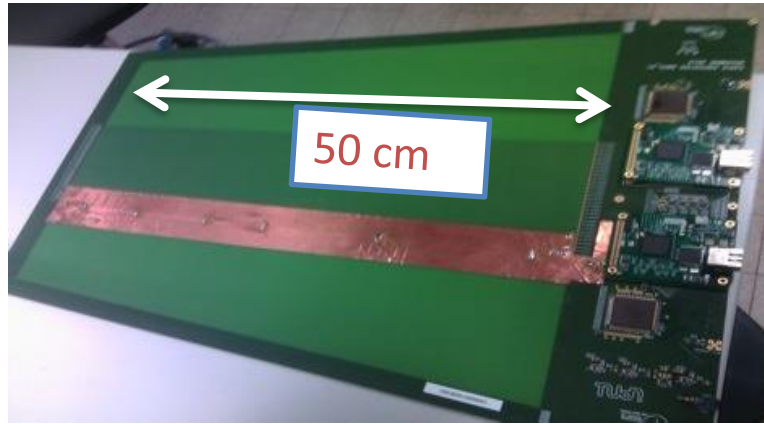2) Less channels (2/eta rather than 5)
3) In addition, with 2-gap RP*C of 1.4 mm gas gap 1 ns absolute
     time resolution could be achieved $\rightarrow$ noise reduction and
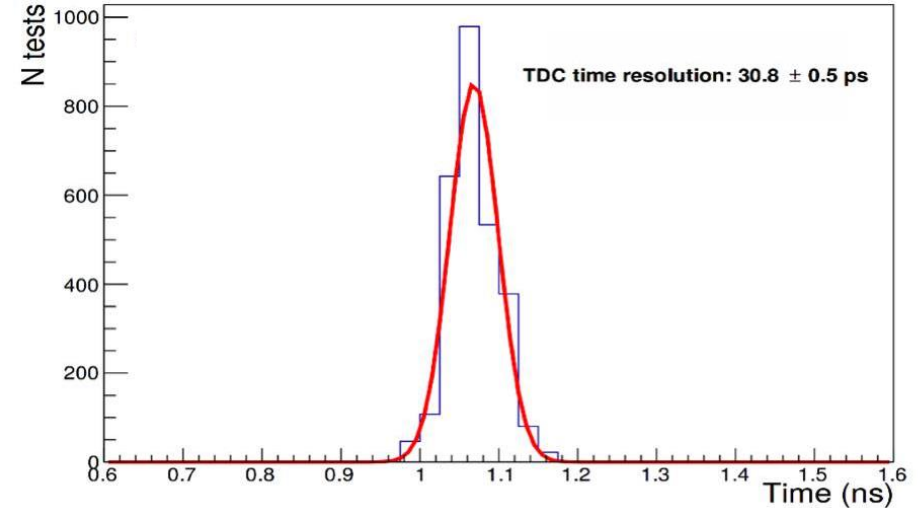   better Muon and HSCP trigger performance
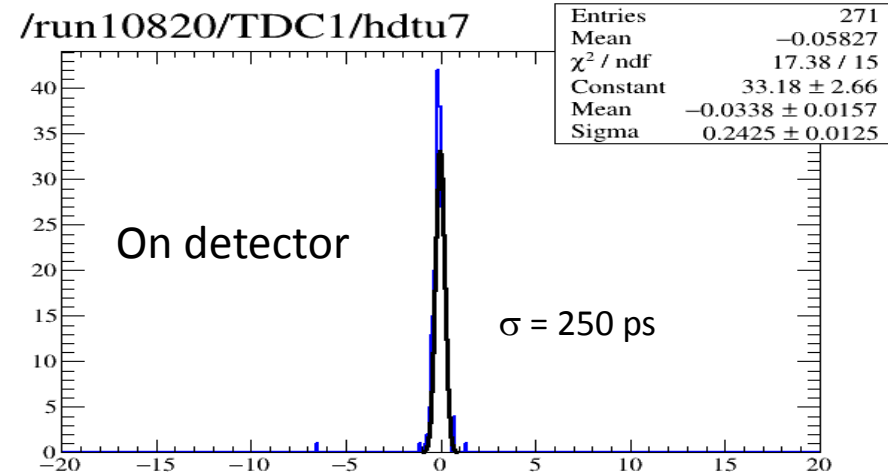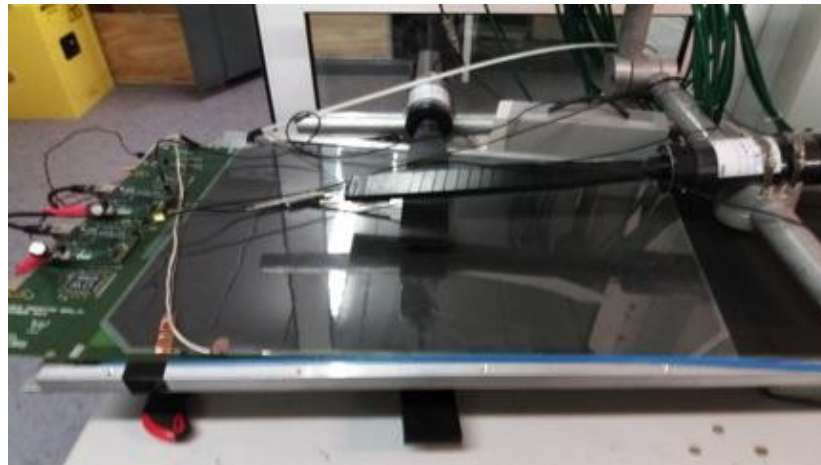
L

t_2

t_1

Y

CMS RPC Electronics

First demonstrator : 32 on-detector strips with 3.5 mm pitch
and 32 off-detector return strips 1 mm pitch
→64 channels = 2 PETIROC + 2 TDC (Delay Line TDC on FPGA
→, 10 ps of LSB)

50 cm

By charge injection on the strips

TDC time resolution: 30.8 ± 0.5 ps

Using cosmic rays

➔

/run10820/TDC1/hdtu7

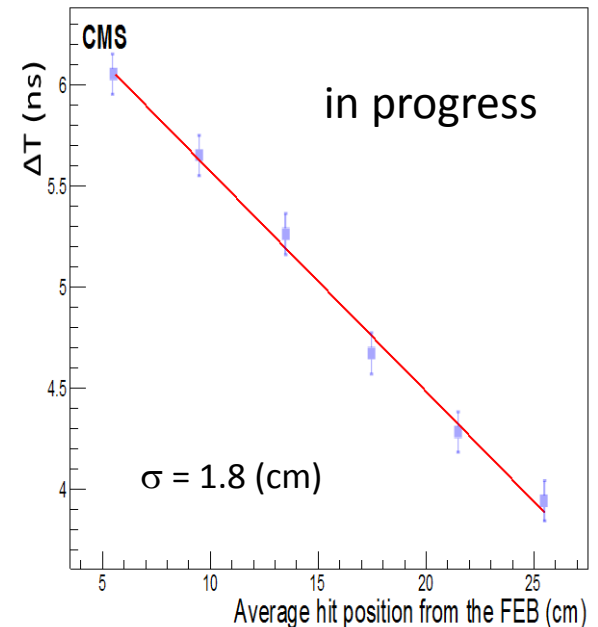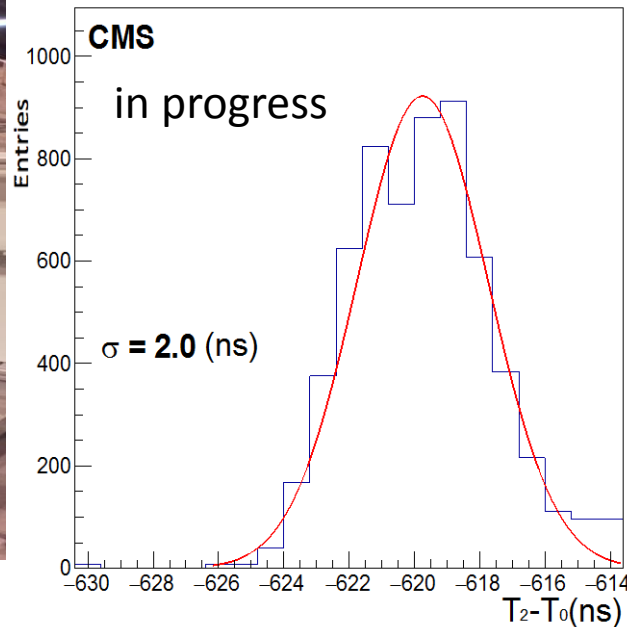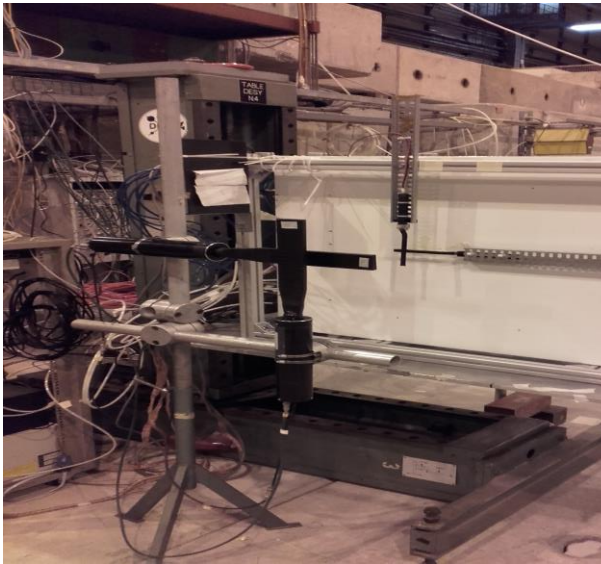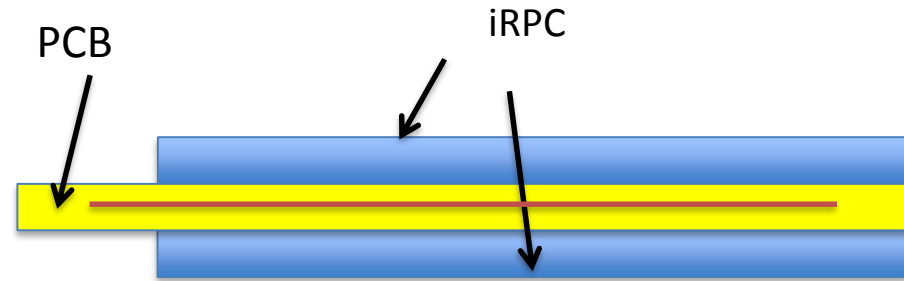| Entries	271
Mean	−0.05827
χ^2 / ndf	17.38 / 15
Constant	33.18 ± 2.66
Mean	−0.0338 ± 0.0157
Sigma	0.2425 ± 0.0125

On detector

σ = 250 ps

- Only one detector
- Scintillator resolution correction not included
-Cluster size correction improvement not included

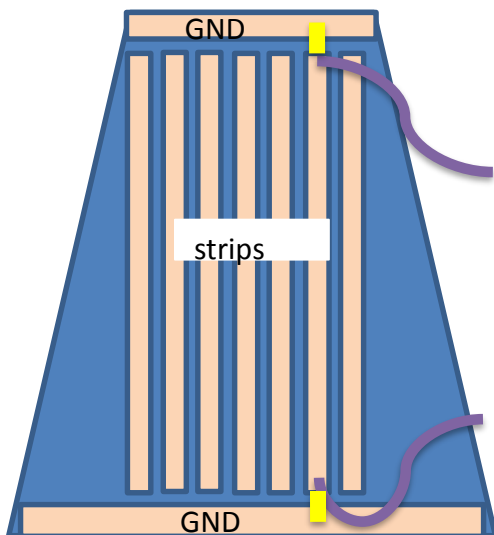The readout electronics was then tested on iRPC detectors in TB:

-2 iRPC chambers :1.4/1.4mm and 1.6/1.6 mm
-Scan studies were performed using moving
tables (< 1mm resolution)

-A DAQ system using external trigger built with
tiny scintillators (1cm width) was used

PCB

iRPC

CMS

in progress

σ = 2.0 (ns)

Entries

T_2-T_0(ns)

CMS

in progress

σ = 1.8 (cm)

ΔT (ns)

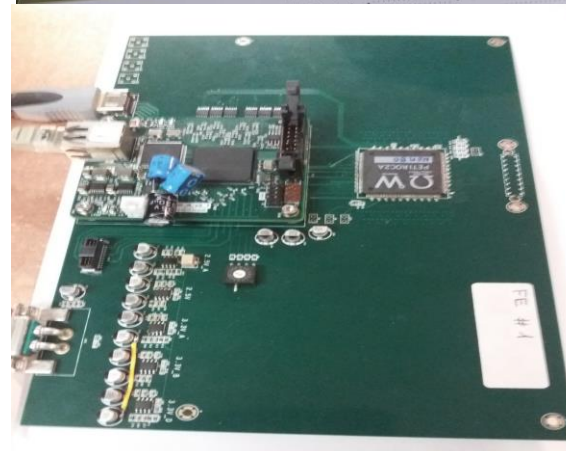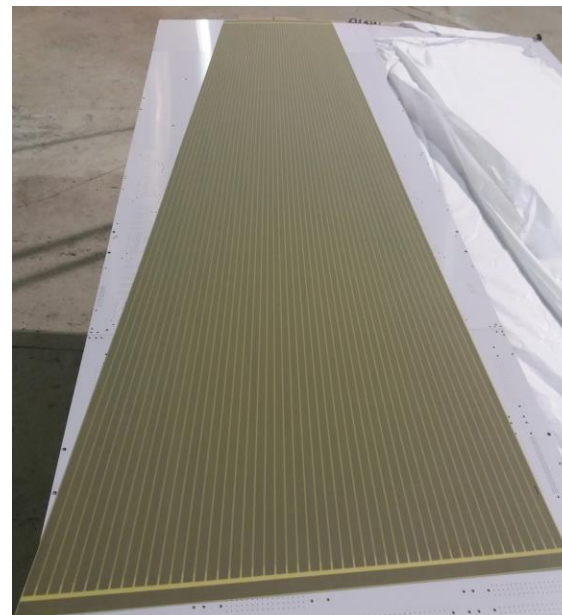Average hit position from the FEB (cm)

To read out RE3/1 and RE4/1 RPC
One sided PCB with strips. Return-strips are replaced with coaxial cables
with the same impedance (company found : ELVIA).

GND

strips

GND

Two large PCB are needed
for the readout of one RPC
chamber

3 petiroc of 64 ch are needed

adapt. board   adapt. board

coax   FE   coax

GND

strip

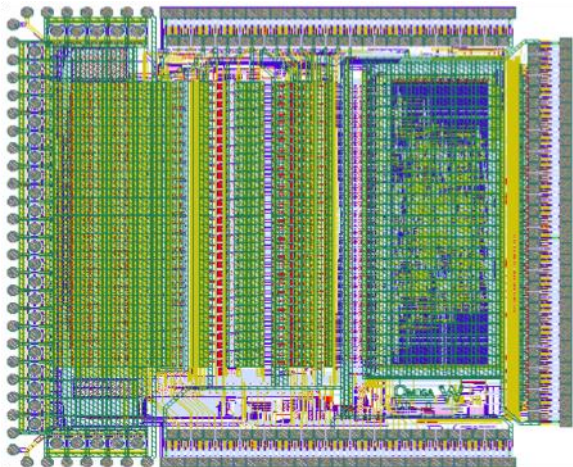This solution is equivalent to the one already tested but simpler and cheaper.
Still, we will produce a large PCB with return strips on the edges to compare the two schemes

Similar development is
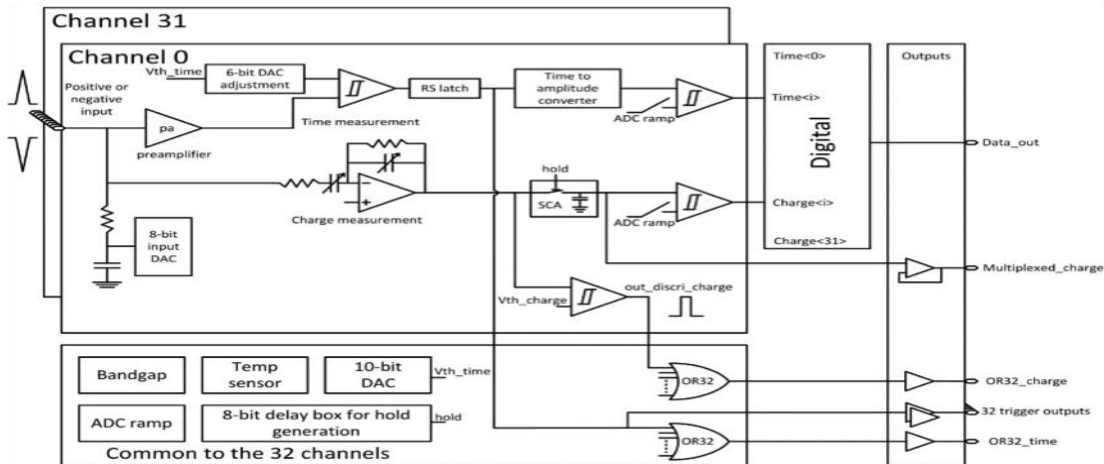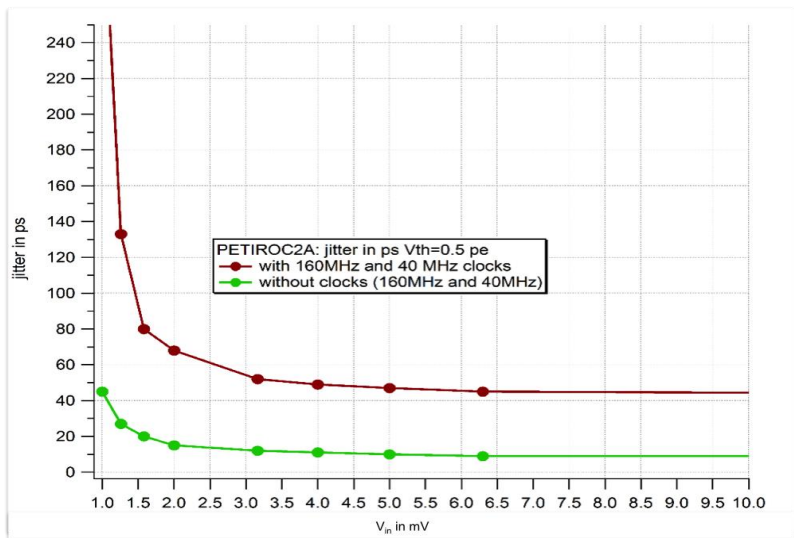followed by GWNU using MRPC

Next steps:
-To validate the readout electronics on large RPC CMS chamber
using a few FB boards

-Assemble the FE boards in one hosting the Petirocs and the TDC
in addition to the Master FPGA to communicate with the DAQ/
Trigger system

- Upgrade the Petiroc from 32 to 64 channels (for compactness,
not a technological challenge) and go for TSMC 130 nm (in
synergy with the HGCAL ROC) for better radiation hardness even
though the expected rate where the FE board is to be fixed is not
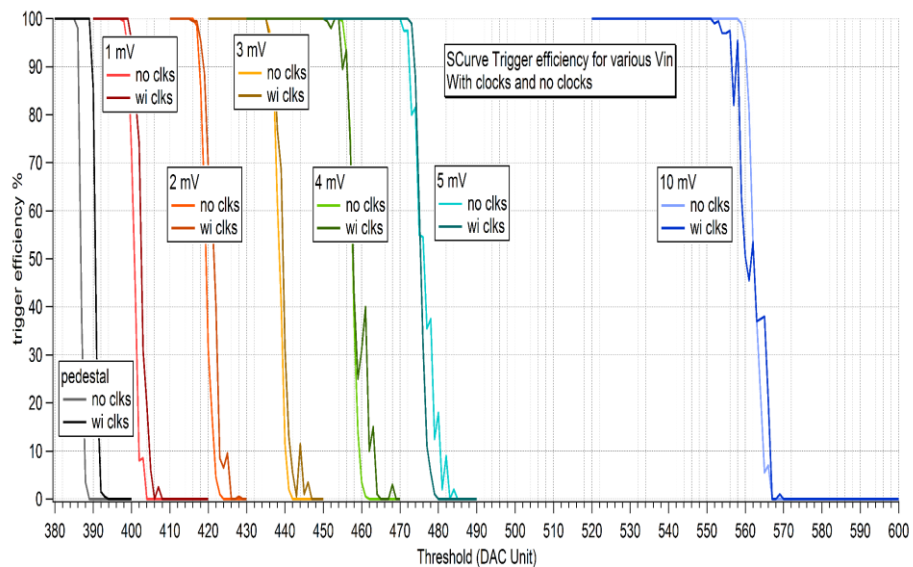high (fluence of a few 10 e12)

PETIROC ASIC, 32ch, SiGe 350 nm technology

Petiroc scheme : only the preamplifier output will be used

Time resolution as a function of the injected charge
1 mV corresponds to about 55 fC

Petiroc S-Curves :
1 DAC unit corresponds to about 3.5 fC

Backup

Alternative

HARDROC2
http://omega.in2p3.fr/

- **64 inputs**

- Current preamp with **8 bits** gain correct: G=0 to 255 (analog G=0 to 2)

- **3 shapers**, variable Rf,Cf and gains:
  - Fsb1, G= ½,**1/4**,1/8,1/16
  - Fsb2, G= 1/8,**1/16**,1/32,1/64

- **3 discriminators**
  - 3 10 bit-DACs to set the thresholds (100fC, 1pC, 10pC)
  - Encoded in 2 bits

- **Auto-trigger down to 10fC up to10pC**

- Store all channels and BCID for every hit in a **127 bit deep digital memory**
  - Data format : 127 (depth)*[2bit*64ch+24bit(BCID)
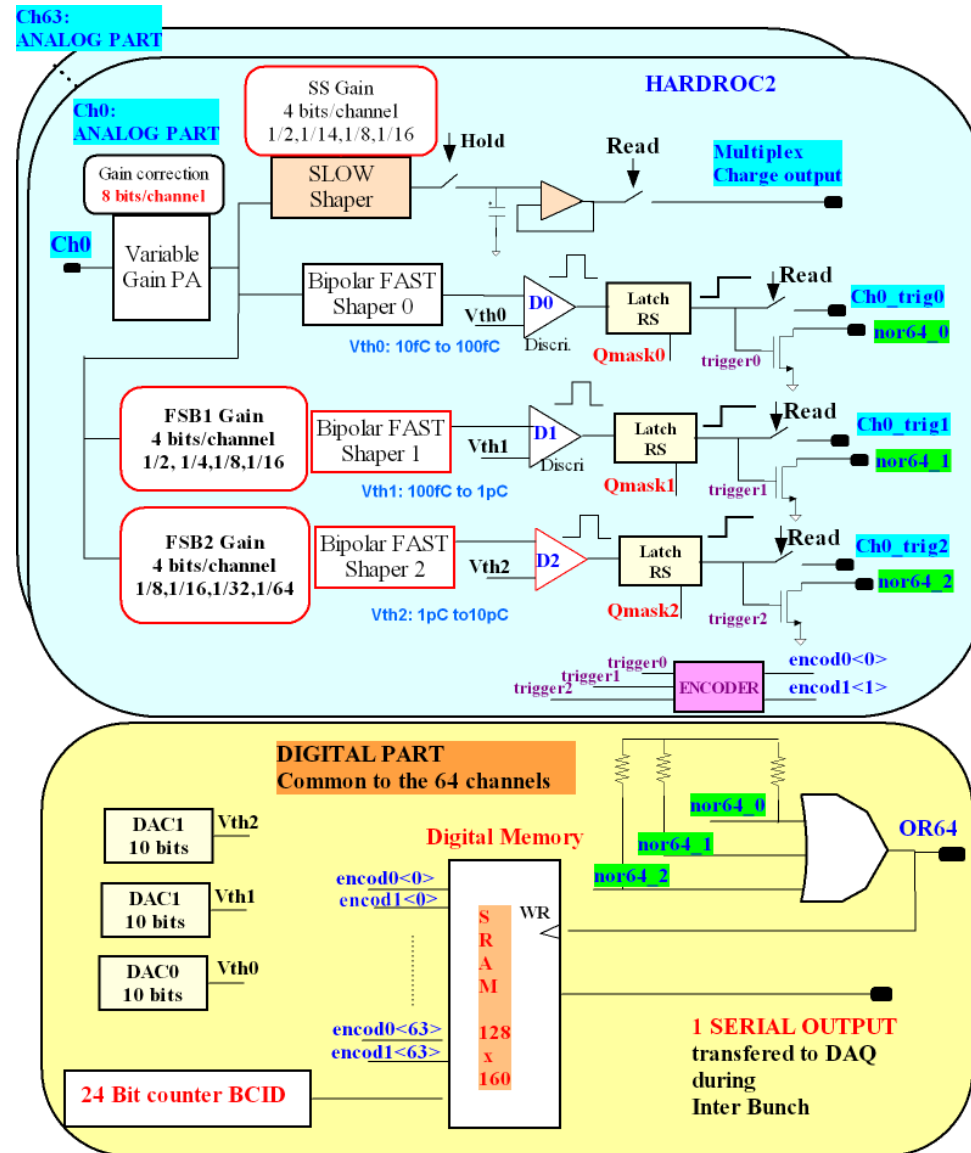 - +8bit(Header)] = 20 320 bits

- **872 SC registers**, default config
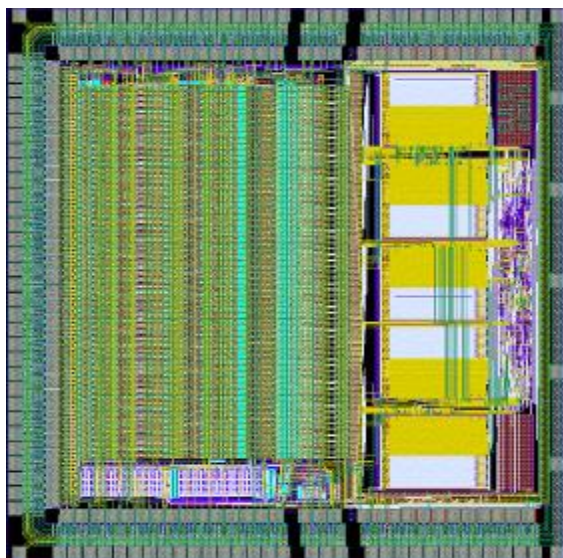 - Mask of bad channels

- **1 mW/ch**

19/10/2017
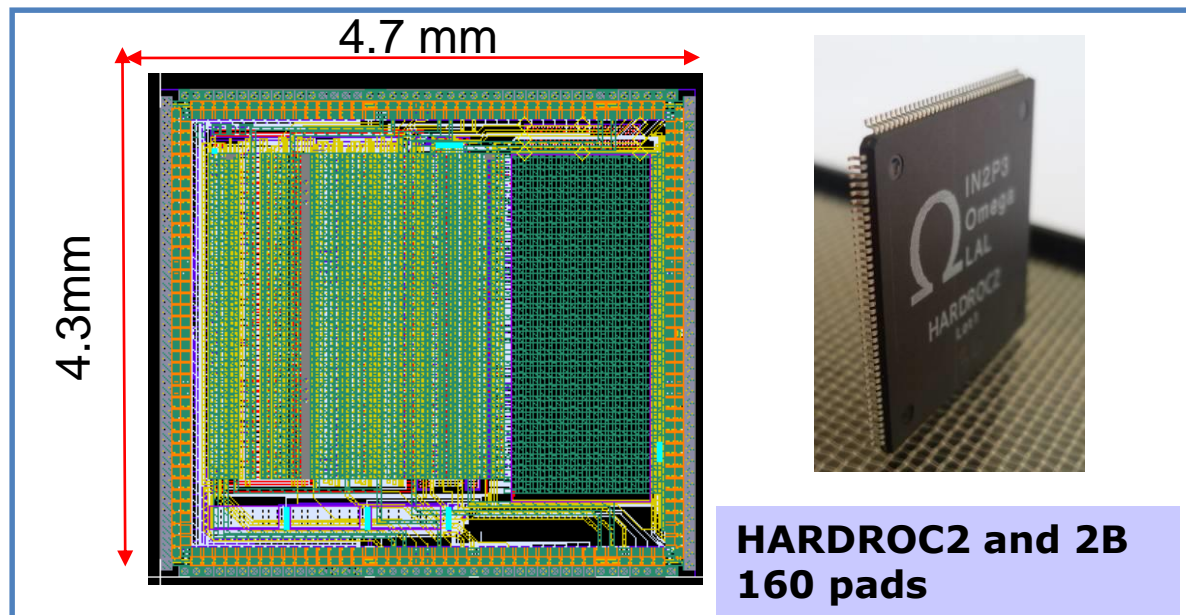
ASIC : HARDROC versions

❑ **AMS 0.35µm SiGe**

❑ **HARDROC1** (Sept 2006):
 - ❑ **1 FSB and 2 discriminators**
 - ❑ **240 staggered pads, QFP240 package 3.4 mm thickness**

❑ **HARDROC2** (June 2008) **and 2B** (June 2009):
 - ❑ **Versions 2 and 2B very similar, 3 FSB, 3 discris**
 - ❑ **160 aligned pads, Thin package TQFP160 = 28 mm x 28 mm x 1.4 mm**
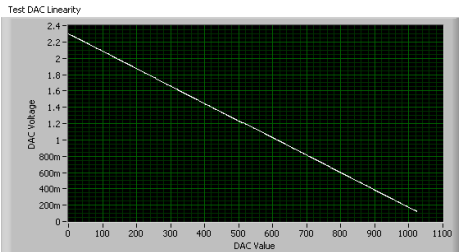

4.7 mm

4.3mm

HARDROC1,
240 staggered pads

**HARDROC2 and 2B
160 pads**
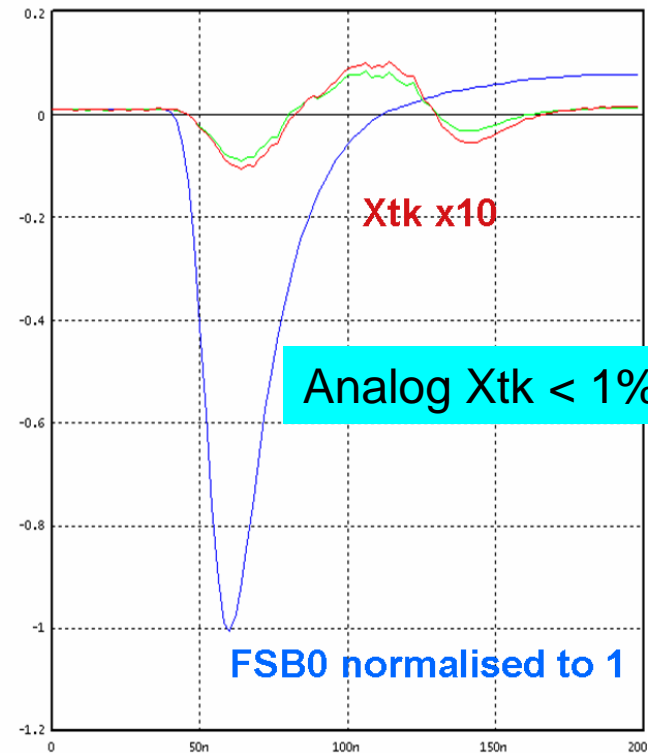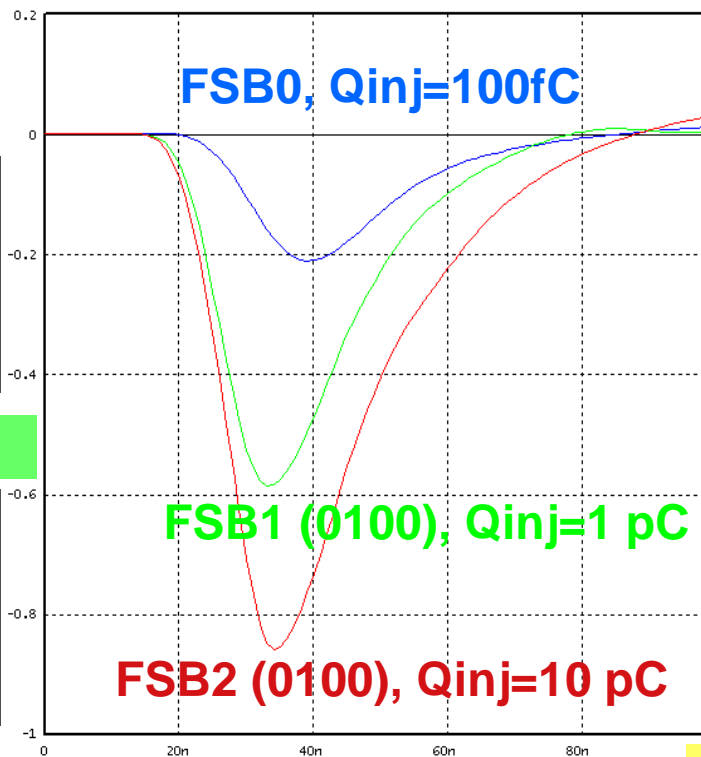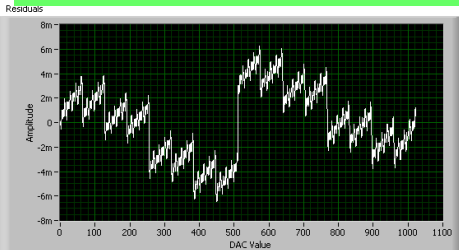
HR2 Trigger path : fast shaper, DAC, Xtk

❑ Fsb0: **Typically 2mV/fC**

❑ 3 integrated DACs to deliver threshold voltages
 ❑ Residuals within ±5 mV / 2.2V dynamic range. INL= 0.2% (2LSB)

❑ **2.1 mV/DAC Unit ie 1 fC/DAC Unit (fsb0)**

2.1mV/DAC Unit

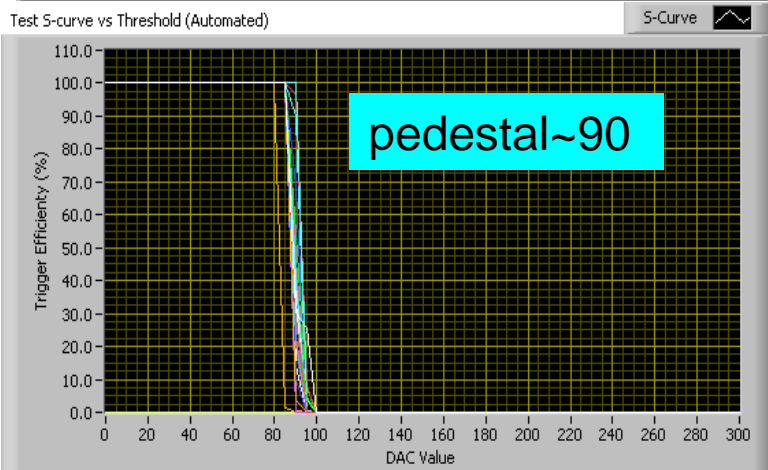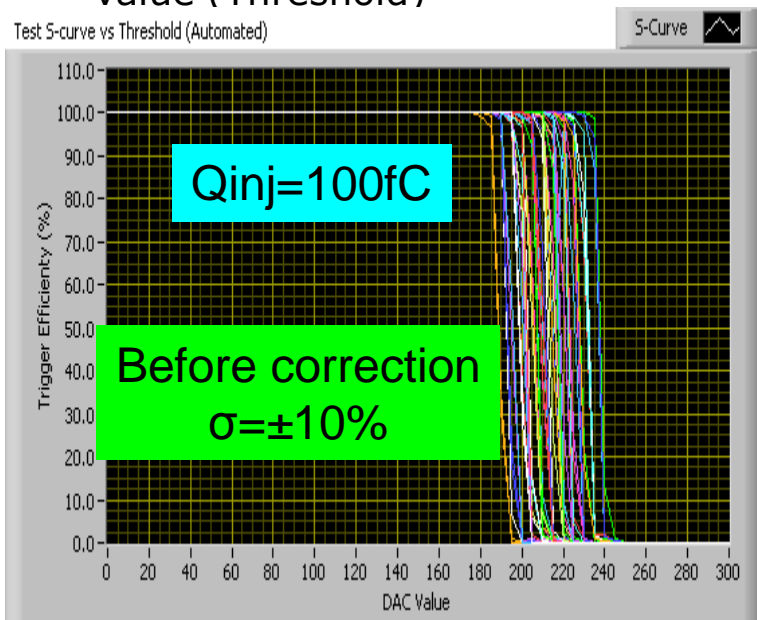Residuals within ±5 mV

FSB0, Qinj=100fC

FSB1 (0100), Qinj=1 pC

FSB2 (0100), Qinj=10 pC

Xtk x10
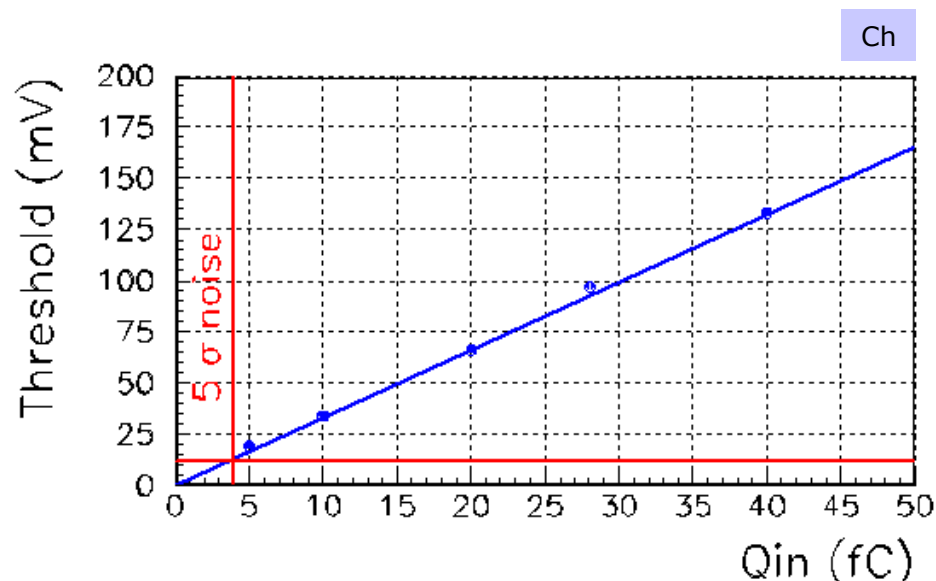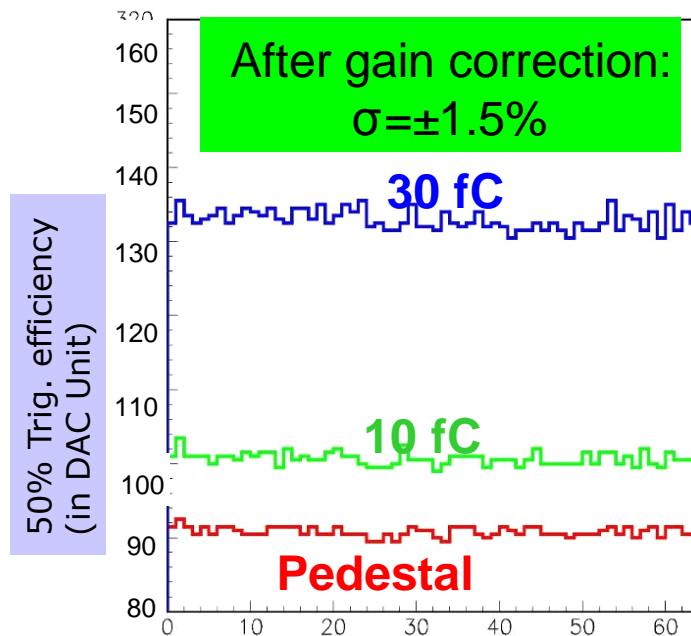
Analog Xtk < 1%

FSB0 normalised to 1

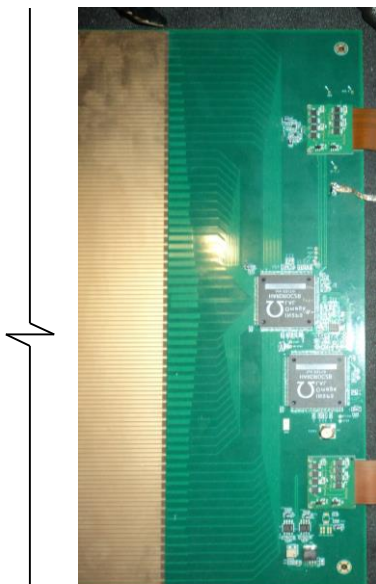**Testboard wo any decoupling cap.**

Trigger efficiency measurements

☐ Scurves performed on FSB0 by varying the DAC value (Threshold)

Test S-curve vs Threshold (Automated)   S-Curve ⌒

Qinj=100fC

Before correction
σ=±10%

Trigger Efficiency (%) — DAC Value

Test S-curve vs Threshold (Automated)   S-Curve ⌒

pedestal~90

Trigger Efficiency (%) — DAC Value

FSB0, 100K, 100fF, G=144

After gain correction:
σ=±1.5%

30 fC

10 fC

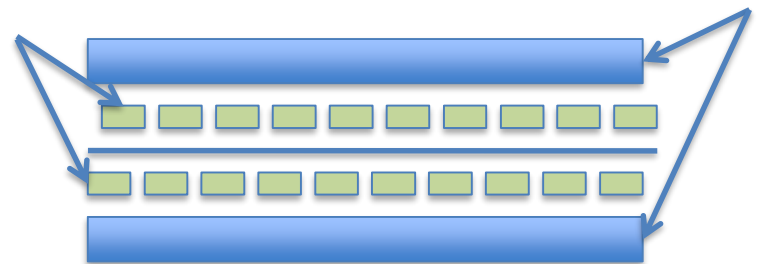**Pedestal**

50% Trig. efficiency (in DAC Unit)

Ch

Threshold (mV)

5 σ noise

Qin (fC)

HR2 was used in pads (SDHCAL prototype with 500000 channels)
and strips PCB configurations on RPC with success

Charge DIF

HR2 (top left strips)
HR2 (bottom left strips)

Strips plane   1 gap

Bakelite 30x30cm strip source off or att=46000