IFAE activities

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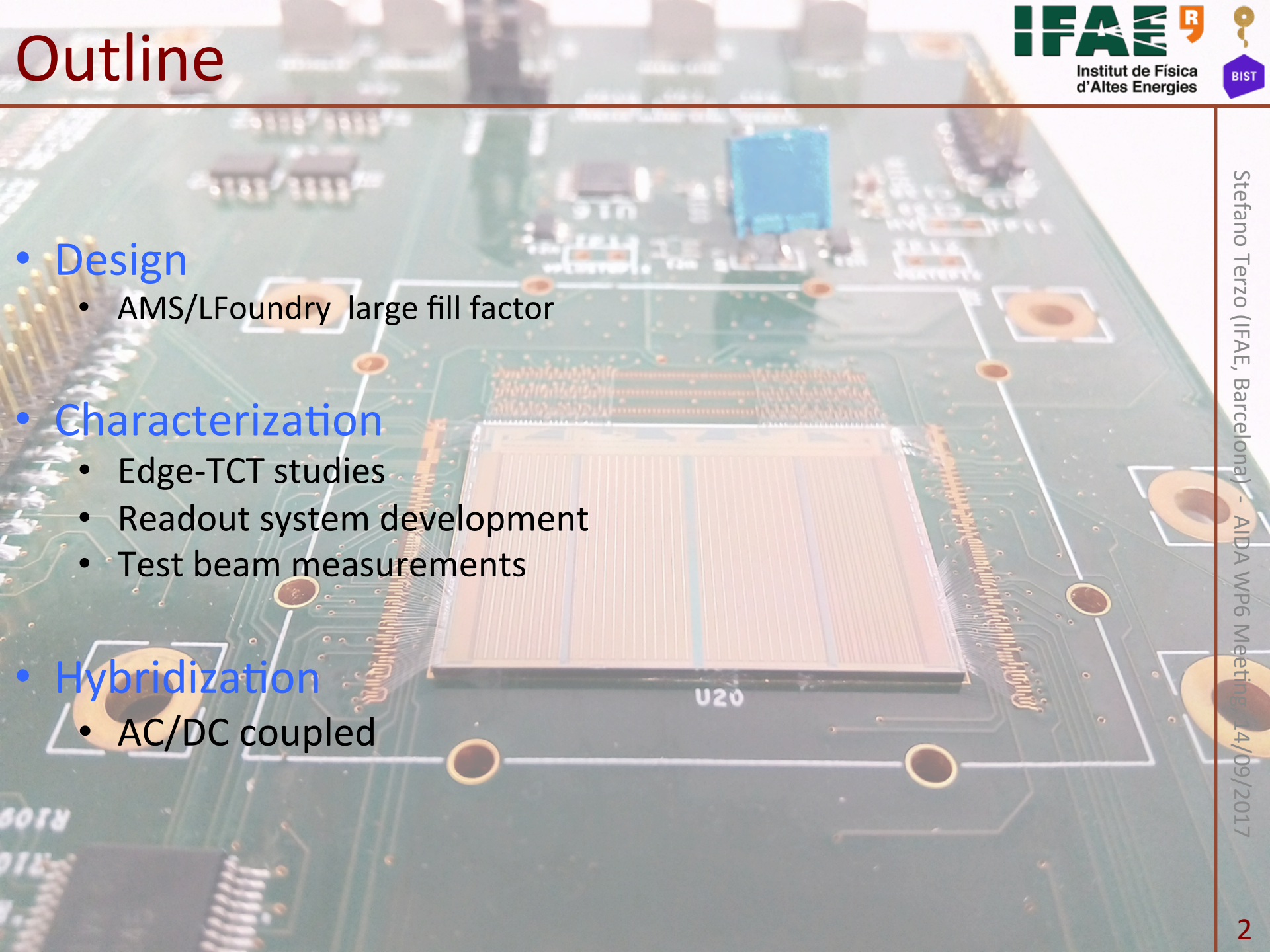
AIDA WP6 meeting
14th September 2017

Outline

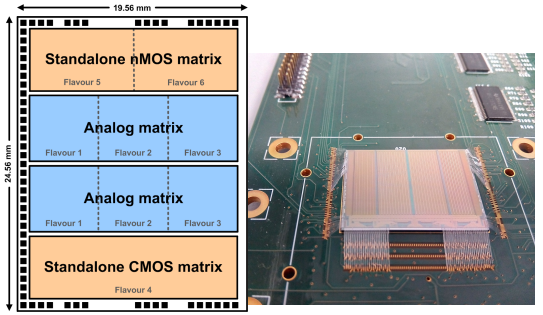
- Design
  - AMS/LFoundry large fill factor
- Characterization
  - Edge-TCT studies
  - Readout system development
  - Test beam measurements
- Hybridization
  - AC/DC coupled



Large fill factor designs

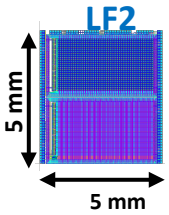
H35Demo

AMS 350 nm
Resistivity: 20-80-200-1k Ω·cm
Design by KIT, IFAE, Uni. Liverpool
Pixel of 50x250 µm², both monolithic and CCPD matrices



LF2

LFoundry 150 nm
Resistivity: 500 Ω·cm and 1.9k Ω·cm
Design by IFAE in collaboration with U.Liverpool
Collaboration of UniGe & KIT
Pixel of 50x50 µm² with analog and digital front-end electronics (isolation layer)

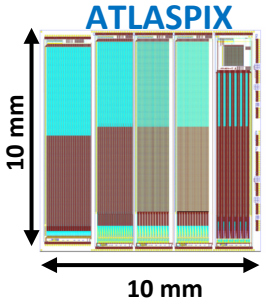


RD50

LFoundry 150 nm
Designed by U.Liverpool, U.Barcelona, IFAE
Main IFAE contribution: matrix with on-pixel TDC for fine time measurements

ATLASPix

Development of future HV-CMOS demonstrator for ATLAS
AMS 180 nm technology, LF 150 nm
Fully monolithic



H35Demo characterization

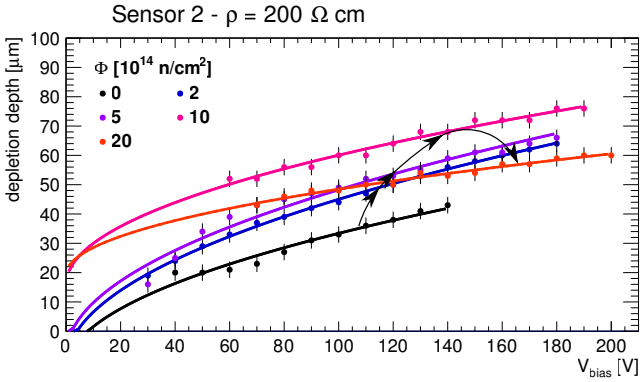
Institut de Física d'Altes Energies

BIST

Edge-TCT

On H35Demo test-structures
Different resistivity: 20-80-200-1k Ω·cm
Before irradiation and after neutron irradiation
Measure of the depletion depth

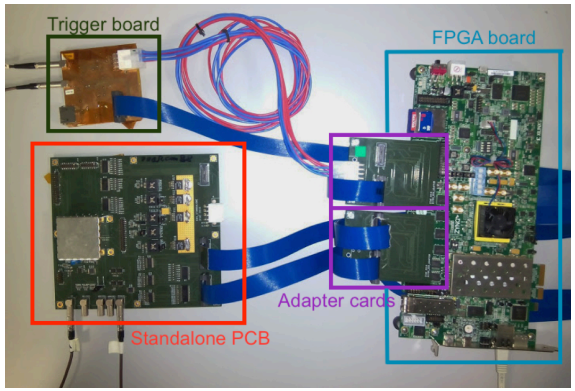
(E.Cavallaro et al., JINST 12 (2017) no.01, C01074)



Readout

For the monolithic matrices of the H35Demo
Based on commercial FPGA Xilinx board
PCBs, firmware & software development at IFAE

(S.Terzo et al., JINST 12 (2017) no.06, C06009)



Beam test

Efficiency measurements of the monolithic H35Demo
Using the UniGe FE-I4 Telescope
SpS in November 2016: first time un-irradiated monolithic CMOS matrices

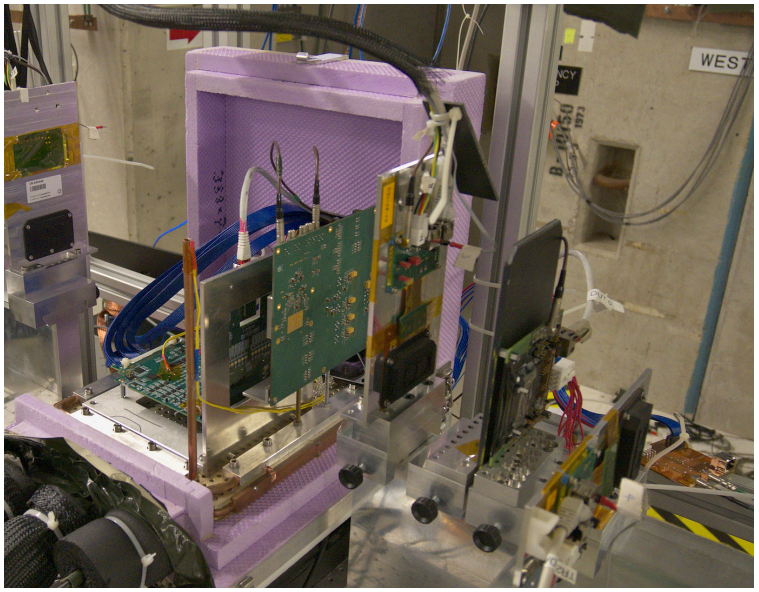
(S.Terzo et al., JINST 12 (2017) no.06, C06009)

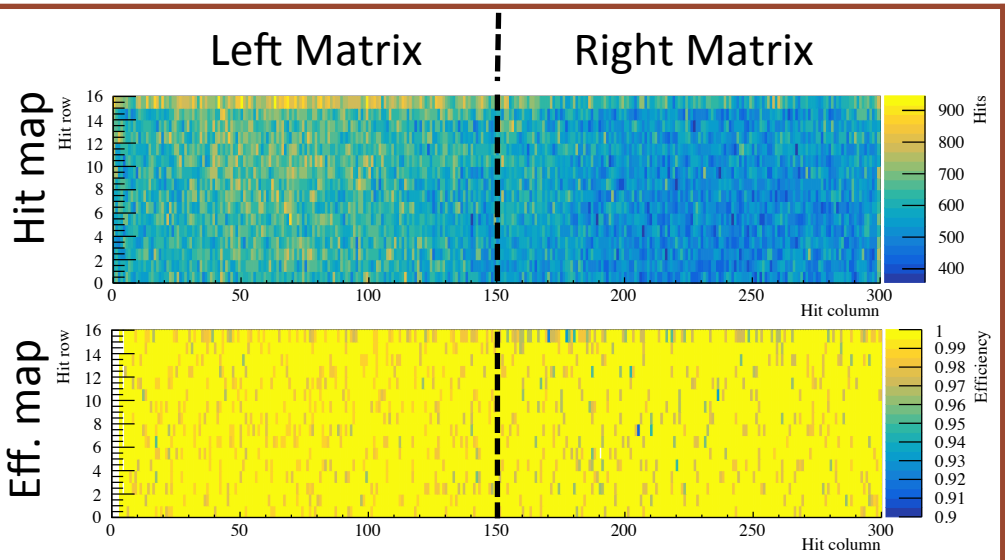
Fermilab in April 2017: Un-irradiated and first time irradiated monolithic CMOS matrices

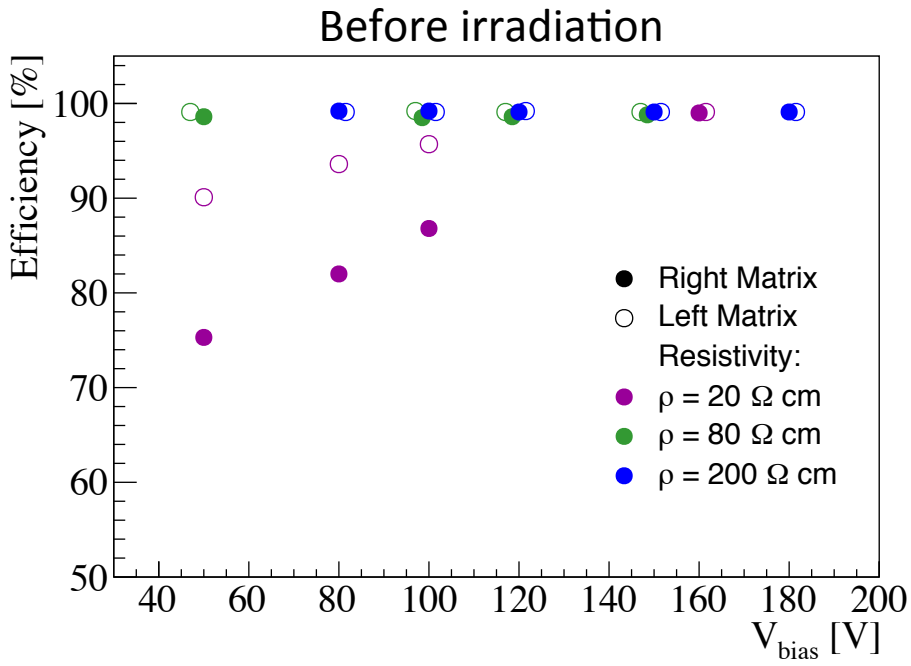
(R.Casanova et al., in proceedings of TWEPP 2017)

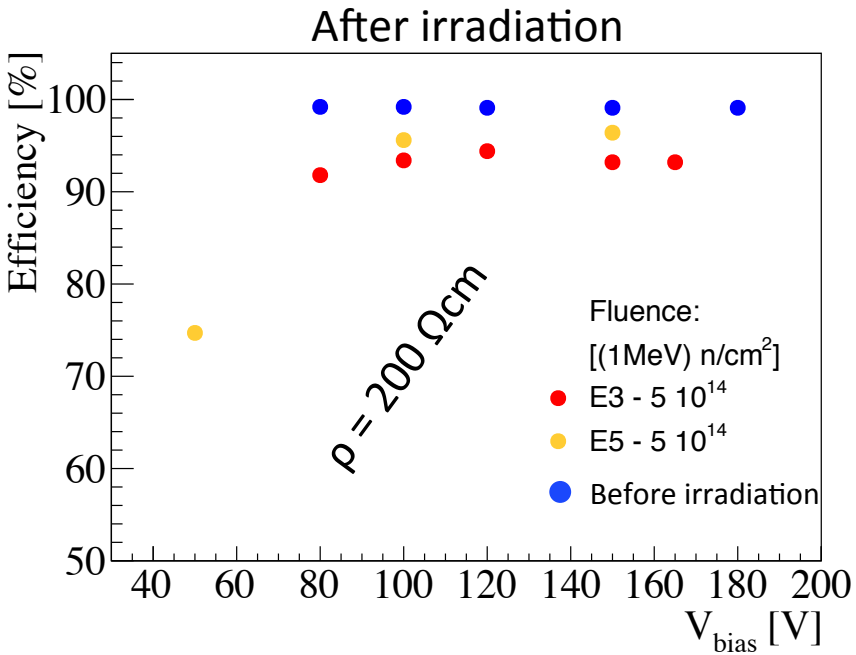
Next beam test at SpS in September 2017: higher irradiations + nMOS matrices

Latest beam test results



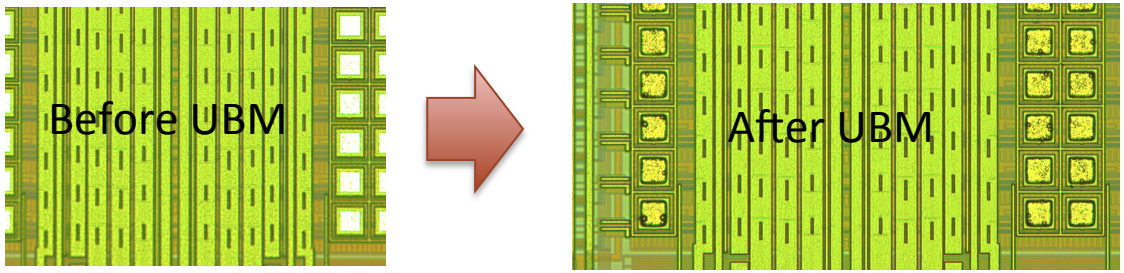


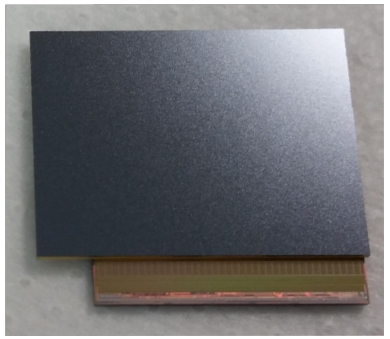


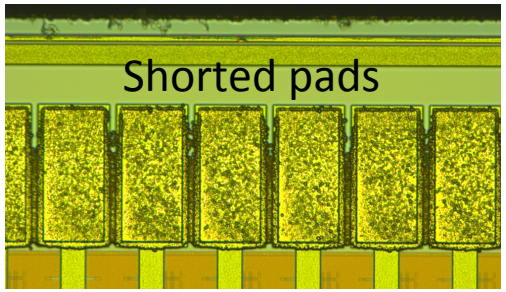


Hybridization

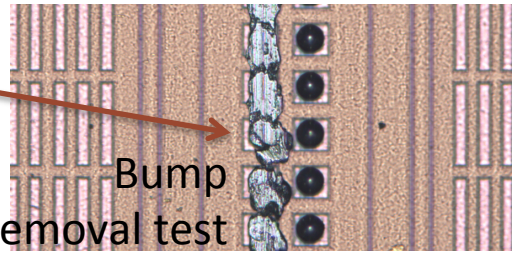
- First bump bonded (DC coupled) H35Demo device was successfully assembled
  - Good Electroless Ni/Au UBM deposition at CNM (4-5um Ni)
  - Flip chipped to SnAg bumped FE-I4B at IFAE
  - Unfortunately chip placed off centered







- Further UBM to produce a second device (centered) failed
  - UBM shorted the wire bond pads (which are very close)
  - Problem solved with kapton protection, next flip-chip soon

- Flip-chipped a V1 LFCPIX to FE-I4 (DC coupled)
  - Device centered to facilitate PCB mounting and wire-bonding
  - Shipped back to Bonn and working well

- Further plans to investigate DC and AC coupled pixels in single device
  - Remove bumps from bumped FEI4B
  - Single bump deposition on FEI4
    - In-house (PacTech SB2 SM bumper)
    - No lithography needed (cost reduction)