Silicon pixel-detector R&D for CLIC

13th “Trento” Workshop on
Advanced Silicon Radiation Detectors

Max-Planck-Institut für Physik, Munich, Germany
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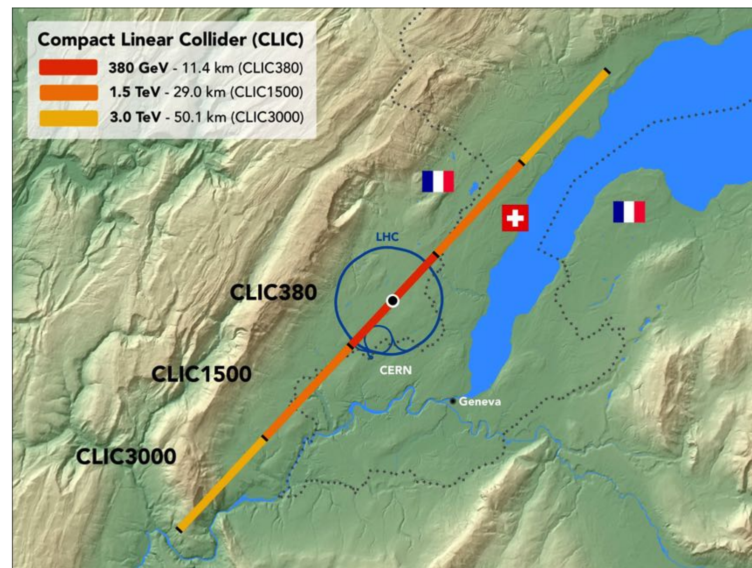
on behalf of the CLICdp Collaboration

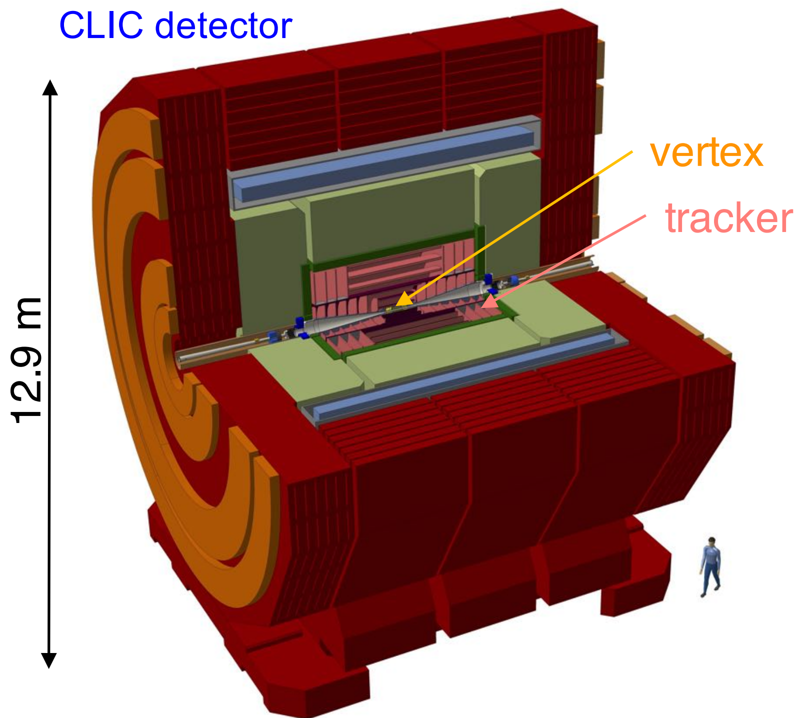
CLIC accelerator and detector

- CLIC (Compact LInear Collider):
  linear e^+e^- collider concept for post HL-LHC phase
- $\sqrt{s}$ from few hundred GeV up to 3 TeV
  (two-beam acceleration with ~100 MV/m)
- Precision and discovery physics at the TeV scale
- Detector and physics studies within the CLICdp collaboration of 30 institutes
- ~10 institutes active in vertex/tracker R&D, collaboration with ATLAS, ALICE, RD53, AIDA 2020

Possible staged CLIC implementation



CLIC detector



CLIC vertex-detector and tracker requirements

Vertex detector:

- efficient tagging of heavy quarks through precise determination of displaced vertices:
  - → good single point resolution: σ_{SP}~3 μm
    - → small pixels <~25x25 μm², analog readout
  - → low material budget: X ≲ 0.2% X_0 / layer
    - → low-power ASICs (~50 mW/cm²) + air cooling

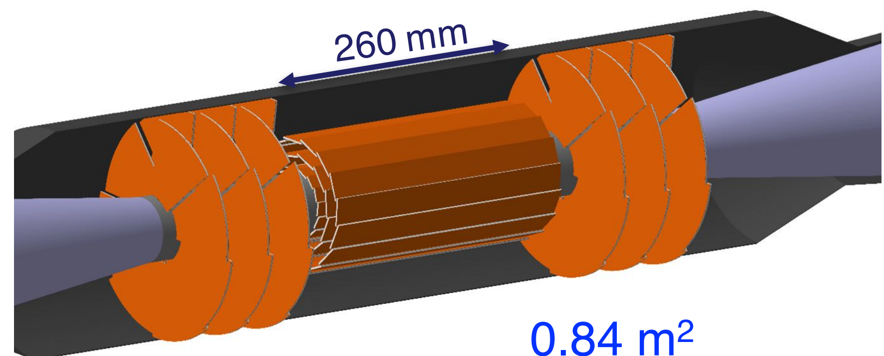
Tracker:

- Good momentum resolution: $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  - → 7 μm single-point resolution (~30-50 μm pitch in Rϕ)
  - → many layers, large outer radius (~100 m² surface)
  - → ~1-2% X0 per layer
    - → low-mass supports + services

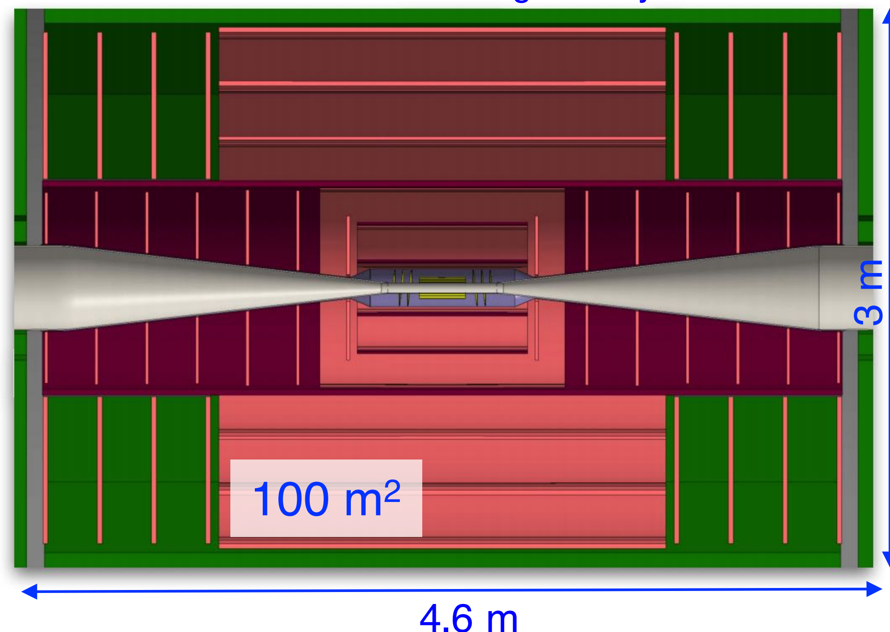
Both:

- 20 ms gaps between bunch trains
  - → trigger-less readout, pulsed powering
- few % maximum occupancy from beam backgrounds
  - → sets inner radius and limits cell sizes
  - → time stamping with few ns accuracy
    - → depleted sensors (high resistivity / high voltage)
- moderate radiation exposure (~10⁴ below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year

Vertex-detector simulation geometry



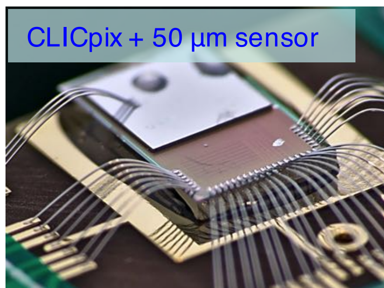
Tracker simulation geometry



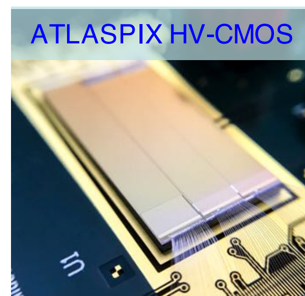
CLIC pixel-detector technology R&D

Summary and outlook

Sensor + readout technology	Considered for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker


CLICpix + 50 µm sensor

C3PD+CLICpix2 glue ass.

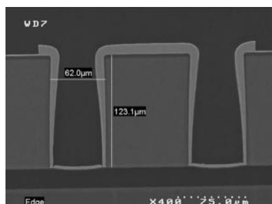

ATLASPIX HV-CMOS

INVESTIGATOR HR-CMOS

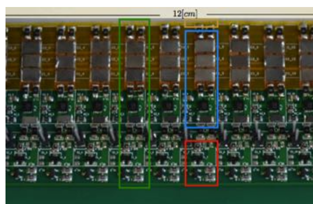
Cracow SOI

- Various sensor + readout technologies under study for CLIC vertex + tracking detector
- Examples of recent developments on the following slides

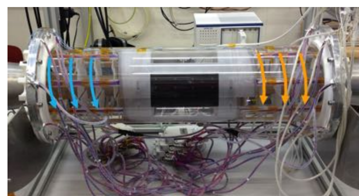
Interconnects



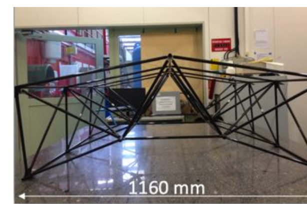
Powering



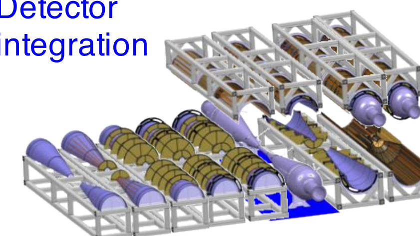
Cooling



Light-weight supports



Detector integration

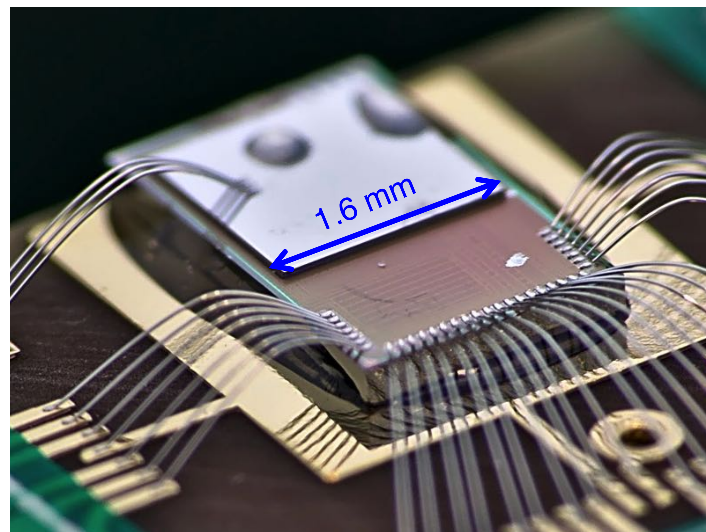


- Extensive detector integration studies → not covered in this presentation

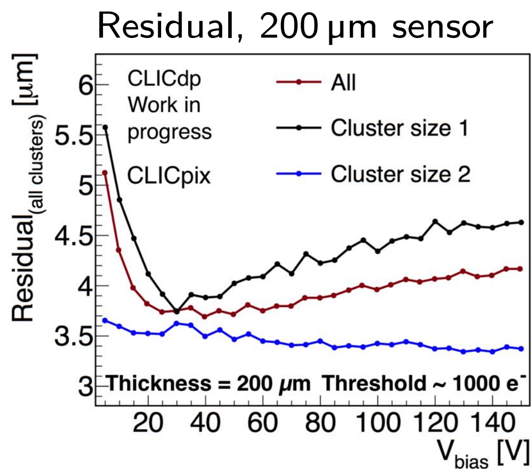
CLICpix planar-sensor assemblies

- 65 nm demonstrator CLICpix r/o ASIC:
  - 64 x 64 pixel matrix
  - **25 µm** pixel pitch
  - simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel
- Single-chip indium bump-bonding with 25 µm pitch at SLAC (C. Kenney, A. Tomada)
- Functional assemblies produced with 50-200 µm thick planar sensors (Micron, Advacam active edge)
- <4 µm single-point resolution for 200 µm thickness
- For 50 µm thickness not enough charge sharing, limits resolution to >~7 µm (~1300 e- threshold)

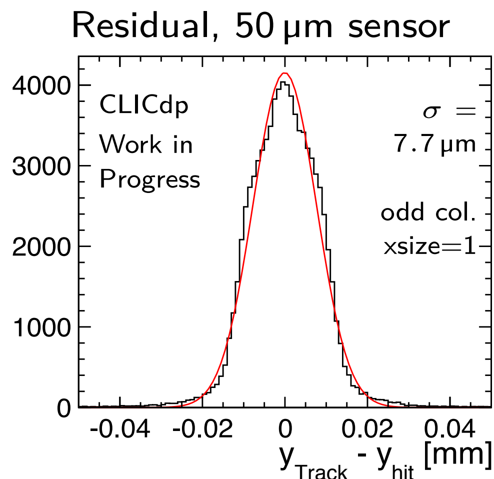
CLICpix with 50 µm planar sensor



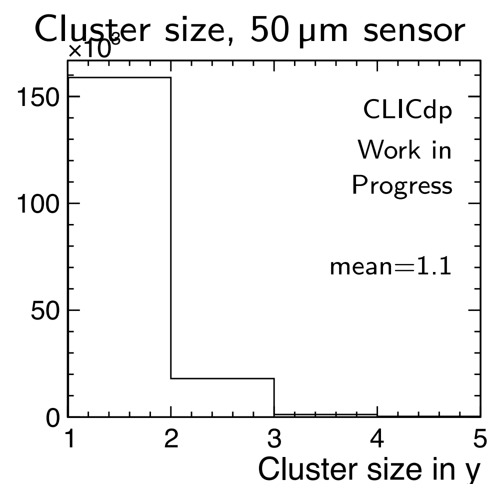
Residual, 200 µm sensor



Residual, 50 µm sensor



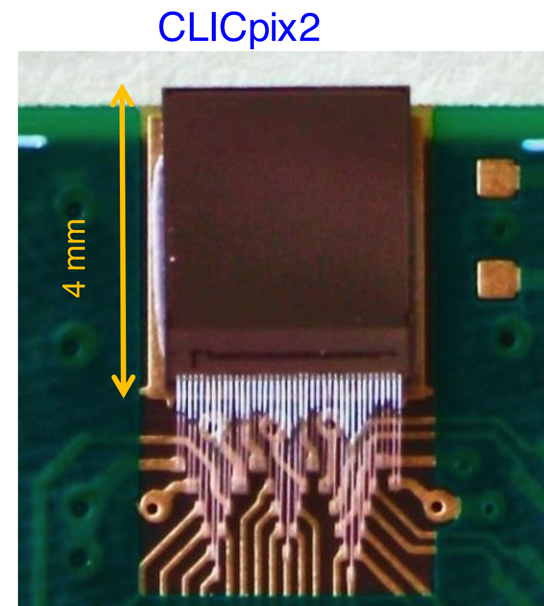
Cluster size, 50 µm sensor



CLICpix2 r/o ASIC

- New CLICpix2 in same 65 nm process as CLICpix:
  - Increased matrix size to 128 × 128 pixels
  - Longer counters for charge (5-bit) and timing (8-bit) measurements
  - Improved noise isolation and removal of cross-talk issue observed in first CLICpix
  - More sophisticated I/O with parallel column readout and 8/10 bit encoding
  - Integrated test pulse DACs and band gap

CLICpix2



- Test results with chips from Multi-Project-Wafer-Run
- Same chip on RD53 wafer, received in Dec 2017 (change from 5+1 to 7+1 metal layers)
  → access to full wafers for bump-bonding process development

CLICpix2 analog F/E specifications

Parameter	Value
Power dissipation	≤ 12 μW
Area	≤ 12.5x25 μm^2
Input charge, Q_{in}	nominal 4 ke-, max. 40 ke-
Minimum threshold, $Q_{th,min}$	≤ 600 e-
Equivalent input-referred noise, $Q_{n,in}$	≤ 70 e-
ToT dynamic range	≥ 40 ke-
ToA accuracy	≤ 10 ns
Total ionizing dose (for 10 yr)	1 Mrad
Input charge types	e-, h+
Testability	in-pixel test pulse (i.e. Q_{test}) injection

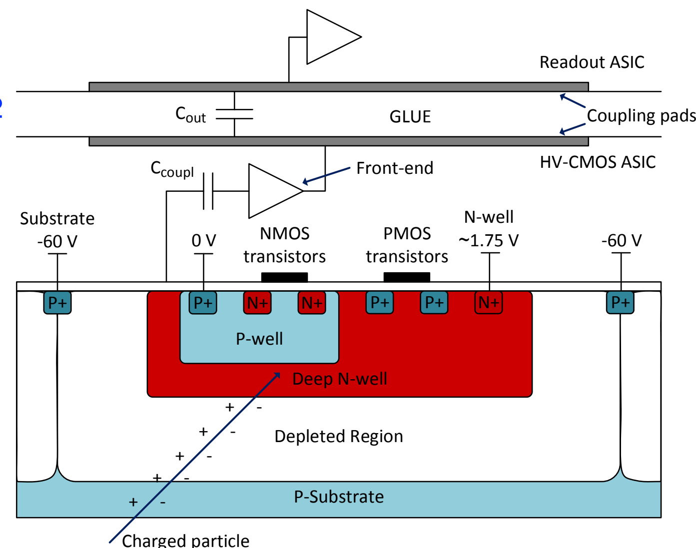
C3PD HV-CMOS sensors

- C3PD: active HV-CMOS sensor for capacitive coupling
- Commercial 180 nm High-Voltage CMOS process: transistors in deep n-well, acting as collecting electrode
- Footprint matching CLICpix2: 128 x 128 pixels, 25x25 μm^2
- Charge Sensitive Amplifier (CSA) + unity gain buffer

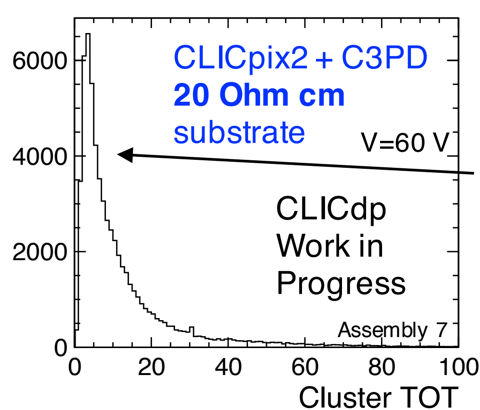
- Production wafers of various resistivities: 20, 80, 200, 1000 Ohm cm
- Test-beam results for standard bulk resistivity: ~20 Ohm cm, ~15 μm depletion at 60 V

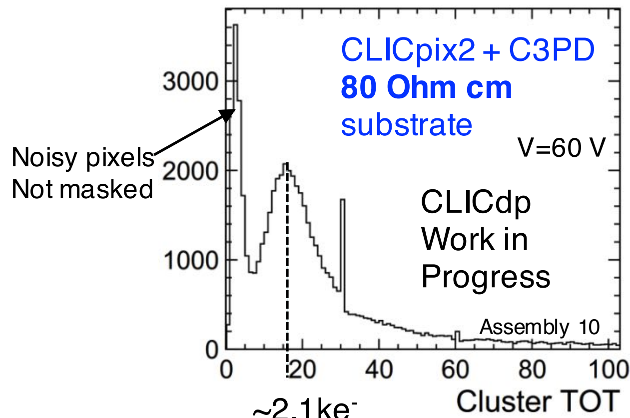
- First lab tests for assemblies with 80 Ohm cm confirm larger drift signal, increased active depth ~25 μm

Schematic cross section of C3PD

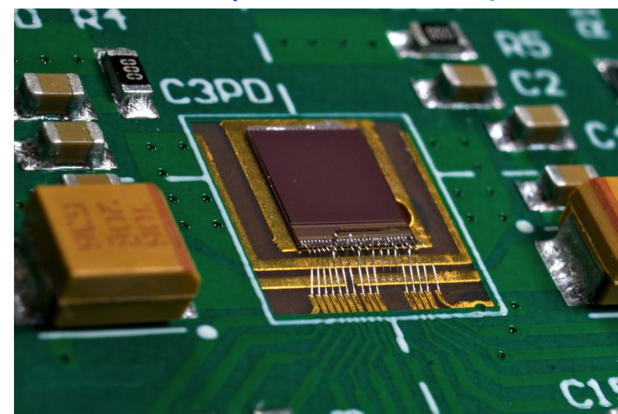


Sr-90 source exposure





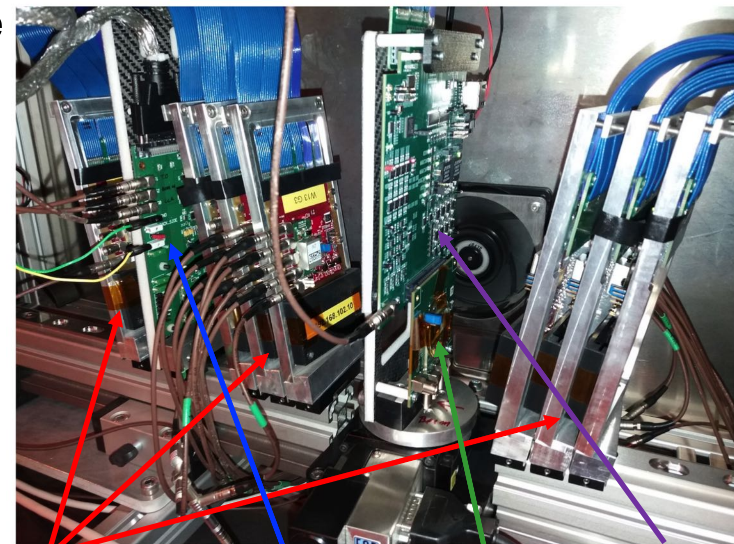
C3PD chip thinned to 50 μm



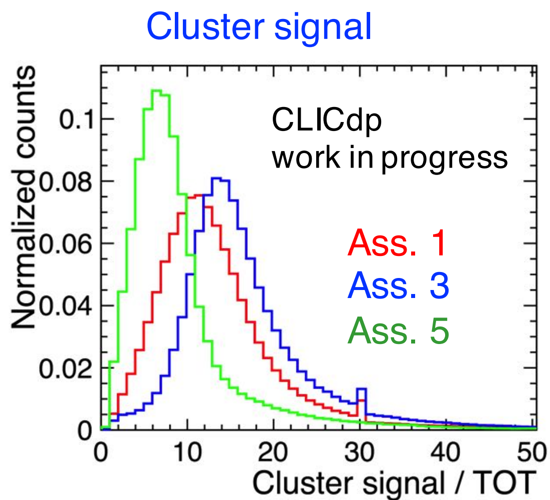
C3PD+CLICpix2 in test beam

- Test-beam measurements in CLICdp Timepix3 telescope for 5 assemblies with 20 Ohm cm substrate:
  - C3PD bias scans
  - CLICpix2 threshold scans
  - Angles between 0º (perpendicular) and 30º
- Analysis in progress
- Preliminary results show difference in cluster signals and sizes (varying glue-assembly quality)
- Similar residuals of 8.5-9 µm (threshold <~1000 e^-), as expected from low cluster multiplicities
- Expect improved performance for high-res. substrates

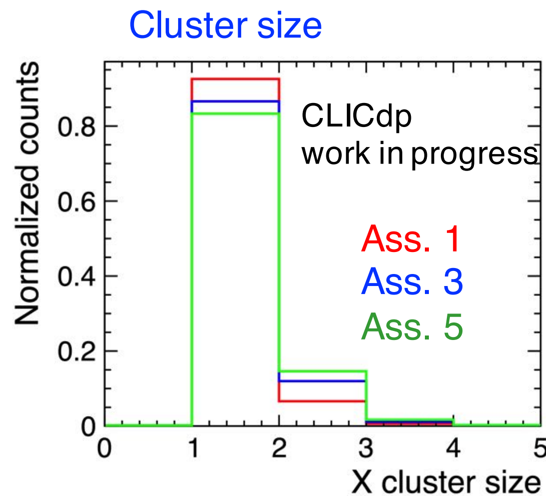
C3PD+CLICpix2 assembly in Timepix3 telescope



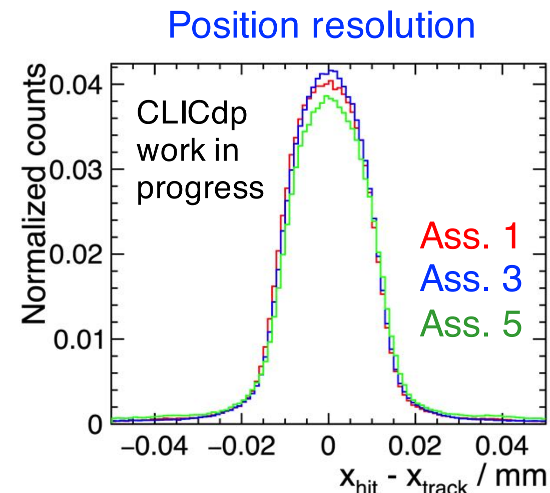
Cluster signal



Cluster size



Position resolution

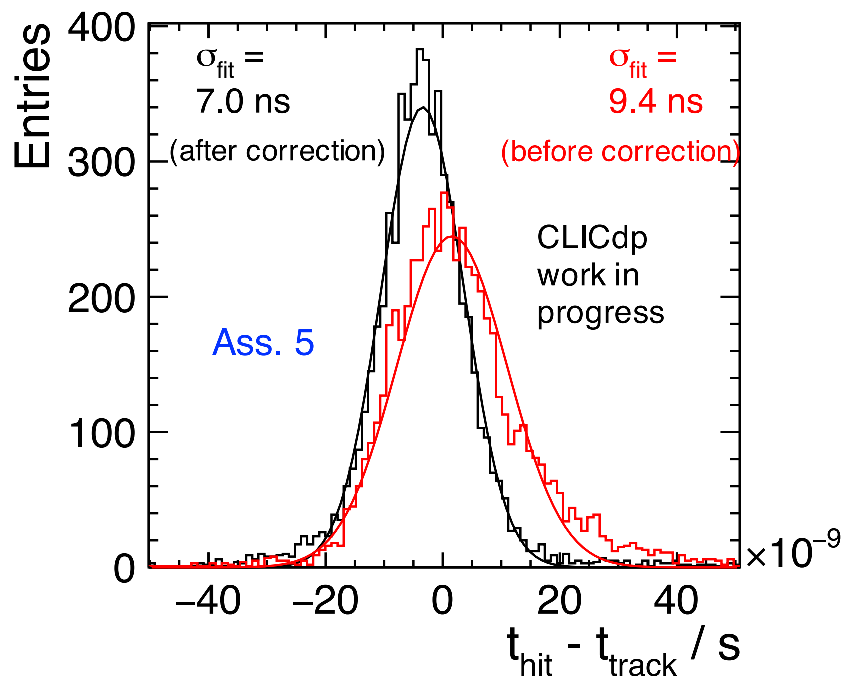


C3PD+CLICpix2 time resolution

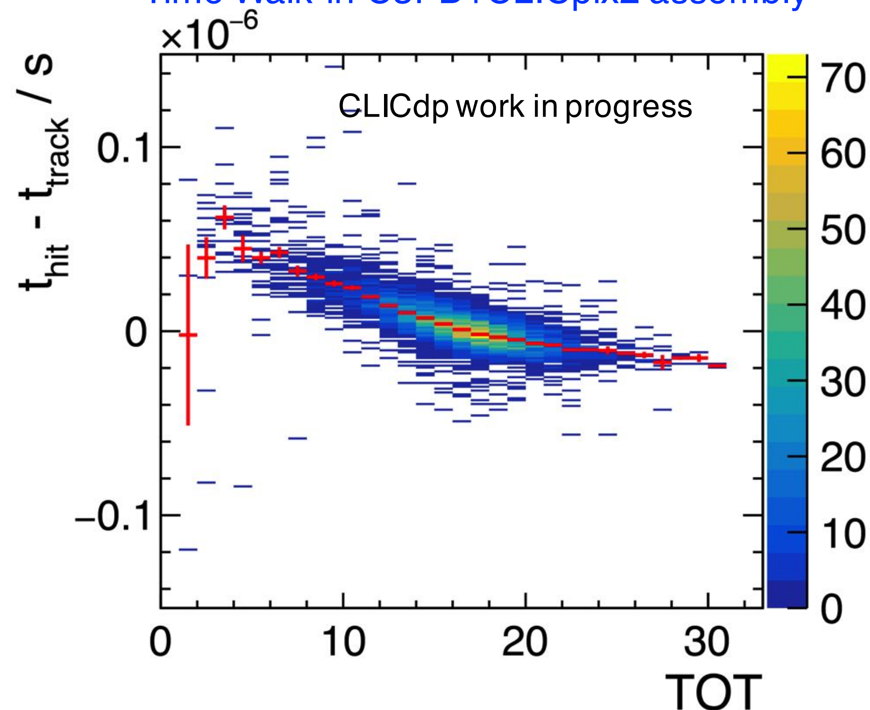
- Track time resolution of CLICdp Timepix3 telescope <~1 ns
  → precise characterization of DUT timing capabilities
- CLICpix2: 100 MHz ToA clock → 10 ns time binning
- Gauss fit of time residuals shows width of ~9 ns
- Tail towards later times, as expected from time walk

→ Time residual reduced to ~7 ns after time-walk correction

Hit time residuals in C3PD+CLICpix2 assembly



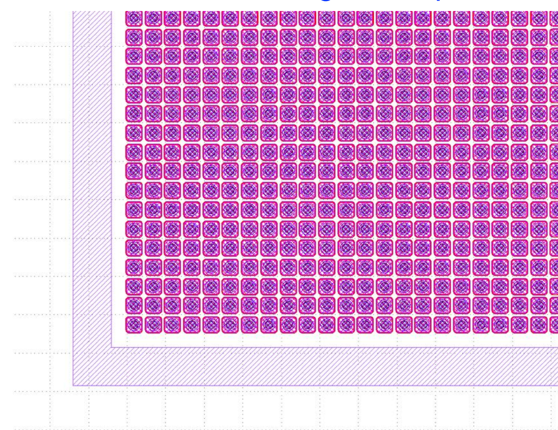
Time Walk in C3PD+CLICpix2 assembly



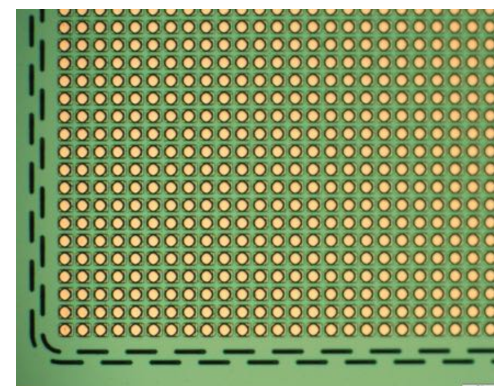
Planar sensors on CLICpix2

- Test results with planar sensors (25x25 μm^2 pitch) needed for full assessment of CLICpix2 performance
- Planar active-edge CLICpix2 sensors with UBM available:
  - Advacam MPW production with ATLAS (50-150 µm thick)
  - FBK AIDA-2020 production (120 µm thick)
- Single-chip bump-bonding on carrier wafers in progress at IZM + thinning of ASICs
- Future plan: develop wafer-level bump deposition process for CLICpix2 wafer from RD53 submission

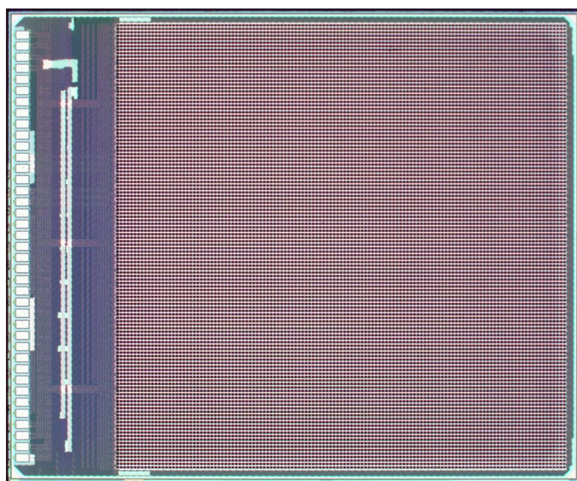
Advacam active-edge CLICpix2 sensor



FBK active-edge CLICpix2 sensor



Bumped CLICpix2 ASIC



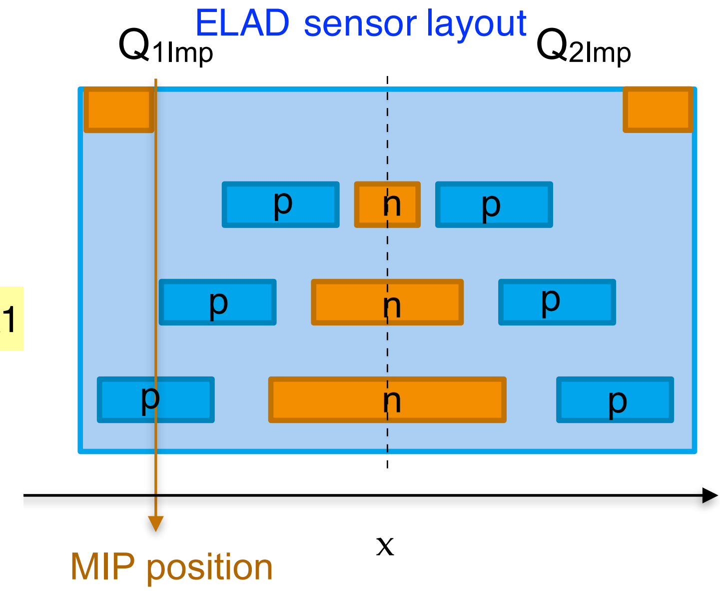
RD53 12" wafer with CLICpix2

ELAD sensors

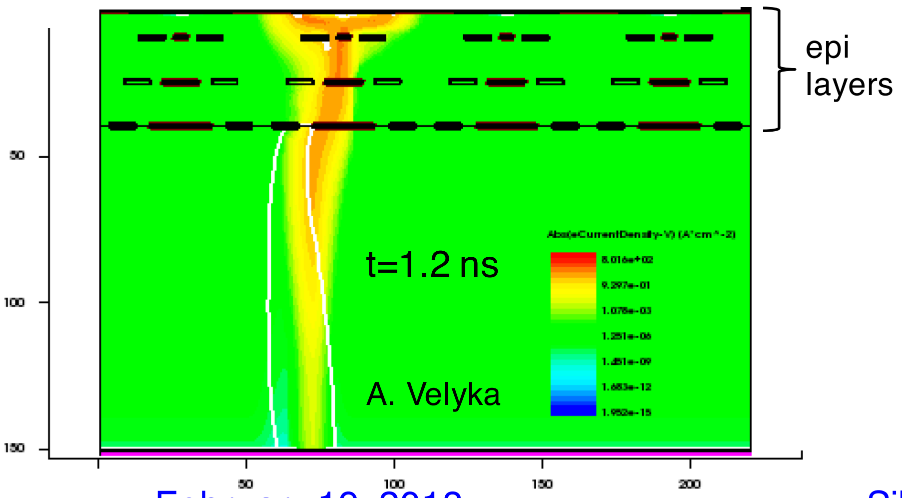
- Position resolution in very thin sensors so far limited to ~pixel pitch / √12 (almost no charge sharing)
- New sensor concept for enhanced charge sharing **E**nhanced **LA**teral **D**rift sensors (ELAD), H. Jansen (DESY/PIER)
- Deep implantations to alter the electric field
  → lateral spread of charges during drift, cluster size ~2
  → improved resolution for same pitch
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- Ongoing TCAD simulations:
  - Implantation process
  - Sensor performance for MIPs
- First production in 2018: generic test structures, strips and test sensors with Timepix footprint (55 µm pitch)

Patent DE102015116270A1

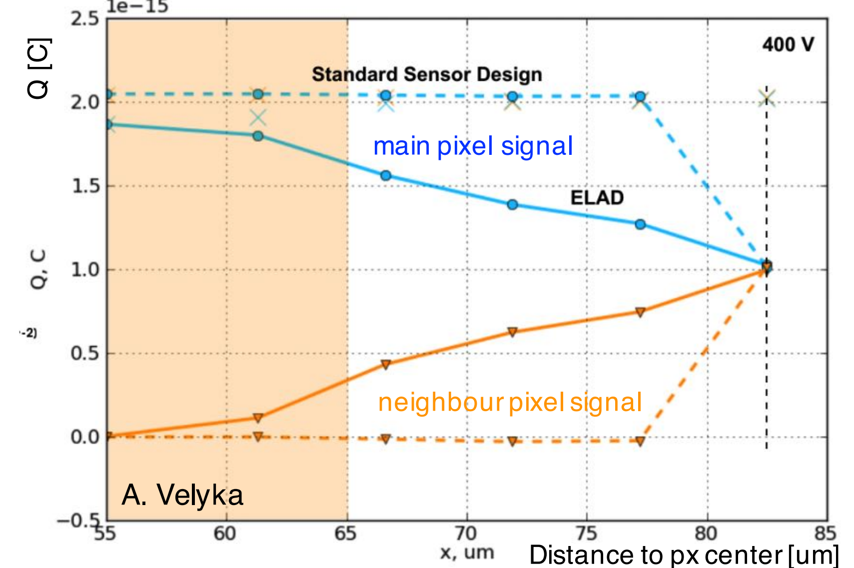
ELAD sensor layout



TCAD simulation of current from MIP



Integrated charge as function of MIP position



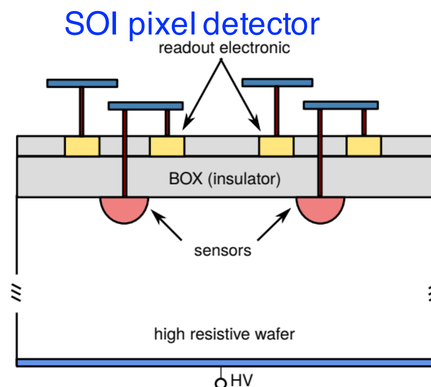
Monolithic SOI sensors

Summary and outlook

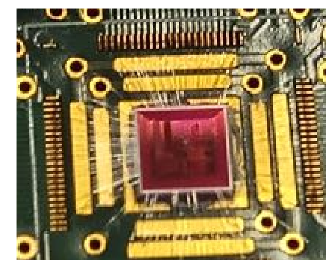
- Sensor and electronics integrated on single wafer with high-resistivity substrate, separated by insulation oxide layer + buried p-wells,
- Considered for vertex and tracker

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, different r/o schemes
- Test results for 500 µm thickness, 30x30 μm^2 pitch, rolling-shutter r/o: >99% efficiency, σ_{SP}<~2 µm

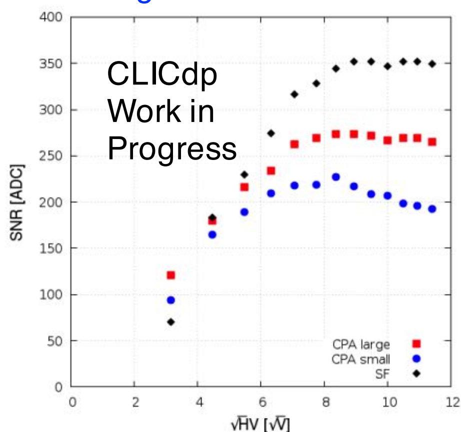
SOI pixel detector



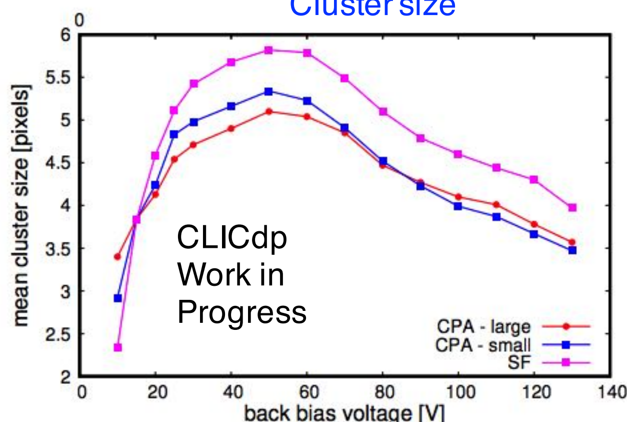
Cracow SOI test chip



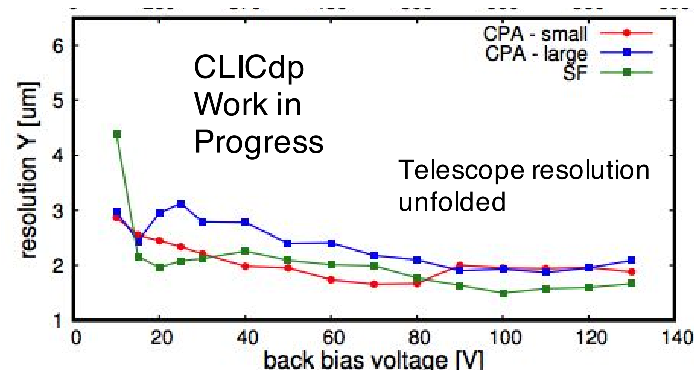
Signal-to-Noise



Cluster size



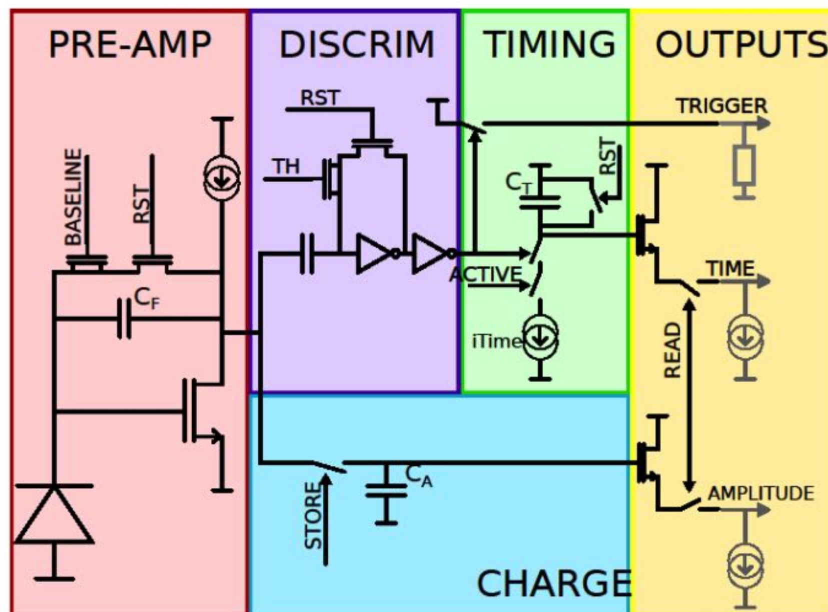
Resolution in y-direction



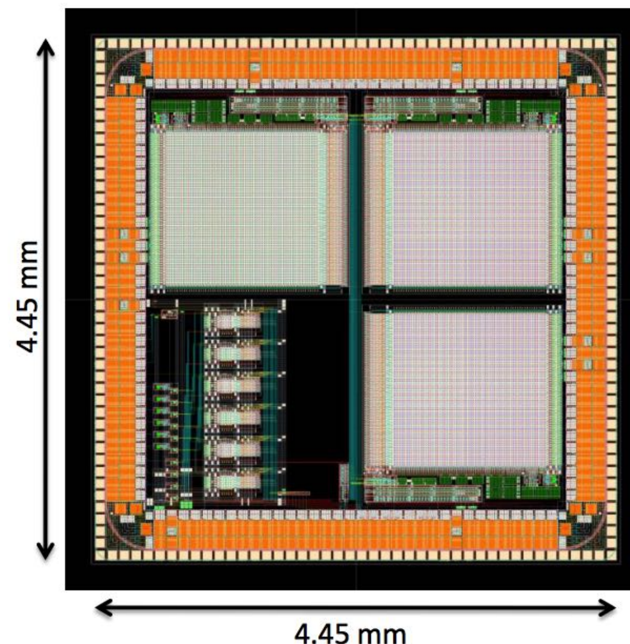
CLIPS SOI sensor

- CLIPS: New AGH SOI chip design targeted to Linear Collider VTX detectors:
  - 64x64 matrix with 20x20 μm² pixels
  - Targets spatial resolution <3 μm, time resolution <10 ns
  - Analog charge and time information in storage capacitors in each pixel
    → no need for fast clock distribution into matrix
  - Snapshot analog readout between bunch trains with external ADC
  - On chip trigger to reduce the data rate
  - Chip submitted November 2017
    → 300-500 μm thick samples expected in April 2018
    → 75-100 μm thinned wafers ~June 2018

CLIPS pixel design



CLIPS layout

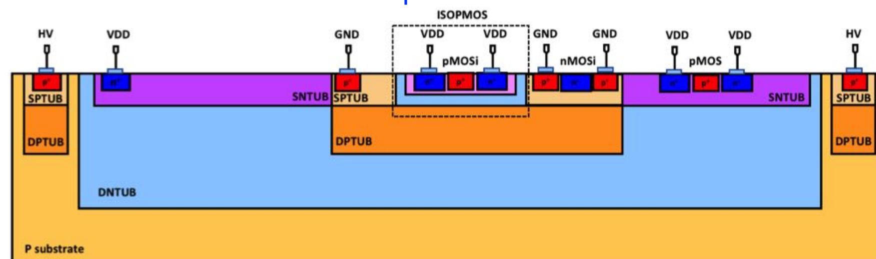


Monolithic HV-CMOS: ATLASPIX

180 nm HV-CMOS process:

- Fully integrated chip designed for ATLAS ITk upgrade
- Process modification: isolated PMOS
- 25 x 400 pixels, 130 µm x 40 µm pixel size
- 20-1000 Ω cm substrates
- Charge amplifier, discriminator in pixel
- ToT and ToA in periphery (point-to-point connection)

ATLASPIX process cross section

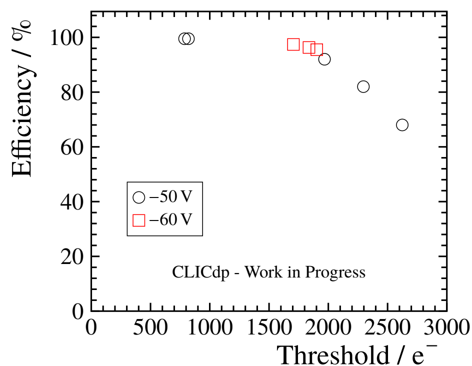


I. Peric et al.

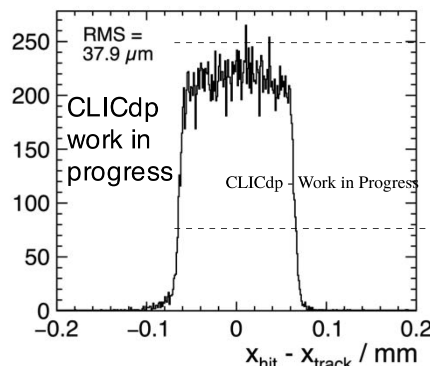
Tests for 80 Ω cm ATLASPIX_Simple in view of CLIC tracker requirements:

- Laboratory calibration and beam tests in CLICdp Timepix3 telescope at CERN SPS
  - Efficiency 99.6%
  - Limited charge sharing → box-shaped residuals, σ~pitch/√12
  - Time resolution ~30 ns, dominated by 10 MHz r/o clock, to be improved with new Caribou r/o system

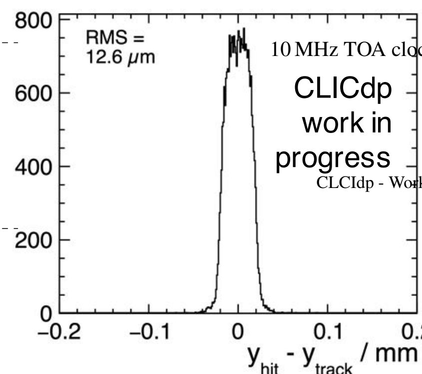
Efficiency



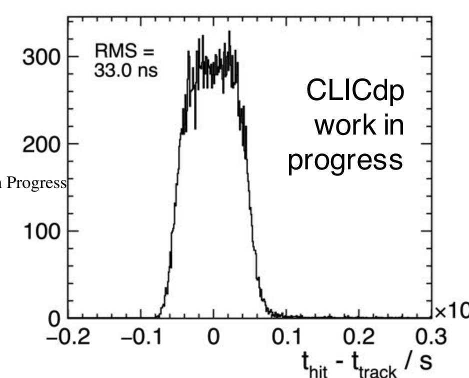
Residual in column direction



Residual in row direction



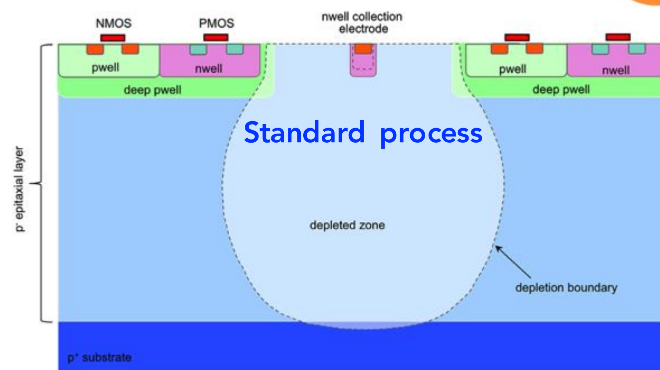
Timing residual



Monolithic HR-CMOS: INVESTIGATOR

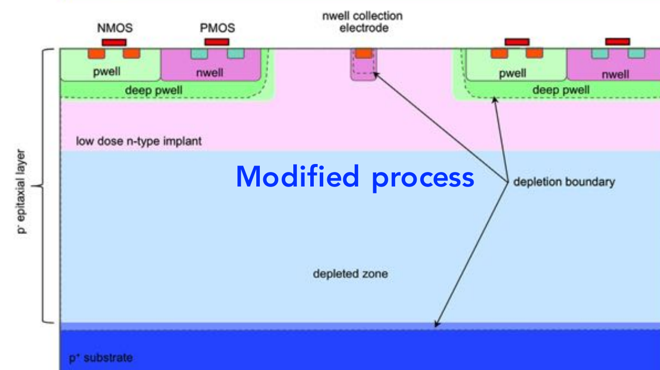
180 nm HR-CMOS process:

- High-Resistivity epitaxial layer (15-40 µm, 1-8 kΩ cm)
- CMOS circuitry shielded by deep P-well
- Small collection diode → small capacitance:
  - Maximise signal/noise
  - Low analogue power consumption and fast timing
- Frontside biasing:
  - Bias voltage limited by CMOS transistors to -6 V



Modified process:

- Additional low-dose N-implant to achieve full lateral depletion:
  - Improved radiation tolerance
  - Faster charge collection
  - Backside biasing possible (not limited to -6 V)

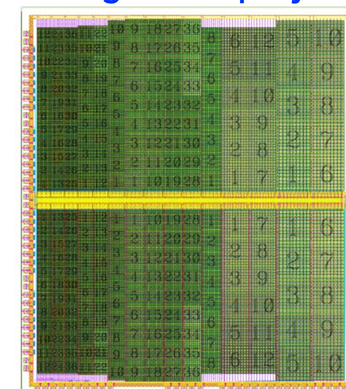


http://dx.doi.org/10.1016/j.nima.2017.07.046

INVESTIGATOR test chip developed for ALICE (W. Snoeys et al.):

- 134 mini-matrices with 8 x 8 pixels (variation of pixel size, collection electrode size, …)
- Source follower in each pixel, analog signals routed to periphery
- Readout with external 65 MHz sampling ADC per pixel
- Beam tests in CLICdp Timepix3 telescope, using chips with 25 µm epi thickness and 28 µm pitch, both processes

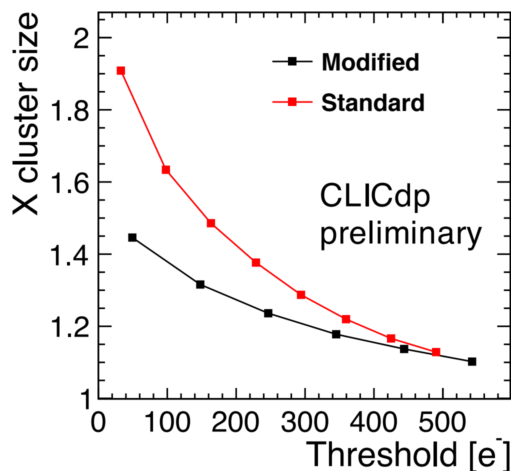
Investigator chip layout



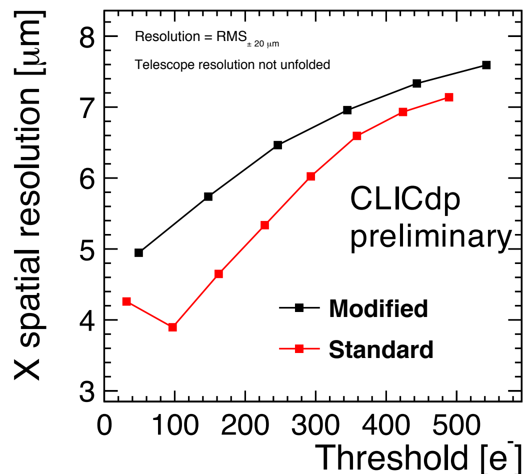
INVESTIGATOR resolution and efficiency

Impact of charge sharing on spatial resolution and efficiency for standard & modified process (pitch of 28 µm, bias voltage of -6 V):

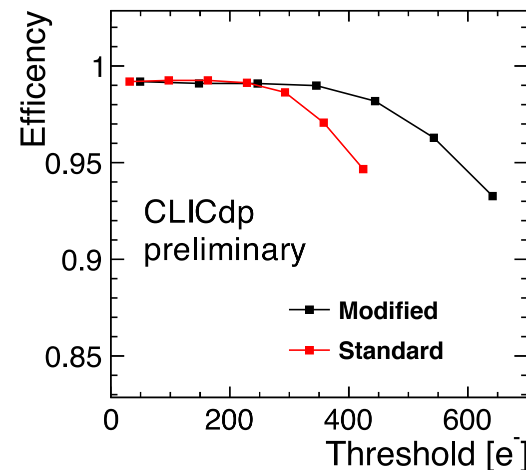
X cluster size vs. threshold:



X resolution vs. threshold:



Efficiency vs. threshold:



- More charge sharing for standard process
- Expected from non depleted regions (diffusion)

- Better spatial resolution for standard process down to ~ 3.5 µm

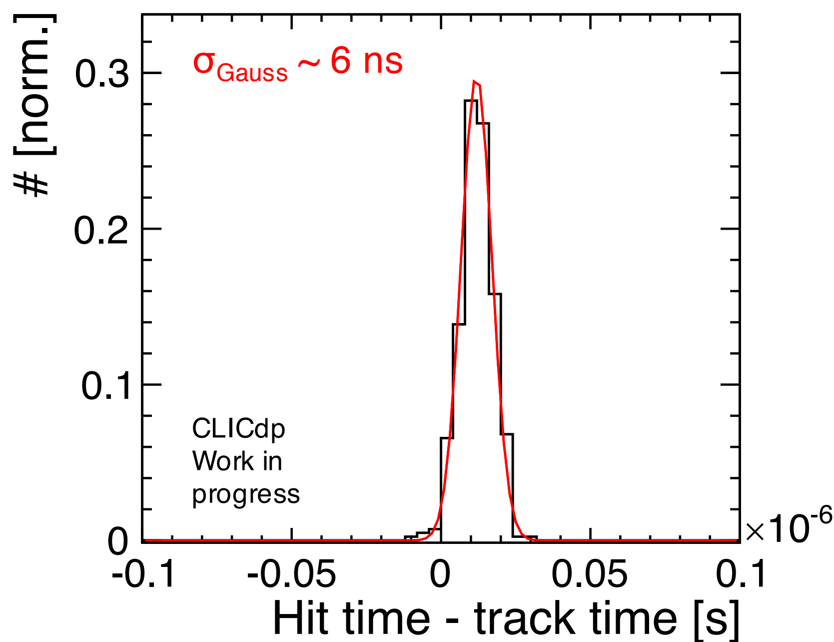
- Earlier drop of efficiency (at lower thresholds) for standard process

→ Efficiency & spatial resolution for both process variants within requirements for CLIC tracker.

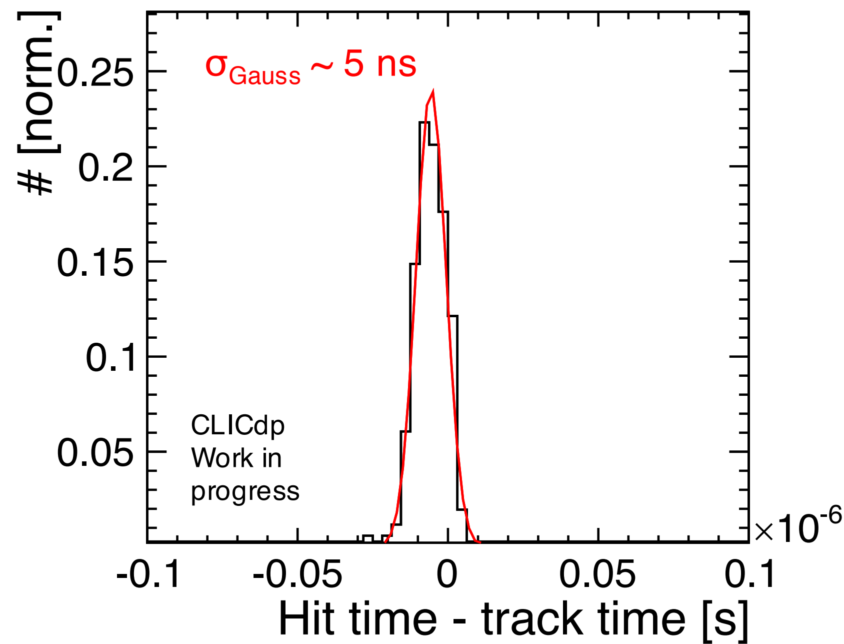
INVESTIGATOR timing

Timing resolution for standard & modified process (pitch of 28 μm, bias voltage of - 6 V):

Standard process:



Modified process:



Comparable timing resolution for both processes
(Readout sampling frequency of 65 MHz limits achievable precision)

CLICTD monolithic HR-CMOS tracker chip

Good performance of studied 180 nm HR-CMOS technology with respect to requirements of CLIC tracker
→ Technology used for ongoing design of a fully integrated chip for the CLIC tracker

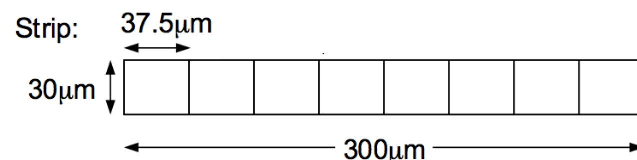
CLIC Tracker Detector (CLICTD) – monolithic HR-CMOS sensor with 30 μm x 300 μm pixels

Segmented macro-pixel structures to maintain advantages of small collection diode (prompt and fully efficient charge collection) while reducing digital logic:

Discriminator output of 8 collection diodes combined in logical OR

Output of logical OR passed to digital circuitry:

- Simultaneous 8-bit ToA and 5-bit ToT measurements
- Expect σ_{SP}~7 μm in short direction (charge sharing)
- Hit bit pattern → maintain good resolution also in long direction
- 100 MHz clock to achieve 10 ns time binning

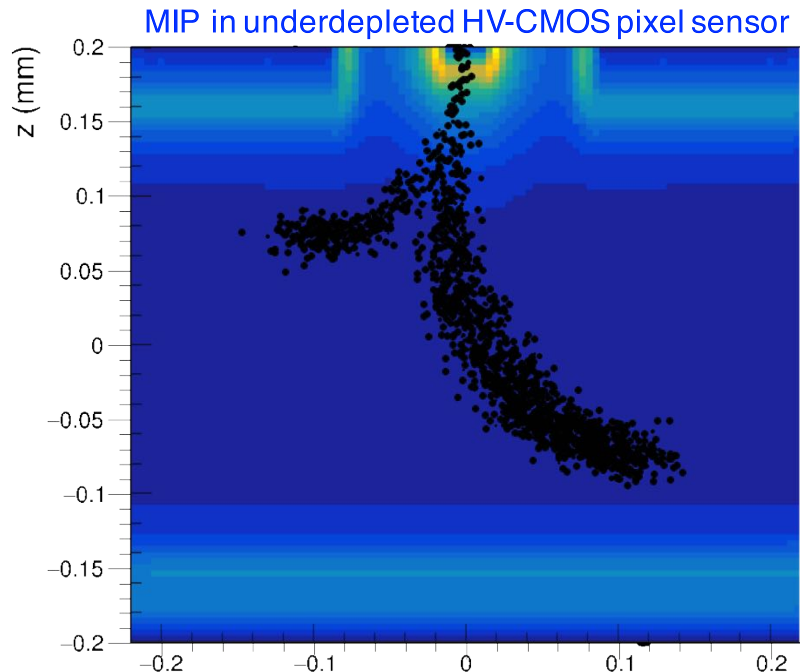


Chip design in progress, target submission date: ~May 2018

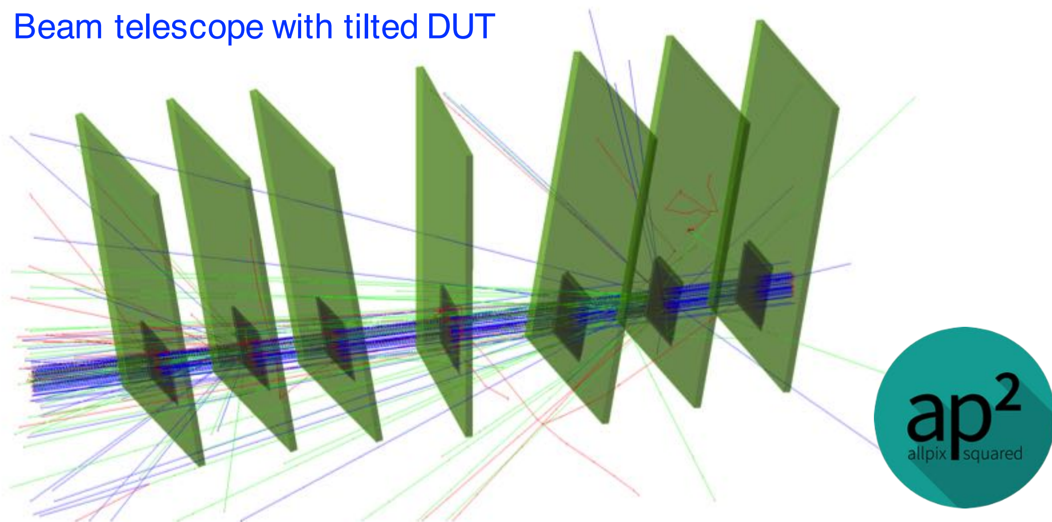
Allpix² simulation framework

- Modular simulation framework for silicon tracking detectors
- Simulates full chain from incident radiation to digitized hits
- Modern and well-documented C++ code
- Full Geant4 simulation of charge deposition
- Fast charge propagation using drift-diffusion model, can import electric fields in the TCAD DF-ISE format
- Simulation of HV-CMOS sensors with capacitive coupling
- Easy to add new modules for new digitizers, other output formats, etc.
- For Introduction, User manual and code reference visit: https://cern.ch/allpix-squared

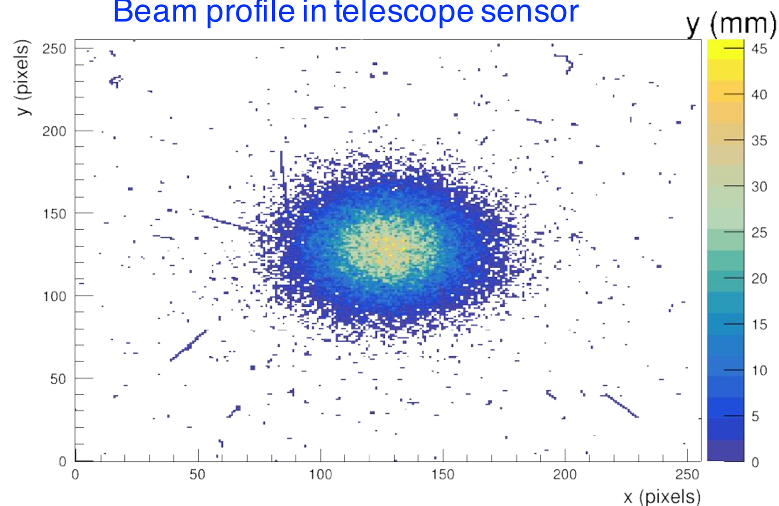
MIP in underdepleted HV-CMOS pixel sensor



Beam telescope with tilted DUT



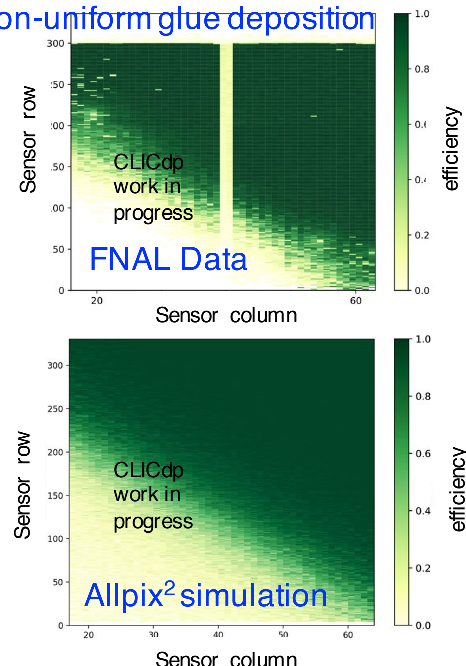
Beam profile in telescope sensor



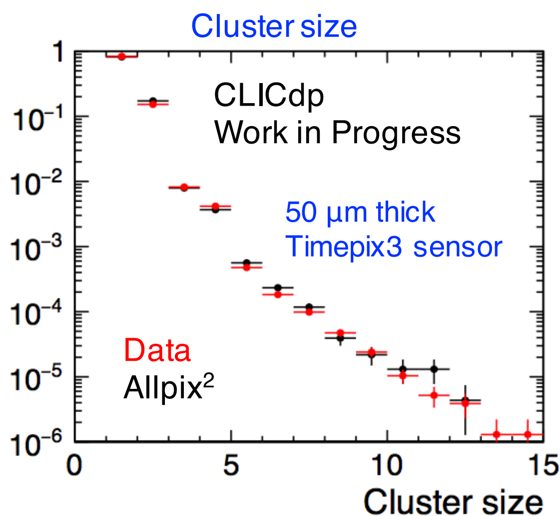
Allpix^2 validation

- Validation ongoing using test-beam data:
  - Timepix3 planar sensor assemblies:
    Charge distribution, cluster size and spatial residuals in good agreement with test beam data
- New sensor types and features are being added by users:
  - SOI pixel detectors
  - capacitively coupled HV-CMOS sensors
  - ELAD sensors
  - …

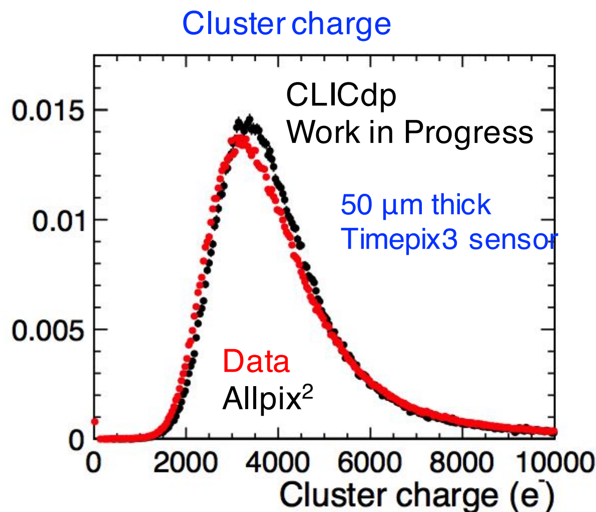
FEI4/H35DEMO: capacitive coupling with non-uniform glue deposition



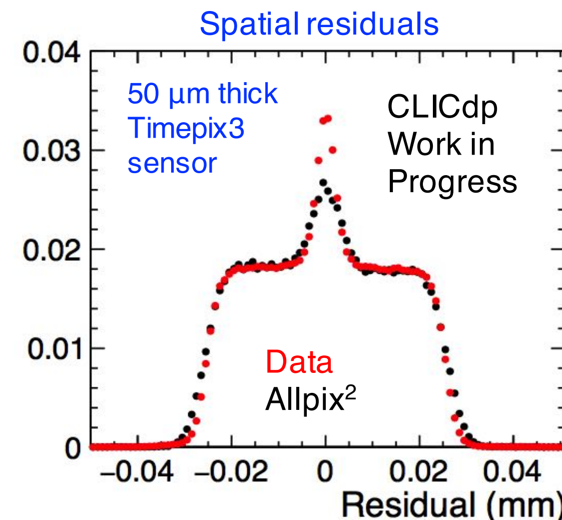
Cluster size



Cluster charge



Spatial residuals



Summary

- Challenging requirements for CLIC vertex+tracking detectors
- Ongoing broad and integrated R&D program:
  - Sensor and readout technologies for precision measurements:
    - Hybrid readout ASICs with planar sensors
    - Hybrid readout ASICs with active HV-CMOS sensors
    - Integrated CMOS sensors
  - Sensor and readout simulation framework Allpix^2
  - Not shown today: powering, cooling and mechanical integration studies incorporating realistic constraints

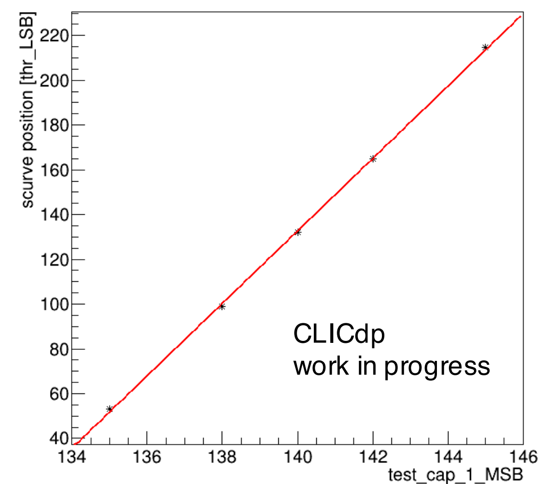
Thanks to everyone who provided material for this talk!

Additional Material

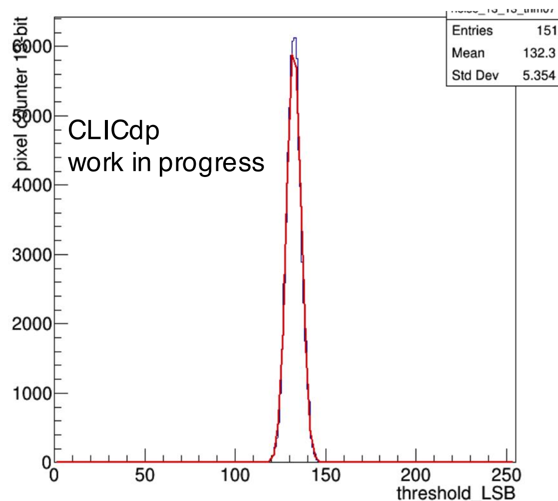
CLICpix2 characterization

- Standalone characterization of CLICpix2 to verify functionality and performance
- 61 e^- noise measured,
  67 e^- expected from simulations
- Homogenous threshold distribution over matrix after trimming
- Linear front-end response to test pulses

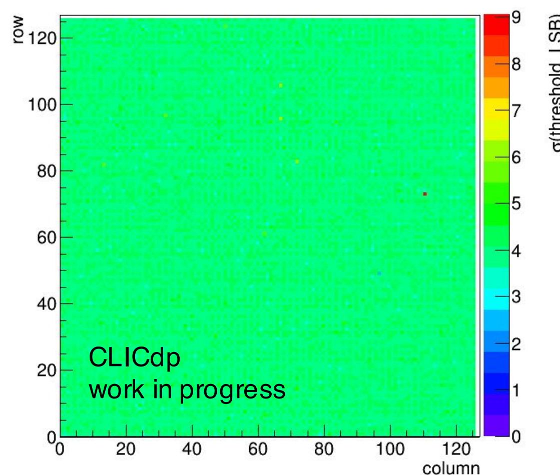
Amplifier linearity



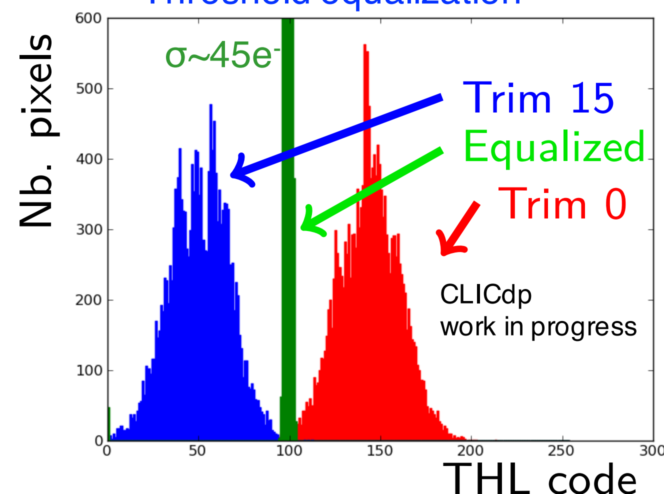
Noise scan for one pixel



Uniformity of noise

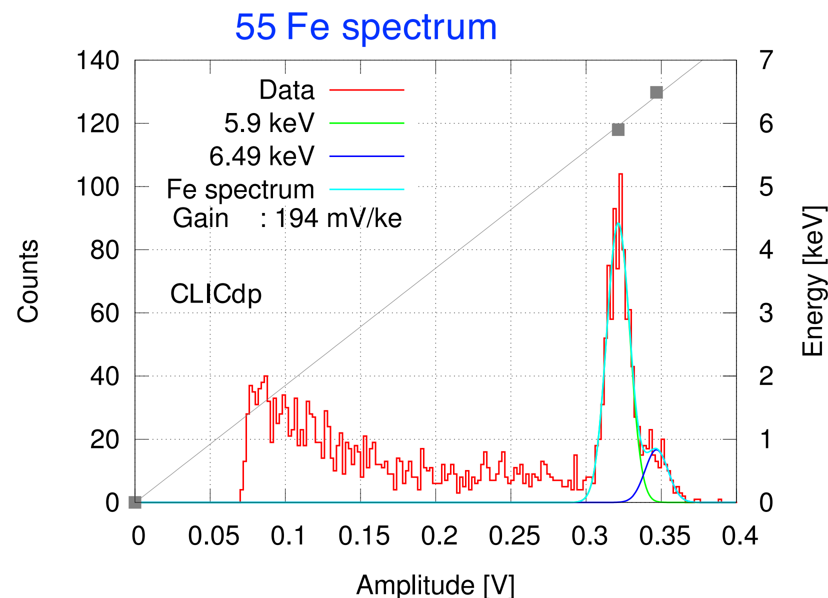


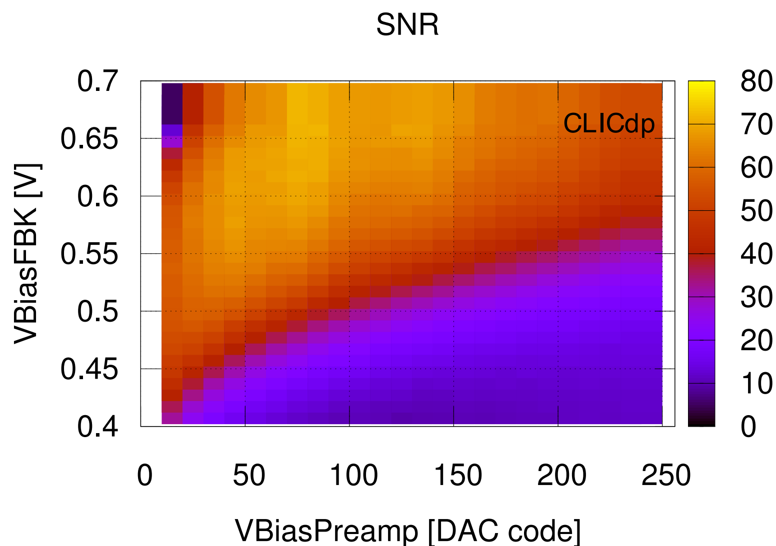
Threshold equalization

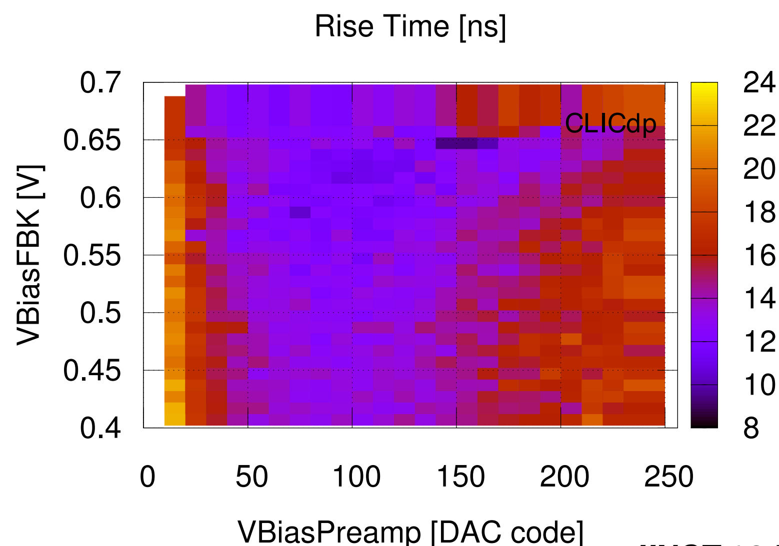


C3PD characterization

- Standalone characterization of C3PD:
  - Noise
  - Internal test pulses
  - Source calibration with ^{55}Fe
- Results according to expectations from simulations:
  - RMS noise: 40 e-
  - Average charge gain: 190 mV / ke^{-}
  - Rise time: 20 ns
  - Power consumption: 5 µW / pixel (continuous)
  - Samples thinned to 50 µm show same performance as standard 250 µm ones
- Optimization of operation parameters (S/N, rise time, power consumption)







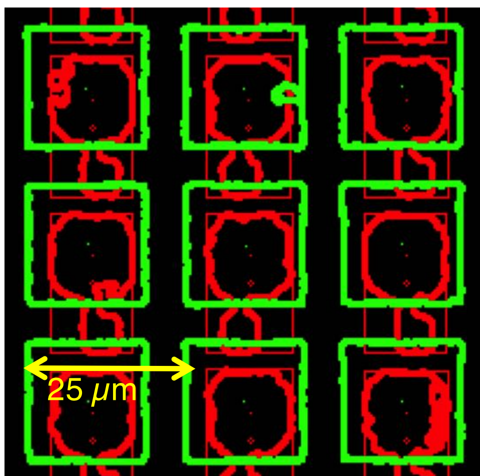
JINST *12 P09012*

C3PD+CLICpix2 glue assemblies

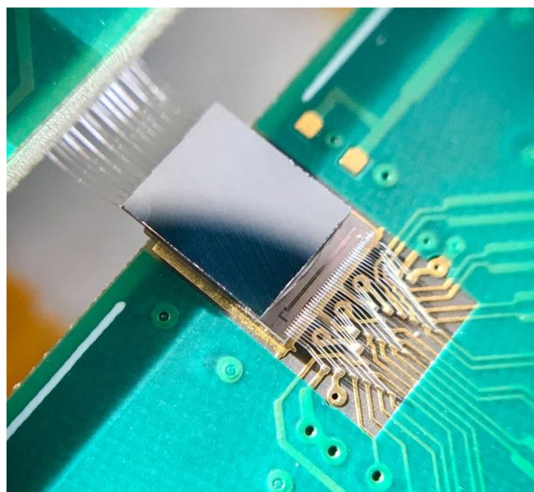
- Production of glue assemblies with C3PD and CLICpix2
  - Semi-automatic flip-chip bonder SET Accura 100
  - Epoxy glue deposition with automatic dispenser
  - *PixelShop* alignment software with pattern recognition
  - Curing at high temperature (100 ^{o}C) and force (5-20 N)
  - Ongoing optimization of production parameters:
    - Uniformity of glue deposition
    - Alignment precision
    - Planarity of flip-chip bonder
    - Curing parameters

Semi-automatic flip-chip bonder

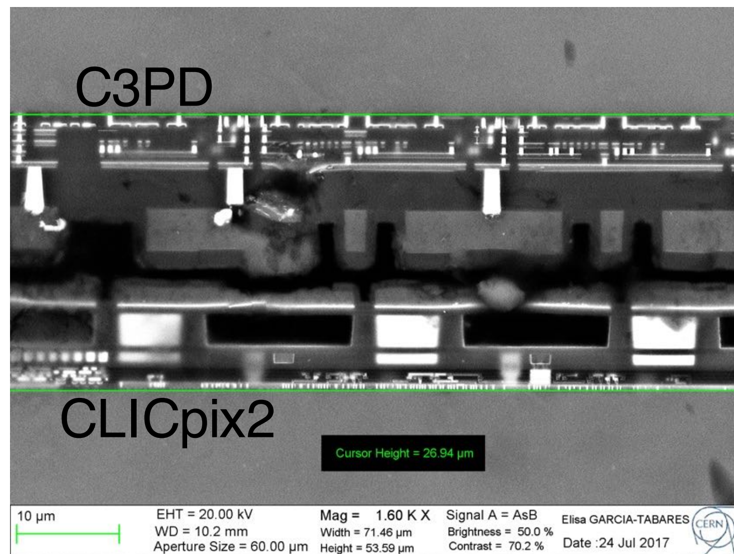
PixelShop alignment tool



C3PD + CLICpix2 glue assembly



Cross section of C3PD + CLICpix2 glue assembly



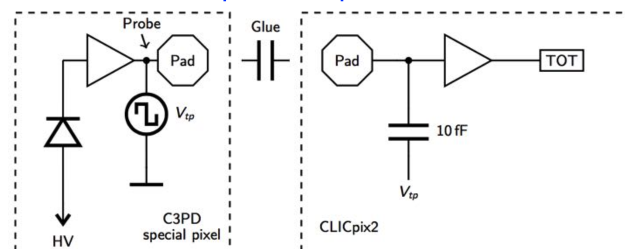
C3PD+CLICpix2 calibration

Complex signal chain with several transfer functions, which are difficult to determine:

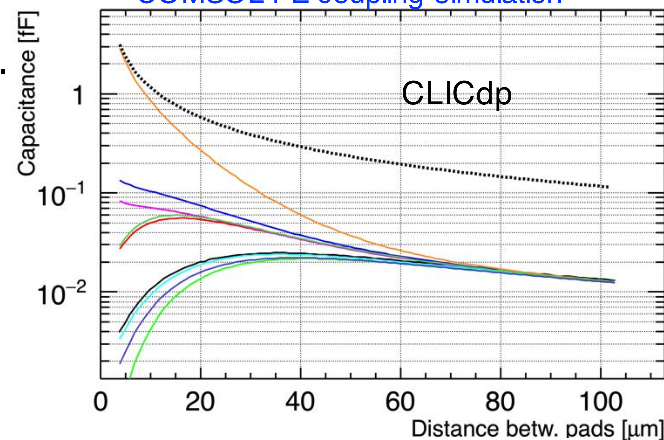
- Transient charge signal in C3PD
  → TCAD / TCT meas.
- C3PD circuit response
  → Circuit simulation / Test pulses, sources
- Capacitive coupling
  → COMSOL FE simul. / cross sections, test-structure meas.
- CLICpix2 response
  → Circuit simulation / Test pulses, planar-sensor meas.

- Characterization and calibration in progress
- Preliminary results show importance of glue uniformity and alignment

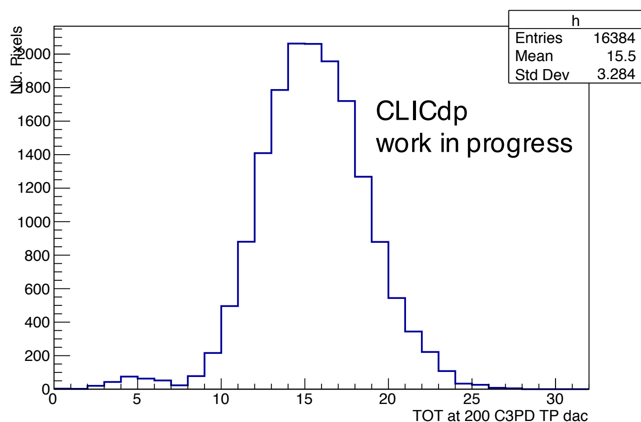
C3PD / CLICpix2 test pulses

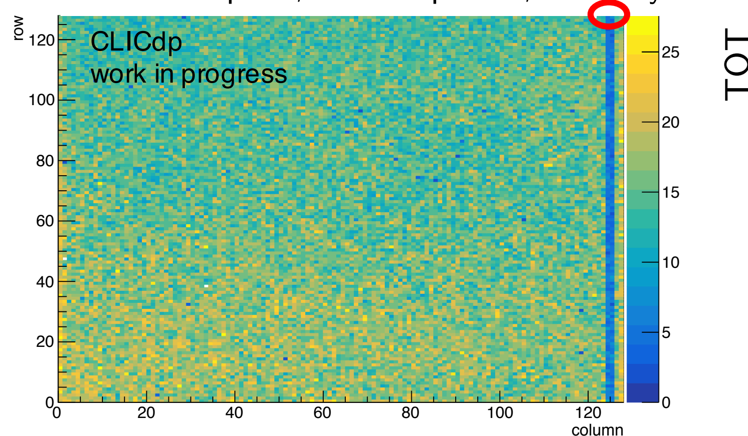


COMSOL FE coupling simulation



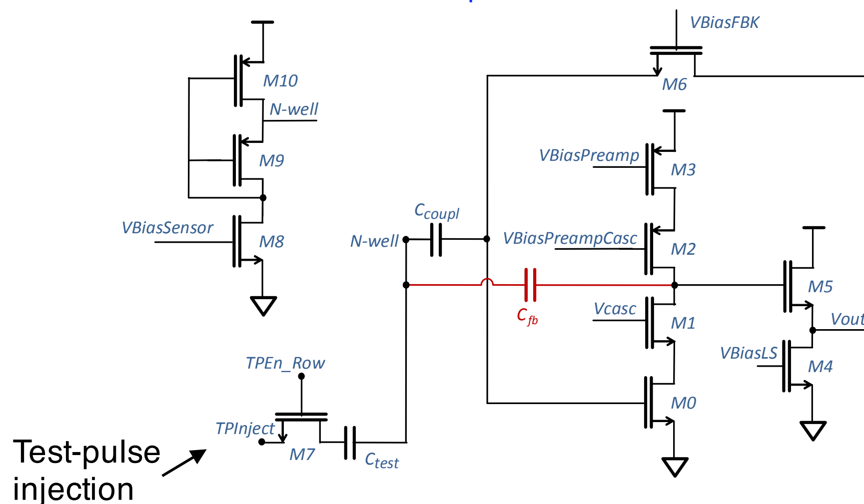
CLICpix2 ToT response to C3PD test pulses



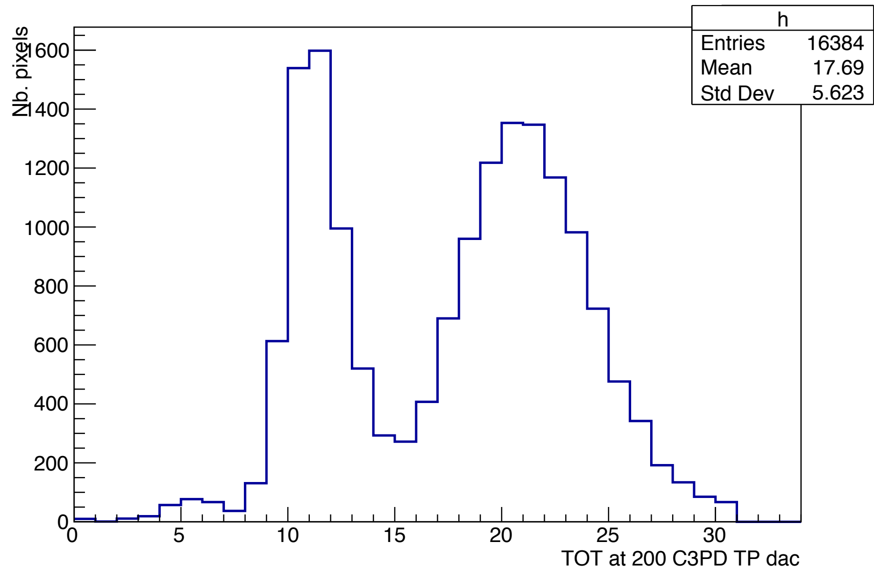


C3PD+CLICpix2 calibration

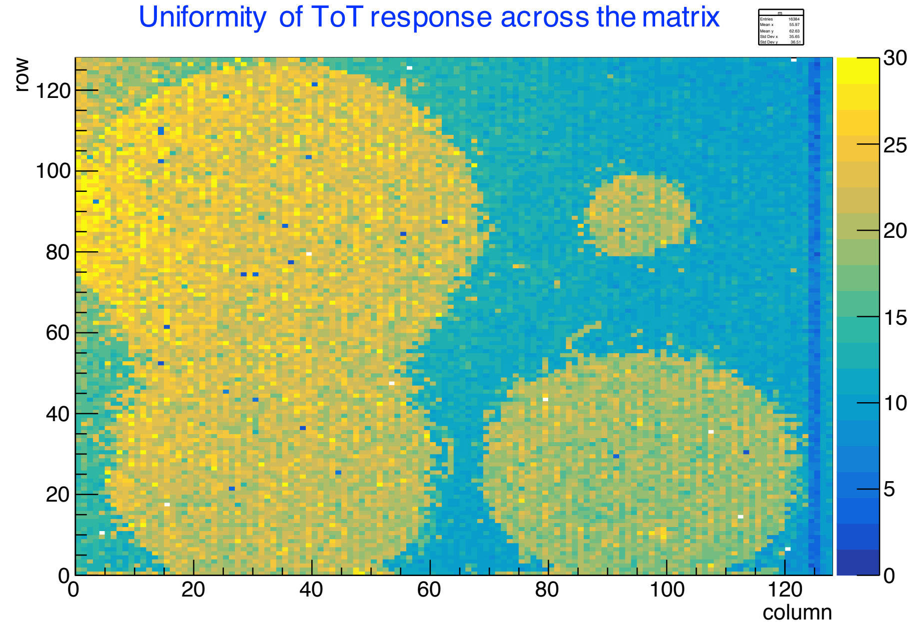
C3PD pixel schematic



CLICpix2 ToT response to C3PD test pulses

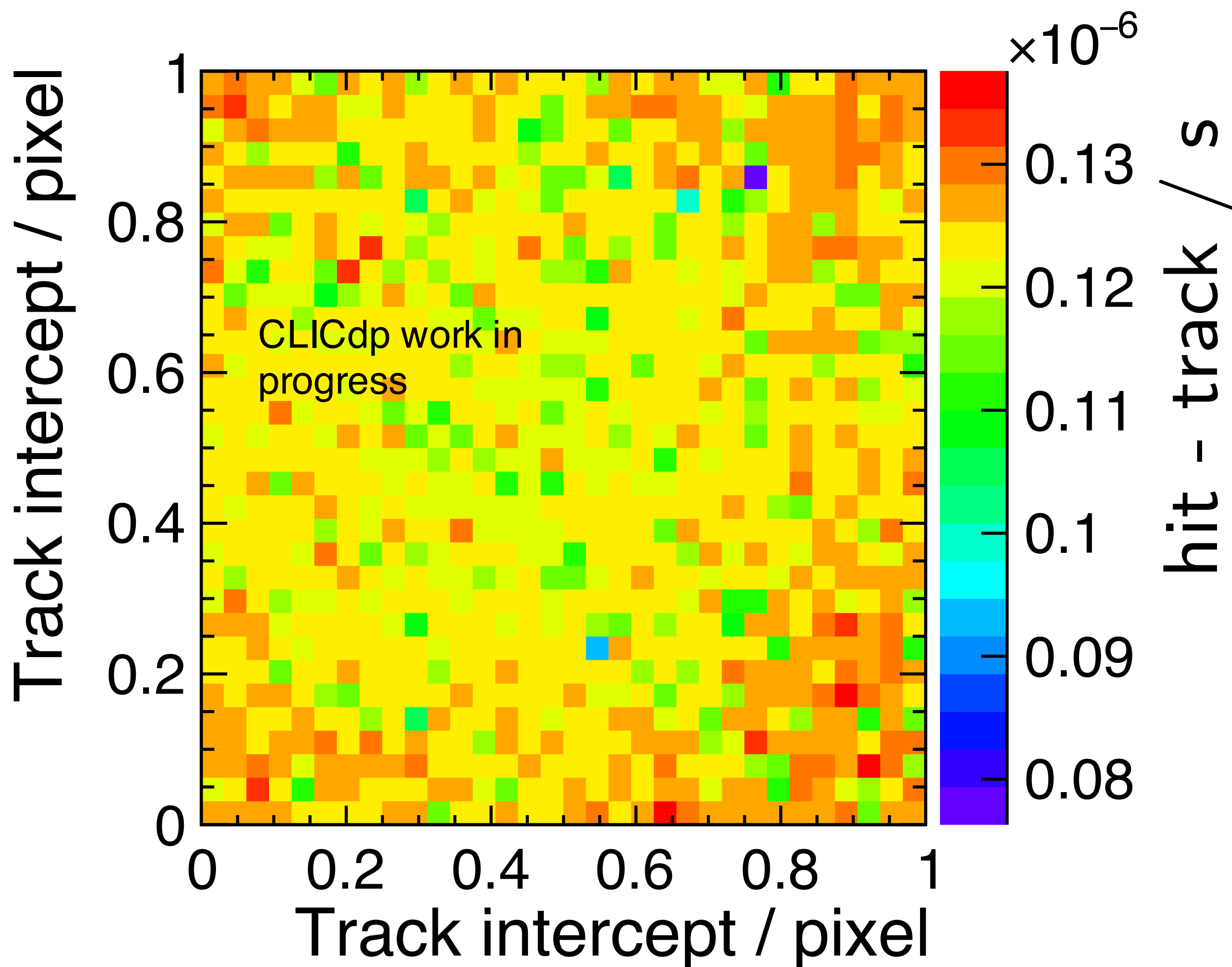


Uniformity of ToT response across the matrix



C3PD+CLICpix2 in-pixel timing

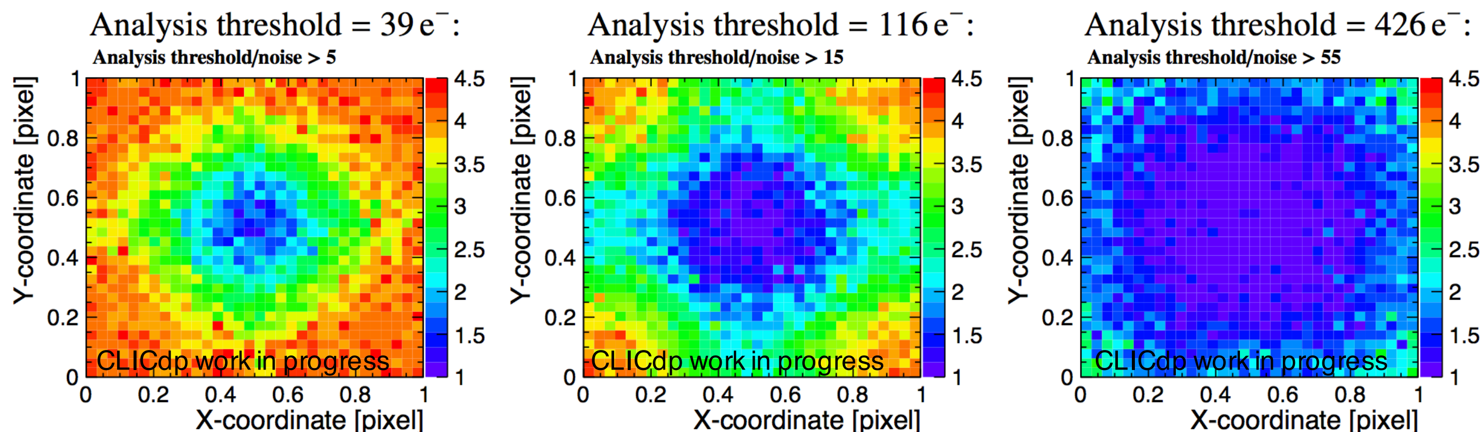
Mean reconstructed hit time vs. in-pixel position (before time-walk correction)



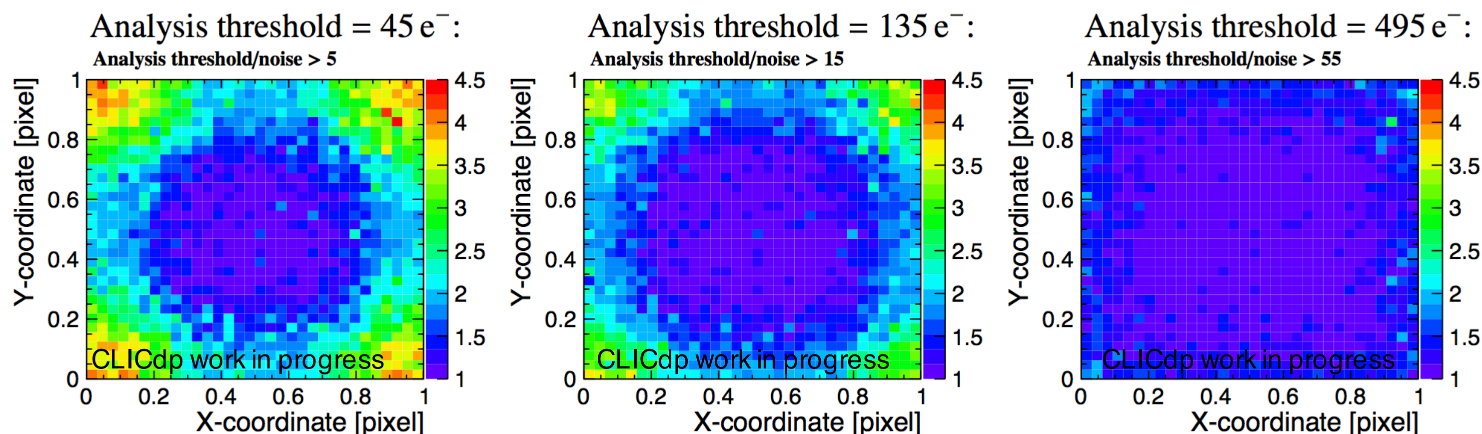
INVESTIGATOR charge sharing

Charge sharing studies (pitch of 28 µm, bias voltage of -6 V):

In-pixel cluster size at different thresholds for the standard process:

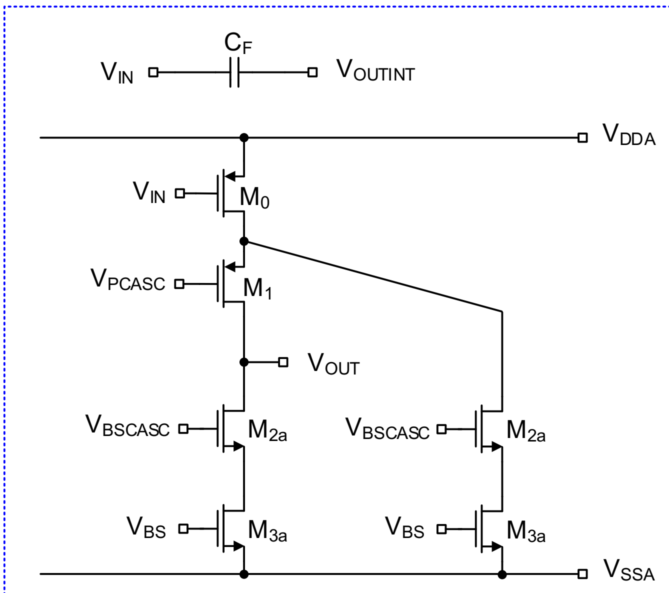


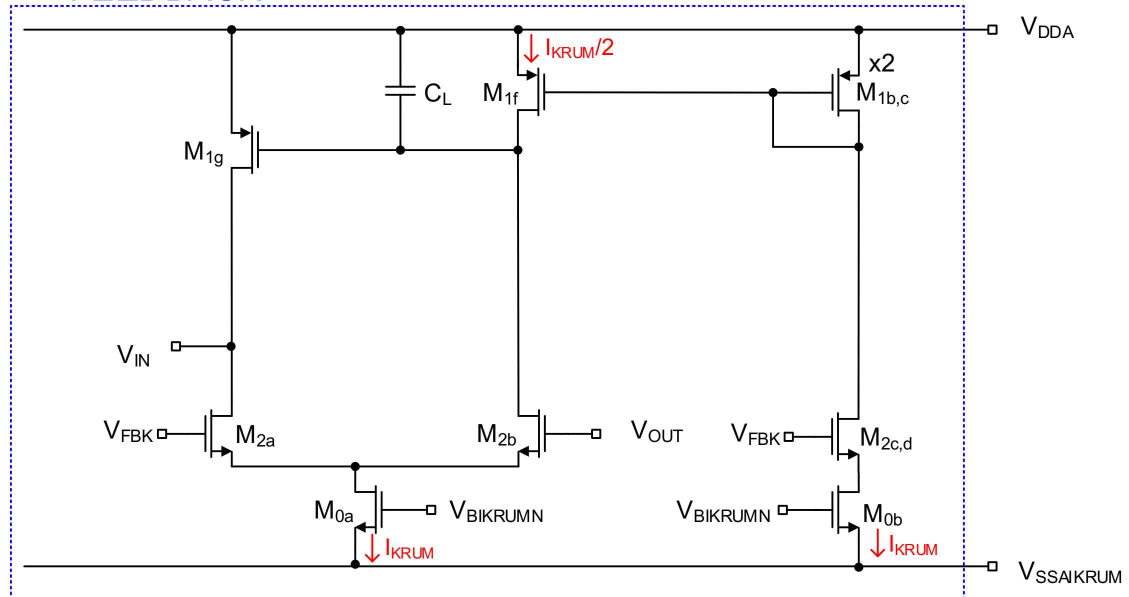
In-pixel cluster size at different thresholds for the modified process:



→ Significantly more charge sharing for standard process, as expected from diffusion.

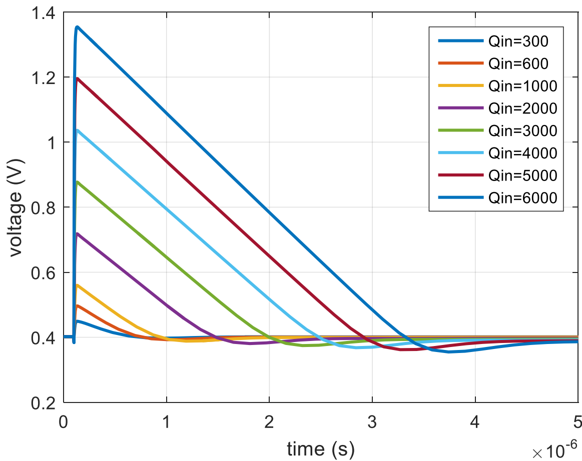
CLITD Charge sensitive amplifier

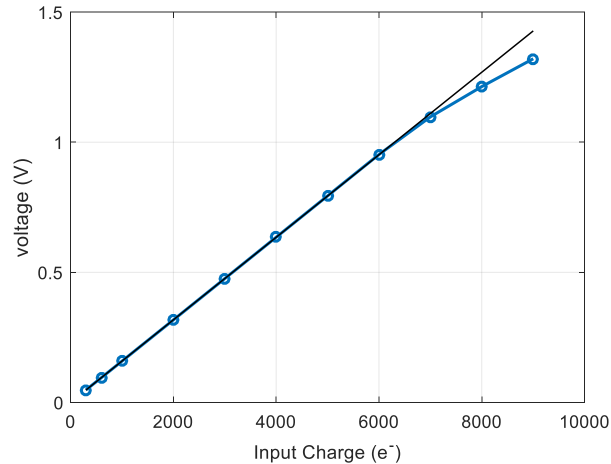


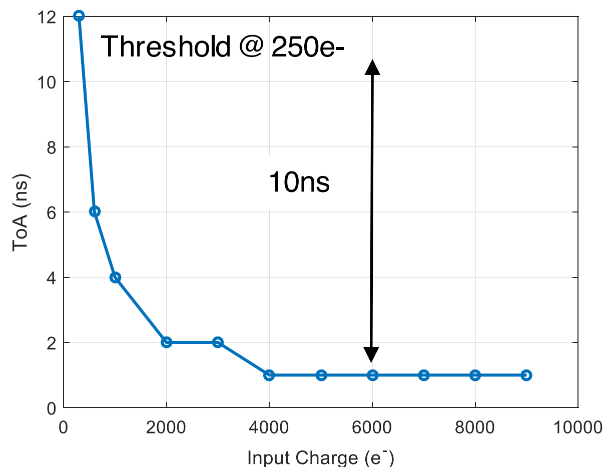


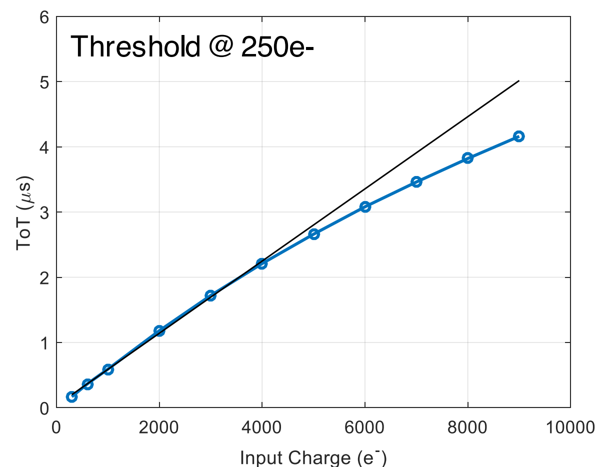
R. Ballabriga

CLICTD Charge sensitive amplifier









C_F=1fF (min value limited by the architecture)
C_D=2fF (detector and interconnections)

I_{PREAMP}=150nA (10mW/cm^2 (preamp only/30um pixels))

Gain=160mV/ke$^-$

Noise=35e$^-$ r.m.s

Unequalized threshold=70e$^-$ r.m.s.

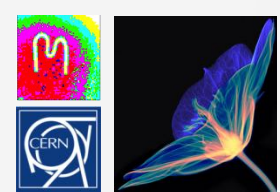
Equalized (3bits)=15e$^-$ r.m.s.

Minimum detectable charge=230e$^-$

Slope=16MV/s
(Jitter=noise/slope~0.4ns (@1ke$^-$))

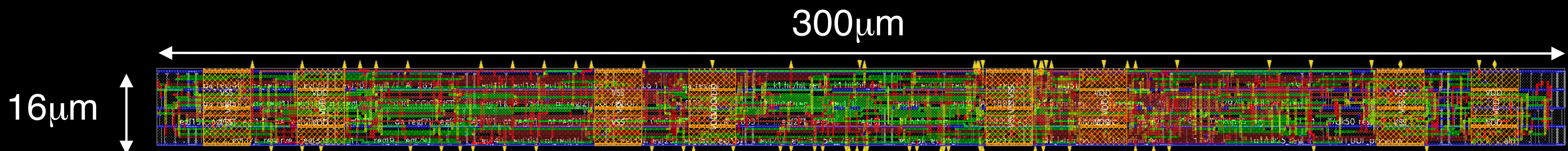
Comparator under study

R. Ballabriga

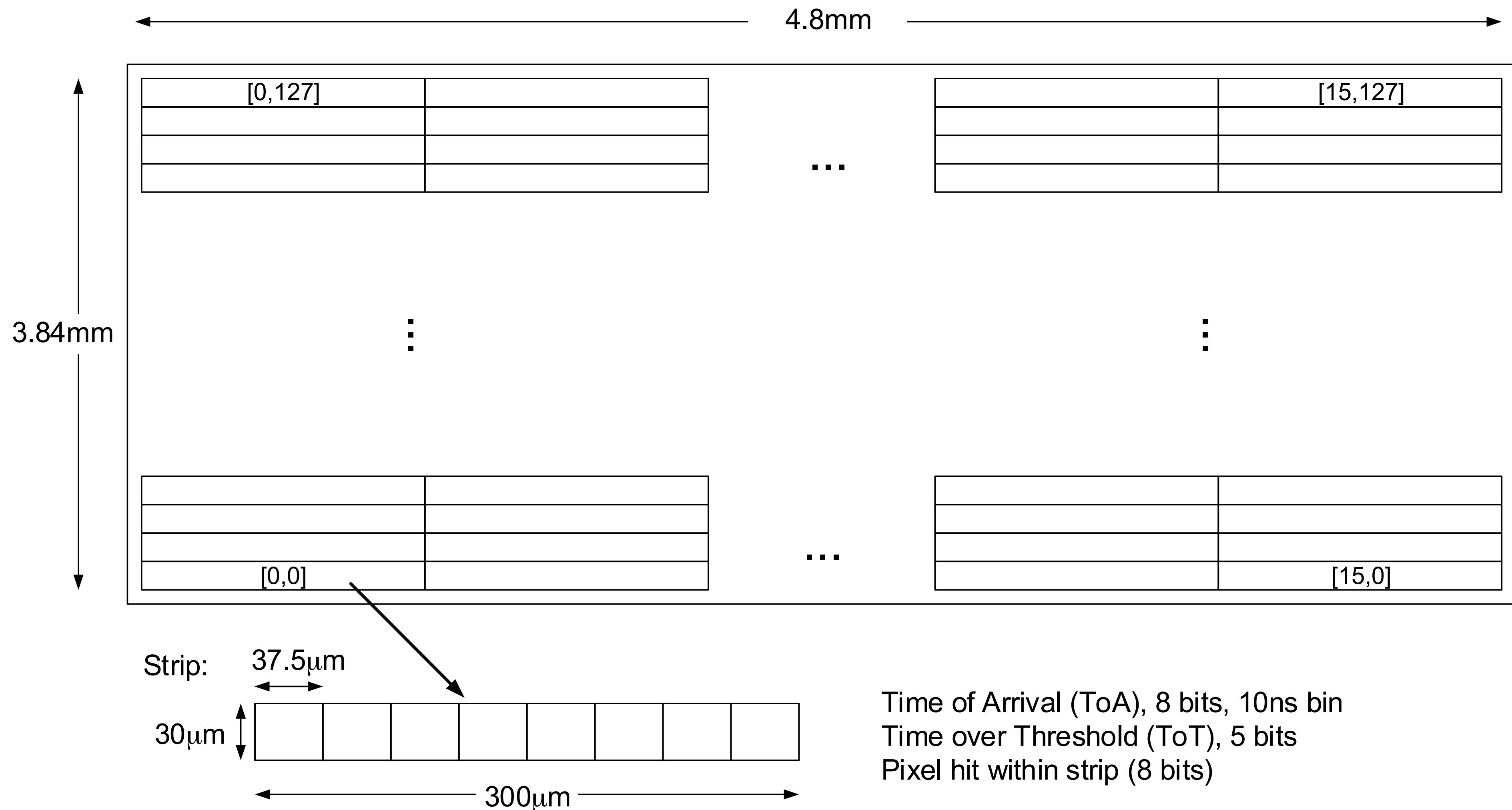


CLICTD Strip working modes

- Configuration
- Acquisition
  - 8 bits ToA, 5 bits ToT, individual hit information (8 bits)
    - ToT clock is generated by dividing the ToA clock (/2, /4, /8, /16 i.e. 50MHz, 25MHz, 12.5MHz or 6.25MHz)
  - 13 bits ToA, individual hit information (8 bits)
  - 13 bits hit counting (mainly for threshold equalization purposes)
- Readout
  - Zero compression is available



CLICTD Chip sensitive area

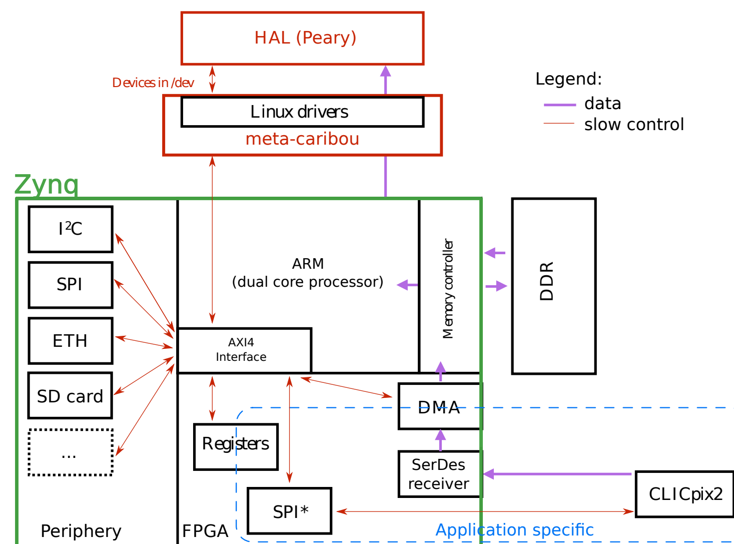


R. Ballabriga

Caribou multi-chip modular r/o system

- Caribou universal r/o system (BNL, UniGE, CERN)
- Target: laboratory and high-rate test-beam measurements
- Generic DAQ Software Peary
- Modular concept:
  - Xilinx FPGA evaluation board ZC706 with ARM Cortex-A9 processor
    → FPGA code reduced to minimum → System-on-Chip (SoC) runs full Linux stack and actual Peary DAQ software, easily customizable
  - Generic periphery board (CaR)
    → Stable voltages, various communication standards, ADCs for monitoring
  - Project specific chip boards:
    currently supporting CLICpix2, C3PD, FEI4, H35Demo, ATLASPIX
    → cheap, minimum functionality: routing, chip-specific buffers
- Open hardware / firmware / software:
  https://gitlab.cern.ch/Caribou/

CaRIBOu DAQ System schematics



CaRIBOu with CLICpix2 r/o ASIC