Ultra-thin Active Pixel Detector for the Belle II VXD

13th Trento Workshop on Advanced Silicon Radiation Detectors
Munich, February 19th – 21st 2018

C. Koffmane for the DEPFET collaboration

Outline

- DEPFET Collaboration
- SuperKEKB and BELLE II experiment
- DEPFET, PXD Module and control and read-out ASICs
- Assembly and Test
- PXD @ Phase 2 (Beast II)
- Summary and Outlook

DEPFET Collaboration

- Original Collaboration: DEPFET pixel detector @ ILC (since 2002)
- now: design, deliver and operate the PXD for Belle II

IHEP Beijing, China (Z.A. Liu)
Charles University, Prague, Czech Rep. (Z. Dolezal)
DESY Hamburg (C. Niebuhr)
University of Bonn (J. Dingfelder)
University of Hamburg (C. Hagner)
University of Heidelberg (P. Fischer)
University of Giessen (W. Kühn)
University of Göttingen (A. Frey)
University of Karlsruhe (T. Müller, I. Peric)
University of Mainz (C. Sfienti)
MPG Semiconductor Laboratory, Munich (J. Ninkovic)
Ludw.-Max.-University, Munich (T. Kuhr)
MPI for Physics, Munich (H.-G. Moser)
Technical University, Munich (S. Paul, A.Knoll)
Struct. Biol.Research Center, KEK (S. Wakatsuki)
IFJ PAN, Krakow, Poland (M. Rozanska)
University of Barcelona, Spain (A. Dieguez)
CNM, Barcelona, Spain (E. Cabruja)
IFCA Santander, Spain (I. Vila)
IFIC, Valencia, Spain (J. Fuster)
University of Tabuk, Saudi Arabia (R. Ayad)

DEPFET@Belle II

Management

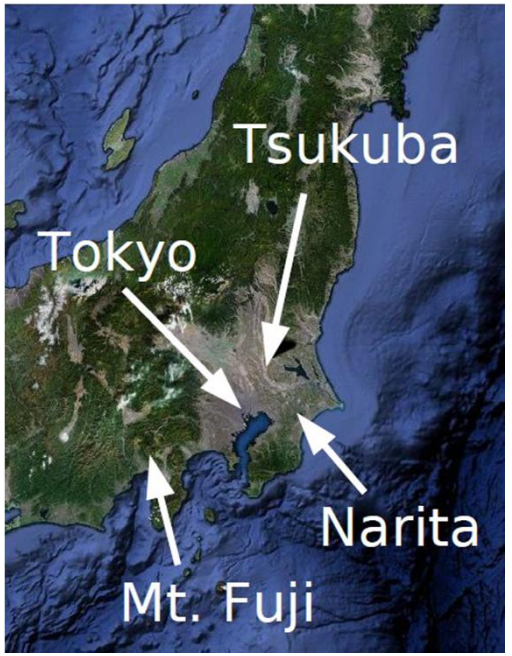
Project Leader
C. Niebuhr (DESY)

Technical Coord.
L. Andricek (HLL)

IB- Board
Chair: J. Dingfelder (Bonn)

Integration Coordinator
Shuji Tanaka (KEK)

KEKB – B-factory in Tsukuba, Japan

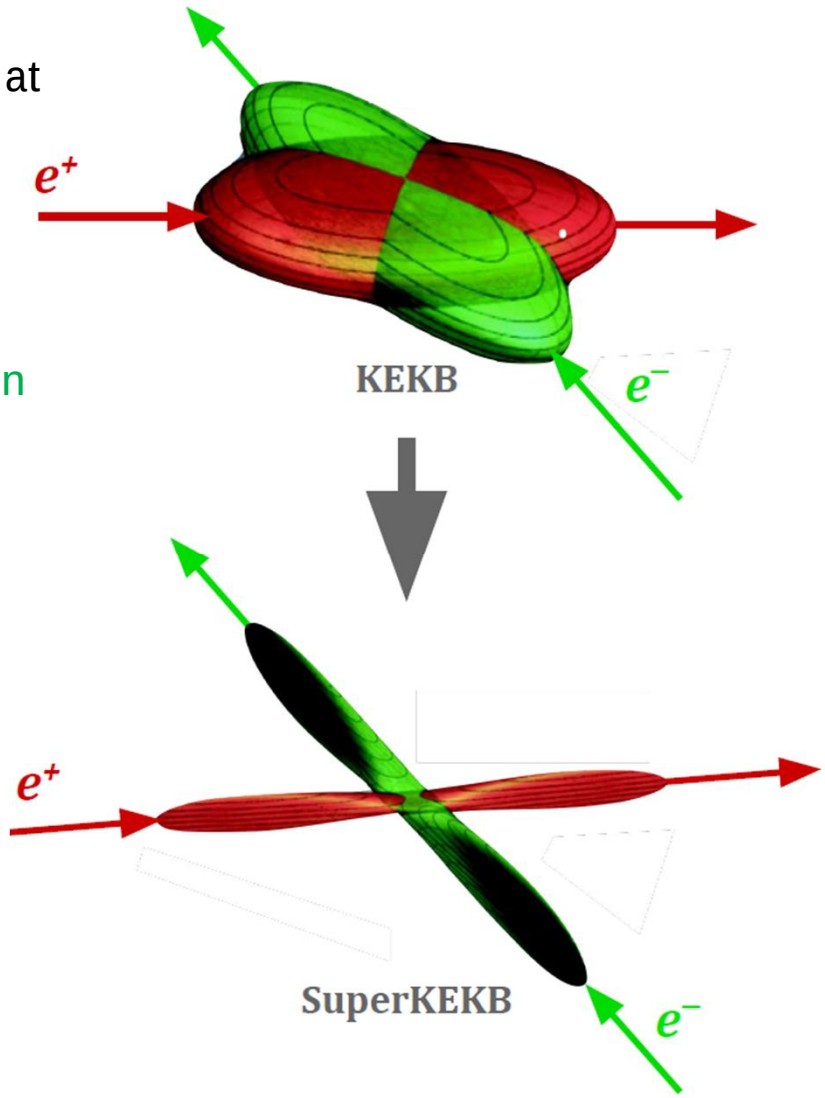


World record luminosity for e+e- colliders: 2.1 x 10^{35} cm^{-2} s^{-1}

SuperKEKB and the BELLE II experiment

- Asymmetric energy (4 GeV, 7 GeV) e+e- collider at the E_{cm} = 10.57 GeV
- Instantaneous luminosity: 8 x 10^{35} cm^{-2} s^{-1} [40 times KEKB]
- Integrated luminosity: 50 ab^{-1} [50 times KEKB]
  - Nano-beam scheme (positron and electron bunch crossing)
  - Doubled beam currents
- First collisions this summer! Exciting times!

Beam parameters		KEKB		SuperKEKB		units
		LER	HER	LER	HER	
Beam energy	E_b	3.5	8	4	7	GeV
Vertical beam size	d_V	0.94	0.94	0.048	0.056	µm
Horizontal beam size	d_H	150	150	10	11	µm
Beam currents	I_b	1.64	1.19	3.60	2.60	A
Luminosity	**L**	**2.1×10^{34}**		**8×10^{35}**		**$cm^{-2}s^{-1}$**



Requirements for the Belle II detector

Higher background (x10-20 compared to Belle)

- à Radiation damage and occupancy
- à Fake hits

§ Higher event rate

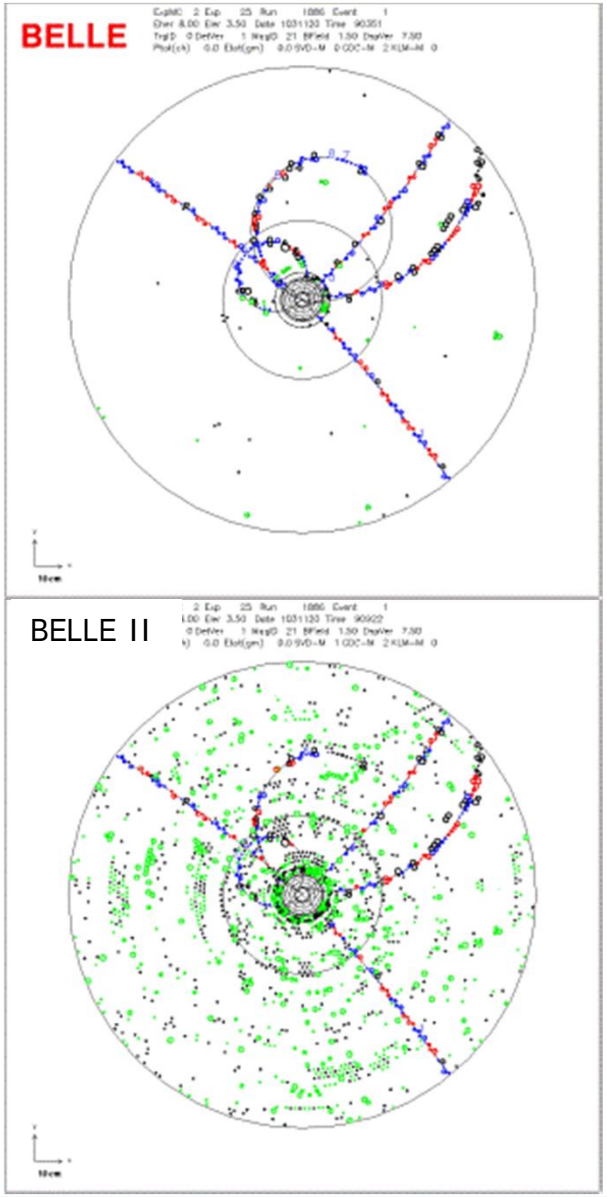
- à Higher trigger rate (0.5 kHz → 20-30 kHz)

§ The physical goals require a vertex detector with unprecedented performance (~10 µm)

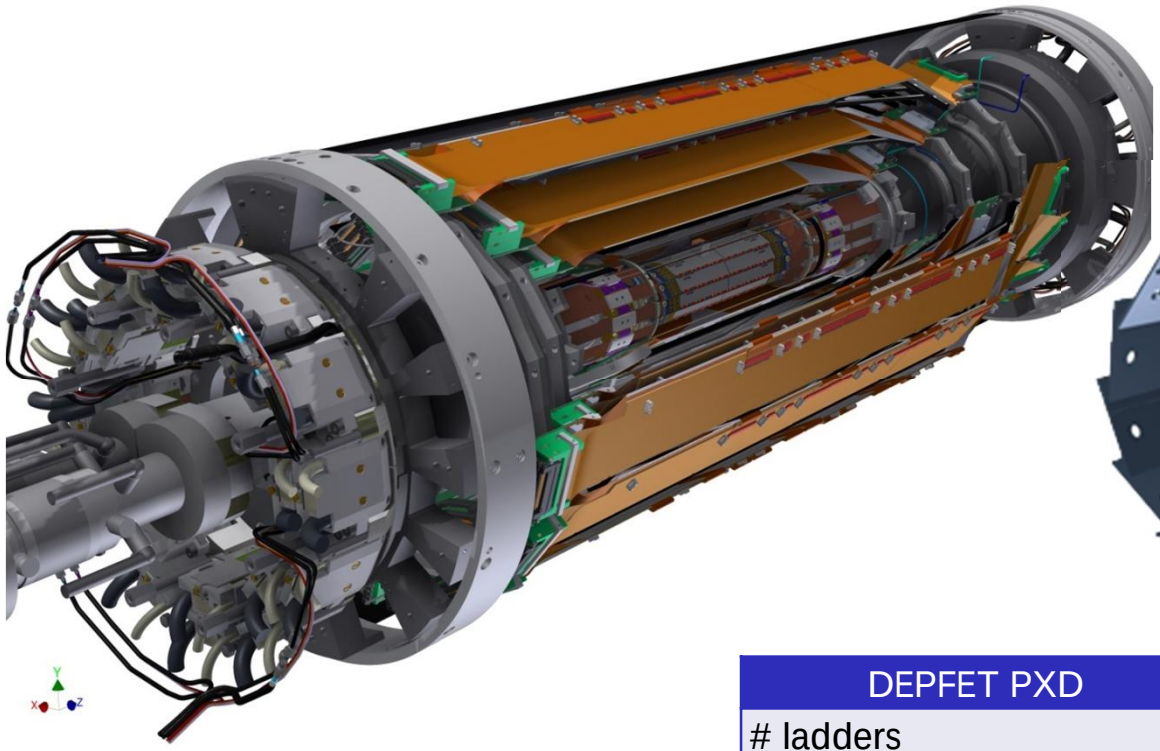
- à low material budget (<0.2 X0 per layer)
- à high granularity pixel detector

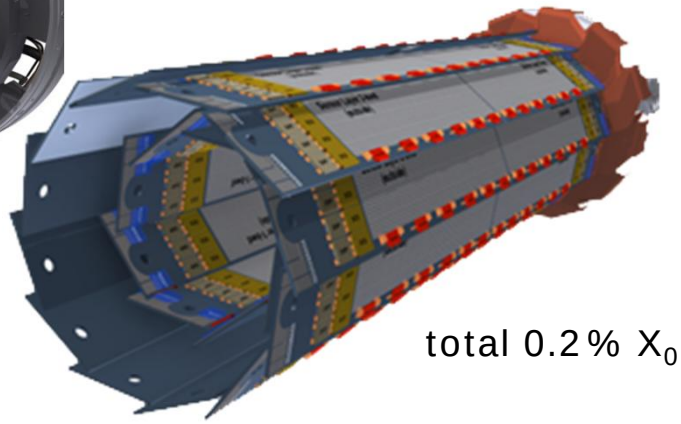
§ New vertex detector

- § 2 layers of pixels based on DEPFET technology, sensor thinned down to 75 µm
- § 4-layers of double-sided silicon strips



The BELLE II Vertex Detector



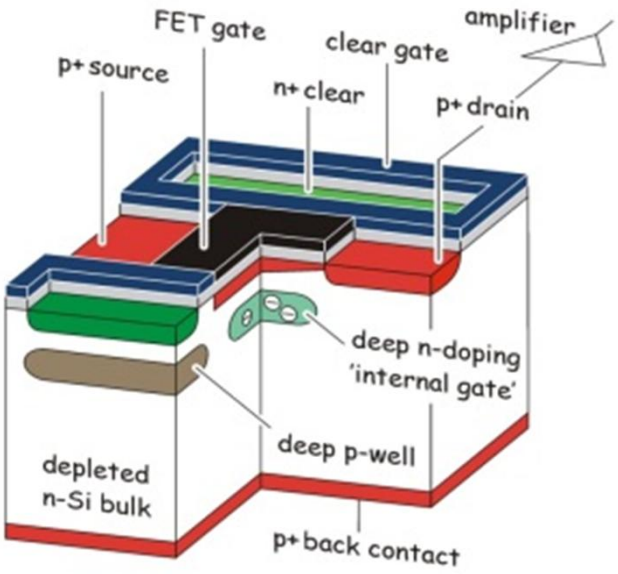


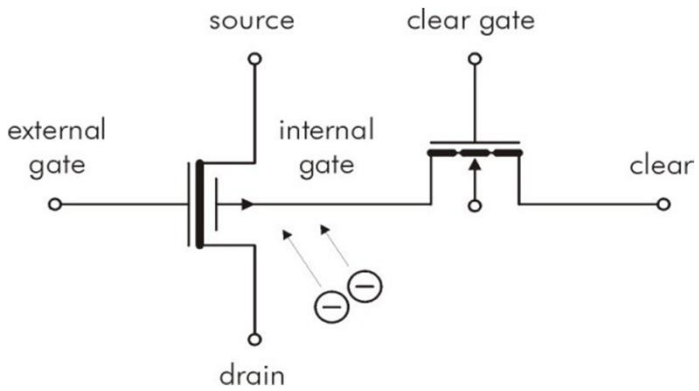
total 0.2 % X_0

- 2 DEPFET layers (PXD)
- 4 Double Sided Si-Strip Detector layers (SVD)

DEPFET PXD	L1	L2
# ladders	8	12
Distance from IP (cm)	1.4	2.2
Sensitive thickness (µm)	75	75
#pixels/module	768x250	768x250
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (μm^2)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Total sensitive Area (cm^2)	89.6	176.9

DEPFET Working Principle

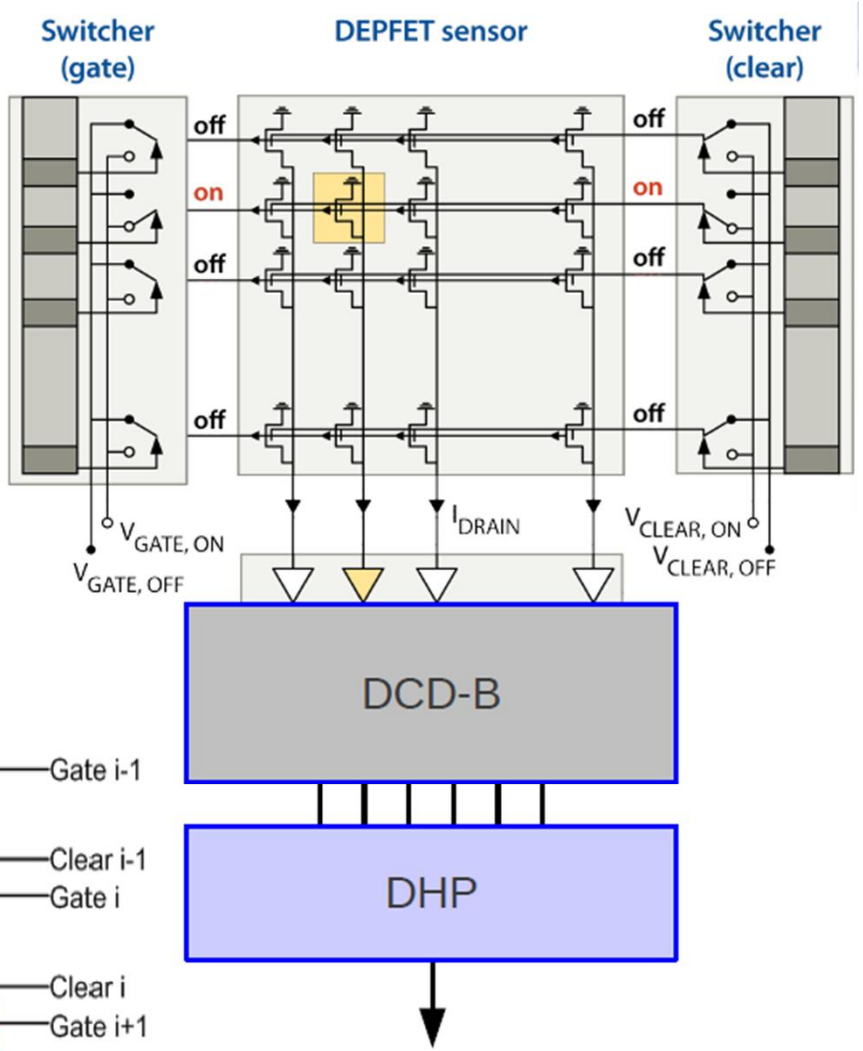


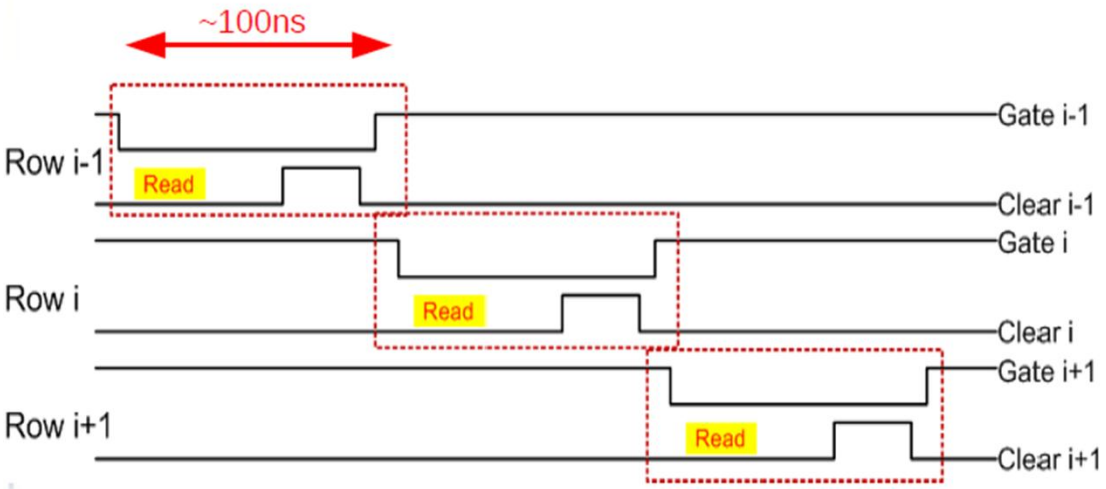


- fully depleted sensitive volume
  - fast signal rise time (~ns), small cluster size
- In-house fabrication at MPS Semiconductor Lab
  - Wafer scale devices possible
  - Thinning to (almost) any desired thickness
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- Charge collection in "off" state, read out on demand
  - potentially low power device
- internal amplification
  - charge-to-current conversion
  - r/o cap. independent of sensor thickness
  - Good S/N for thin devices

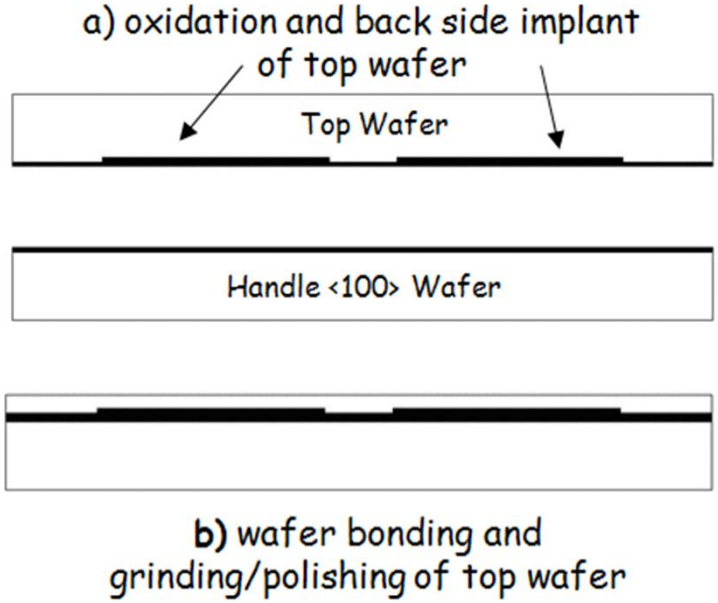
DEPFET Read-out Sequence

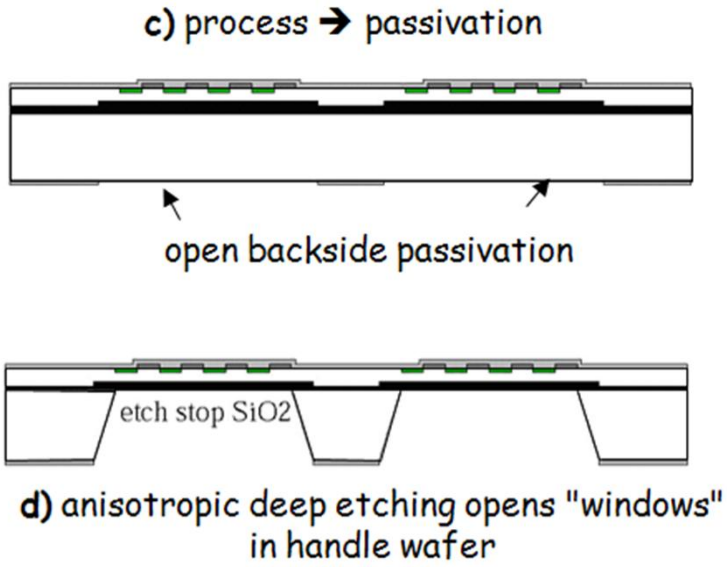
- Row wise readout (Rolling Shutter)
- The SWITCHER chip generates the control signals for the rows GATE and CLEAR
- Readout chip processes all columns in parallel
- DEPFET readout sequence (single sampling):
  1. select row with external gate
  2. readout transistor current
  3. clear charge from internal gate
  4. select next row



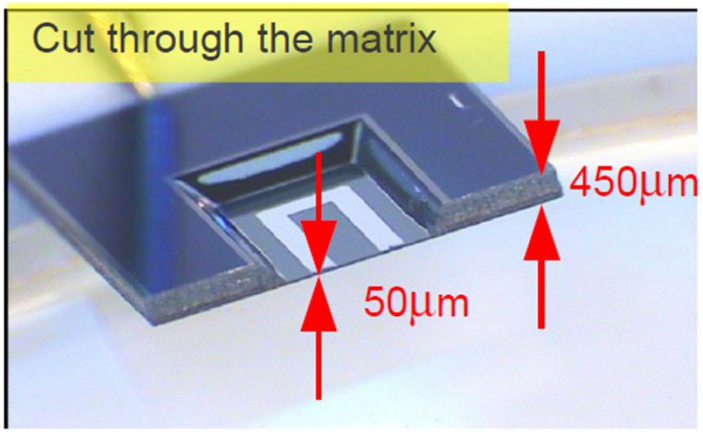


Self-supporting All-Silicon Module



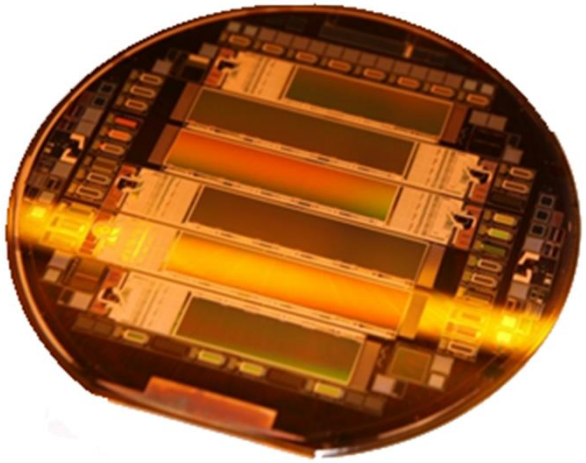


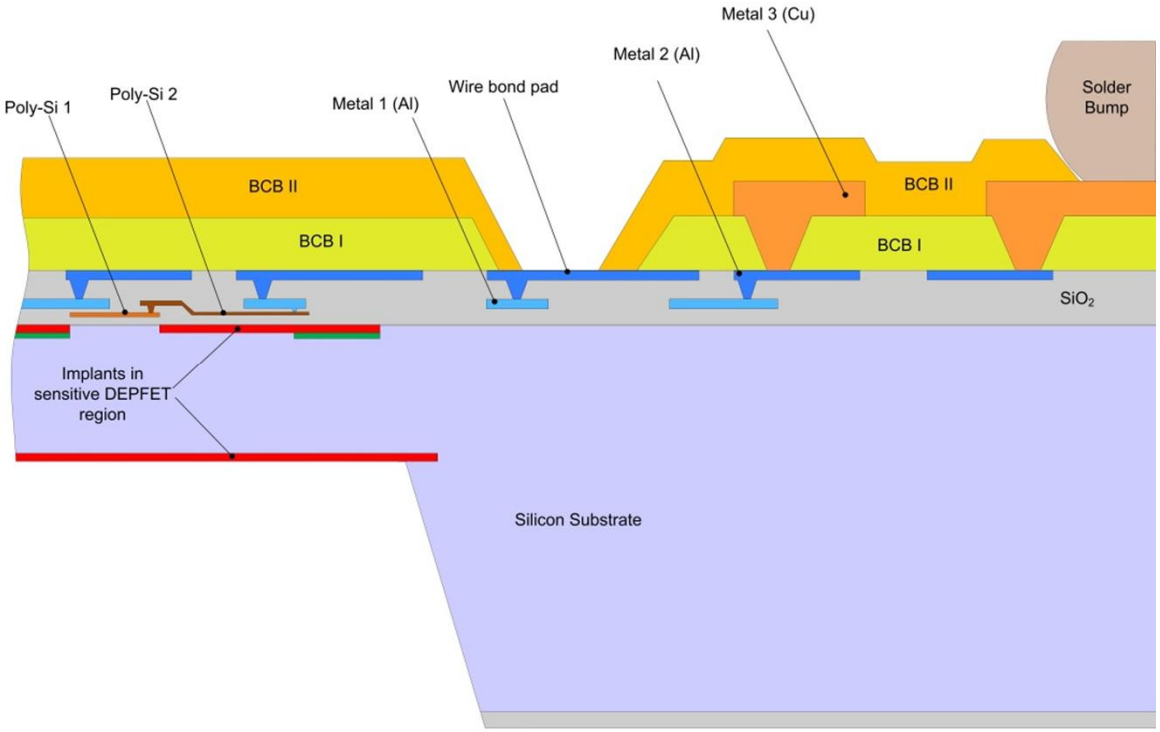
- DEPFET thickness is a free parameter, adjustable to the needs of the experiment
- Key Process Modules:
  - Wafer bonding and thinning of the top layer
  - Sensor fabrication on SOI
  - Etching of the handle wafer
- Modules are supported by monolithic silicon frame
- Two modules are assembled to one ladder

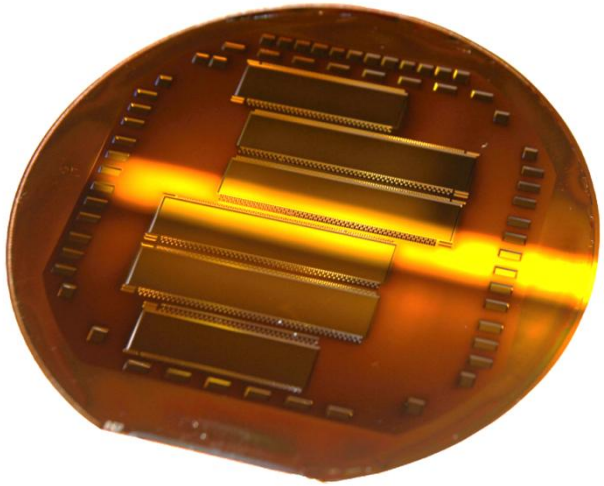


In-house MPG HLL DEPFET Sensor Production

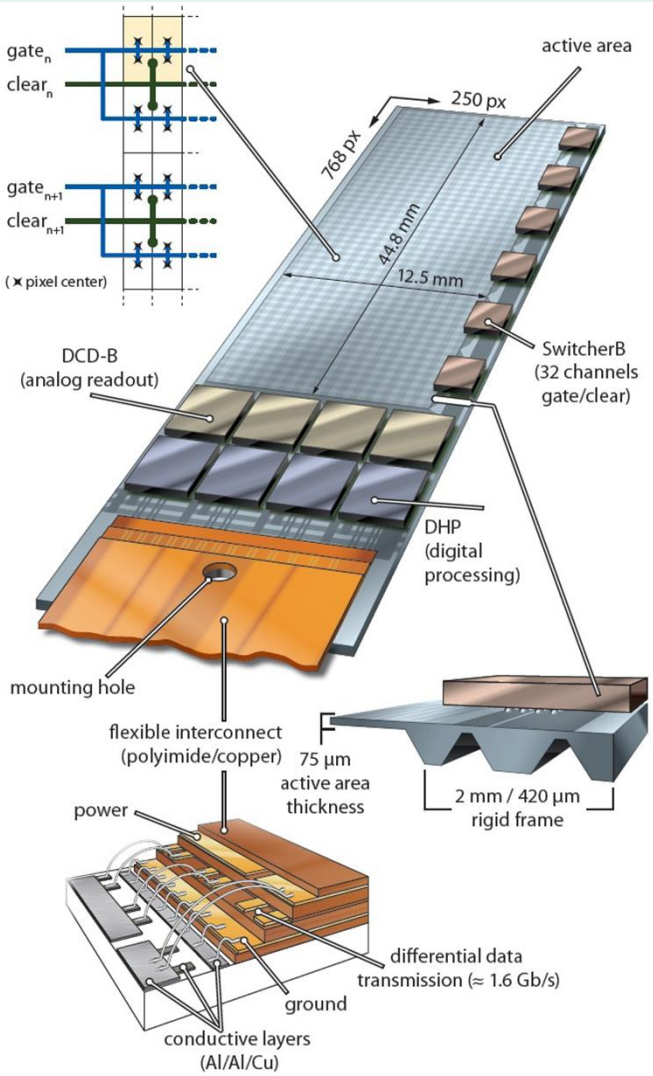
- Starting material SOI wafer: 75µm top, 450µm support
- Production in three phases, 19 lithography steps
  - 9 implantations, 2 poly-silicon layers
  - 9 2 aluminum layers
  - 9 last metal copper and thinning of sensitive area





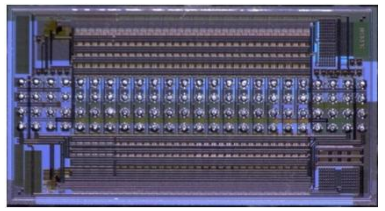


PXD Module



SwitcherB, DCDB: KIT
DHP: Barcelona U., Bonn U.

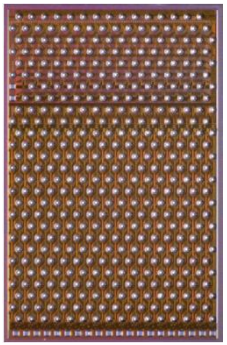
SwitcherB - Row Control



- AMS/IBM HVCMOS 180 nm
- Size 3.6 ´ 1.5 mm^2
- Gate and Clear signal
- Fast HV ramp for Clear
- Rad. hard proved (36 Mrad)

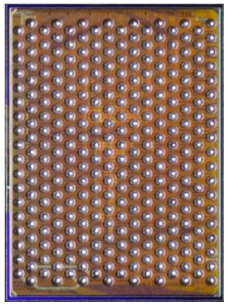
DCDB - Drain Current Digitizer

Amplification and digitization of DEPFET signals.



- UMC 180 nm
- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- Rad. hard proved (10 Mrad)

DHP - Data Handling Processor



- TSMC 65 nm
- Size 4.0 ´ 3.2 mm^2
- Stores raw data and pedestals
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)

Module Assembly and Testing

Flip Chip of ASICs (~240°C) at IZM, Berlin

- Bumped ASICs have the same solder balls (SAC305 and AgSN)
  - DHP bumping at TSMC, DCDB bumping via Europractice
  - SWB bumping on chip level at IZM Berlin

SMD placement (~200°C) at HLL, Munich

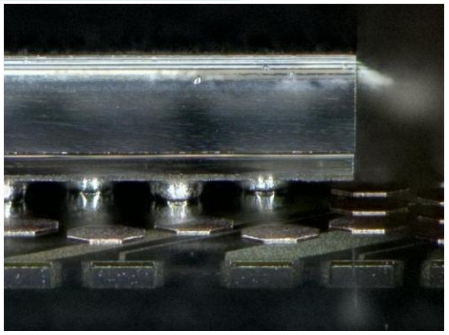
- Passive components (termination resistors, decoupling caps)
- Dispense solder paste, pick, place and reflow
- Module test on probe station

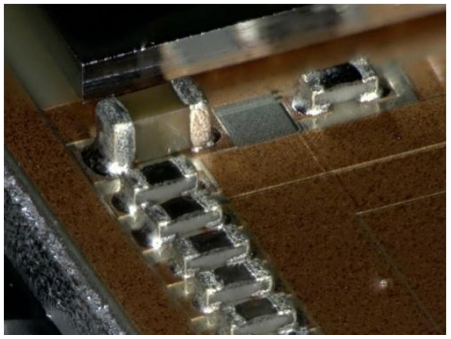
Kapton attachment (~170°C), wire bonding at MPP, Munich

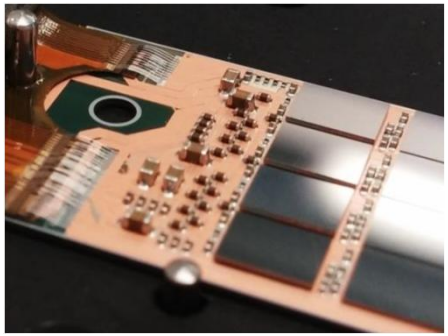
- 4-layer rigid-flex PCB with SMD, ~40cm long
- Solder paste printing on kapton, soldering
- Wire-bond, wedge-wedge, 32 µm Al bond wires
- Module characterization

Ladder gluing at MPP, Munich

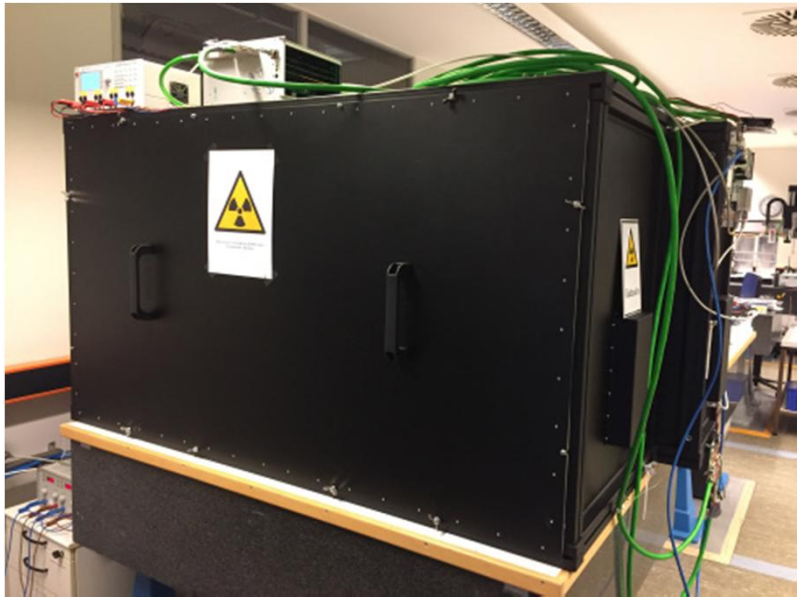
- Dispense adhesive, align two modules and join them together
- Ladder tests (basic verification of the functionality)

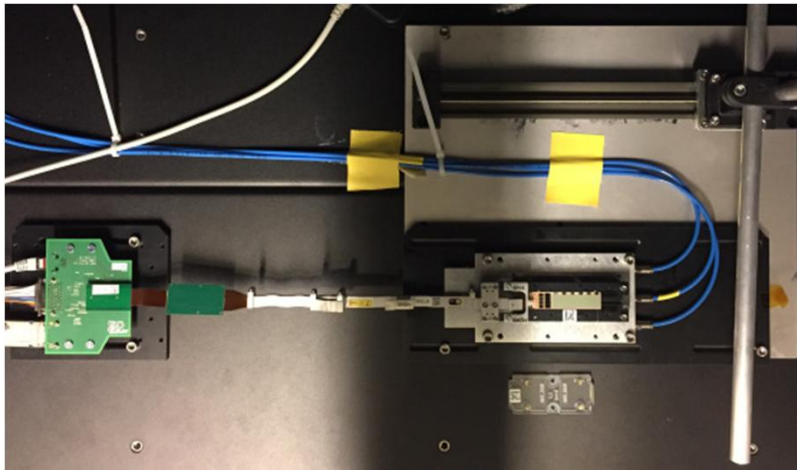




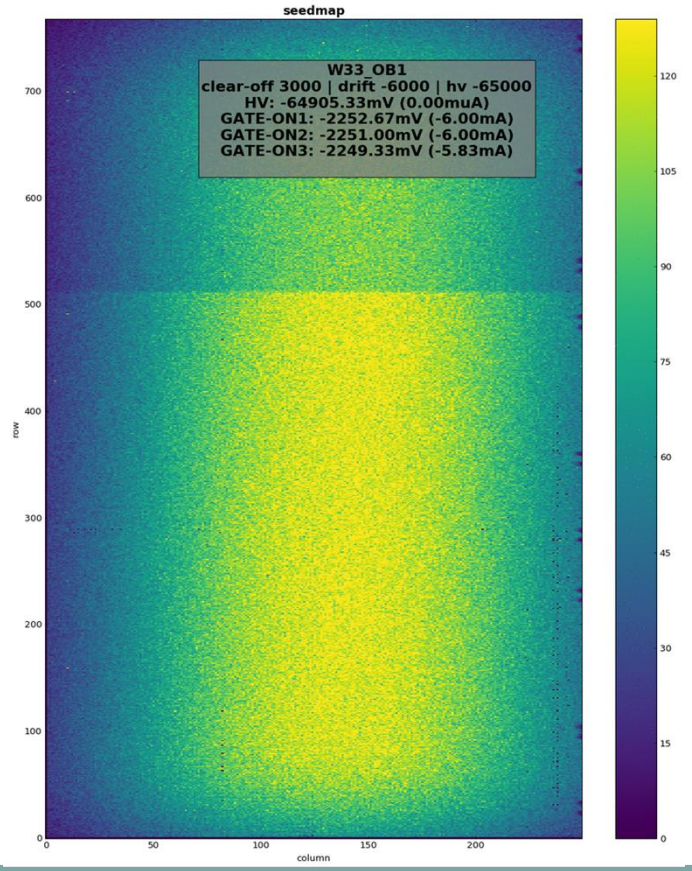


Module Assembly and Testing – Setups and Procedure





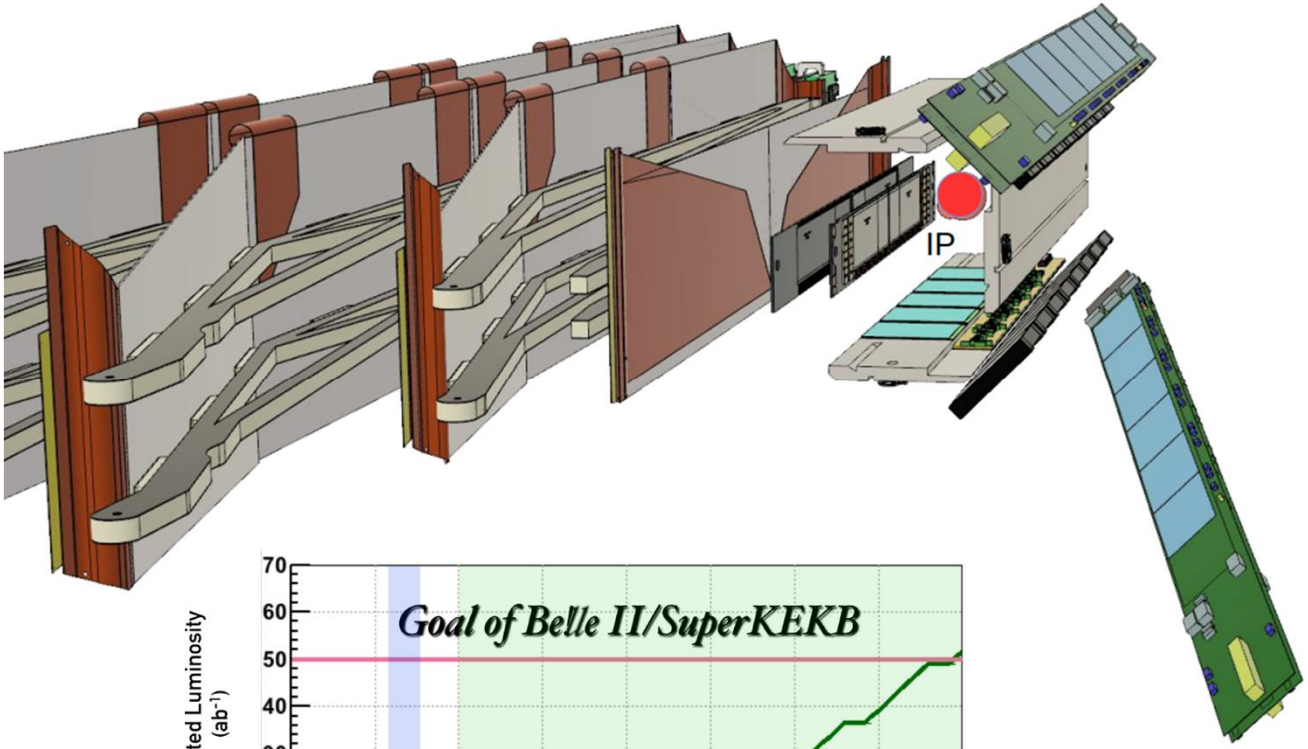
- 7 test setups at MPP, Göttingen, Bonn and HLL
  - script based, automated procedure
  - Optimize ASIC and DEPFET parameters (source scan)

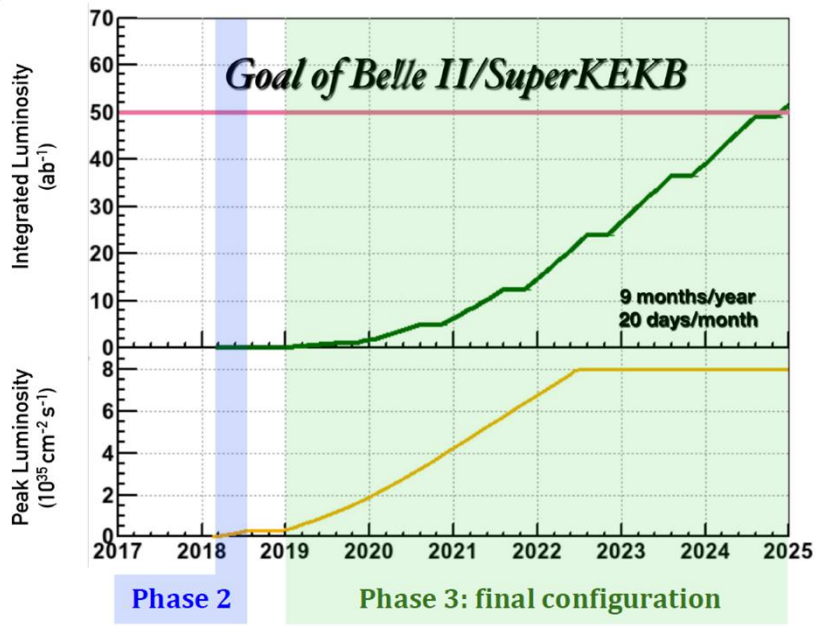


Assembly and Testing

- 12 x IB + 12 x IF modules for L1 tested (8+8 needed)
  - 1 x IB failed due to short on kapton, repair ongoing
  - 3 x IF failed, W05_IF Drain/Source short matrix, W08_IF SWB4 noisy gates, W43_IF DCDB damaged during handling, repair ongoing
- 18 x OB + 18 x OF modules for L2 prepared and currently under test (12+12 needed)
  - 4 OF modules failed at the probe card test before the kapton assembly, exchange of ASICs in preparation
  - ~50% of the modules (7 OB, 8OF) with kapton tested and pass
- Module testing expected to take till end of March
- Ladder Assembly is ongoing (8 x L1, 1 x L2)

Phase 2 Operation and VXD Setup

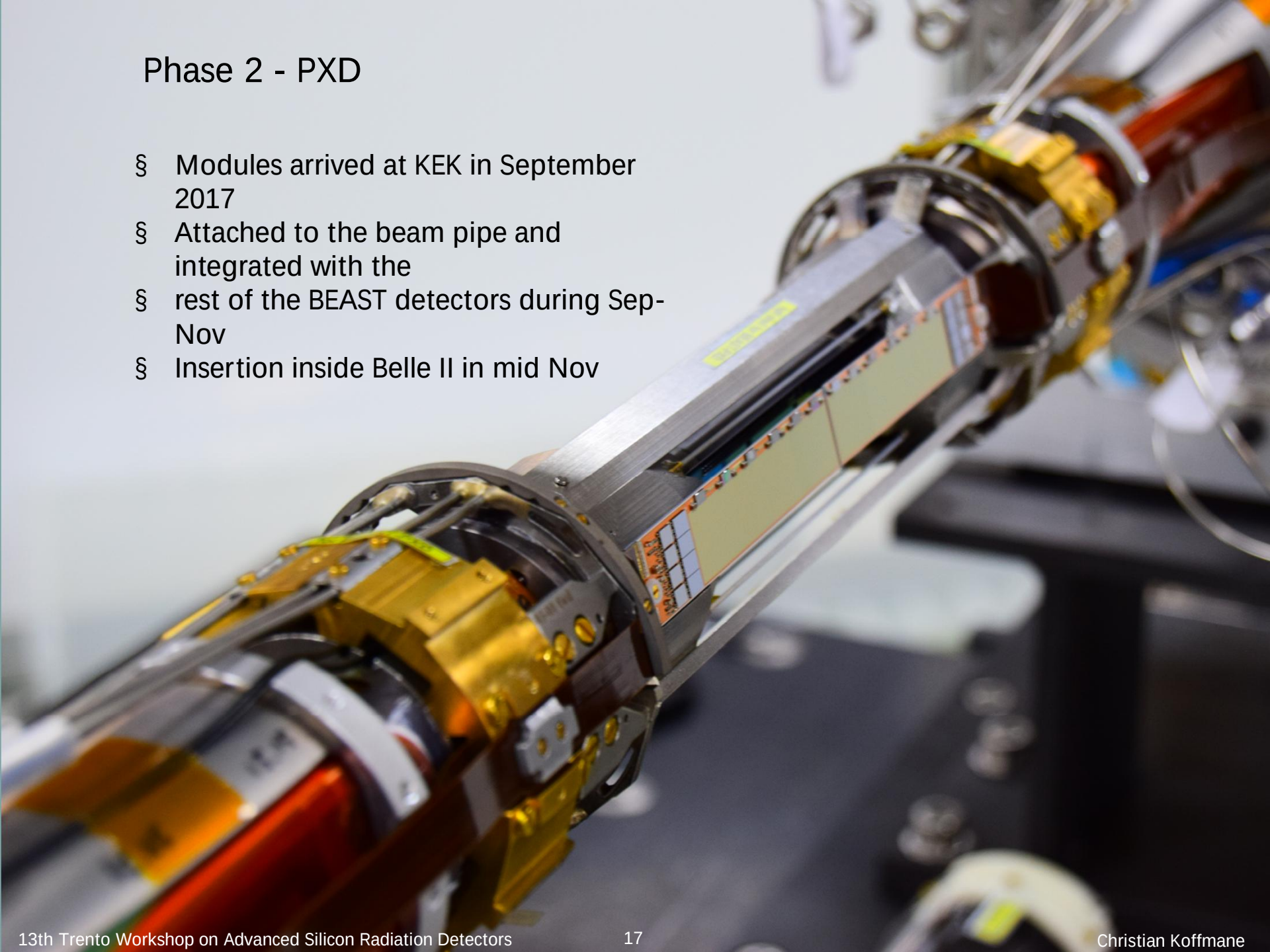




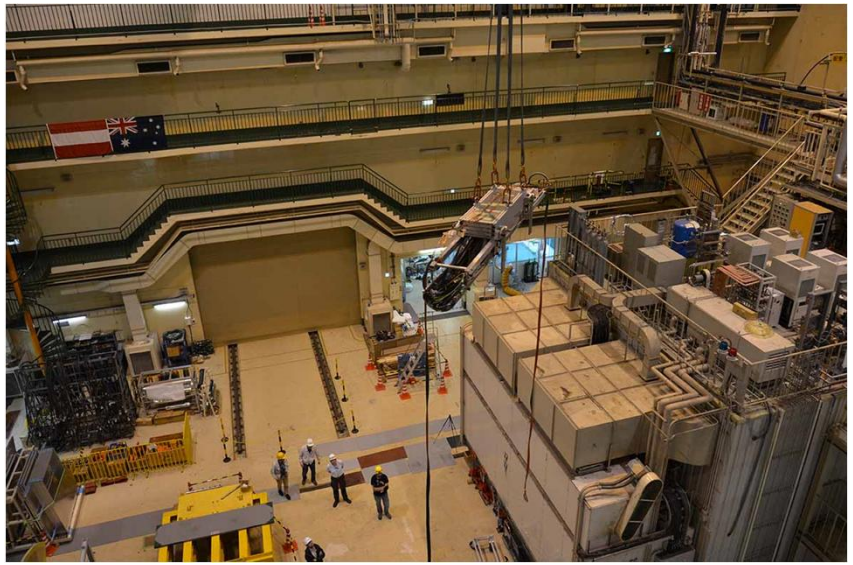
- Machine commissioning and radiation safe environment for the VXD
- 2 PXD ladders and four SVD layers in +X direction
- Rest of the VXD volume contains several radiation detectors for Phase 2 background investigations

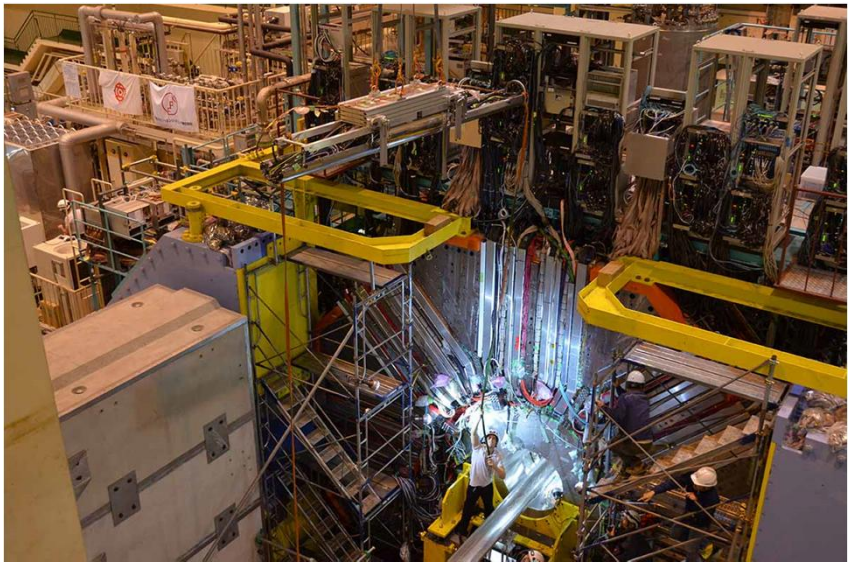
Phase 2 - PXD

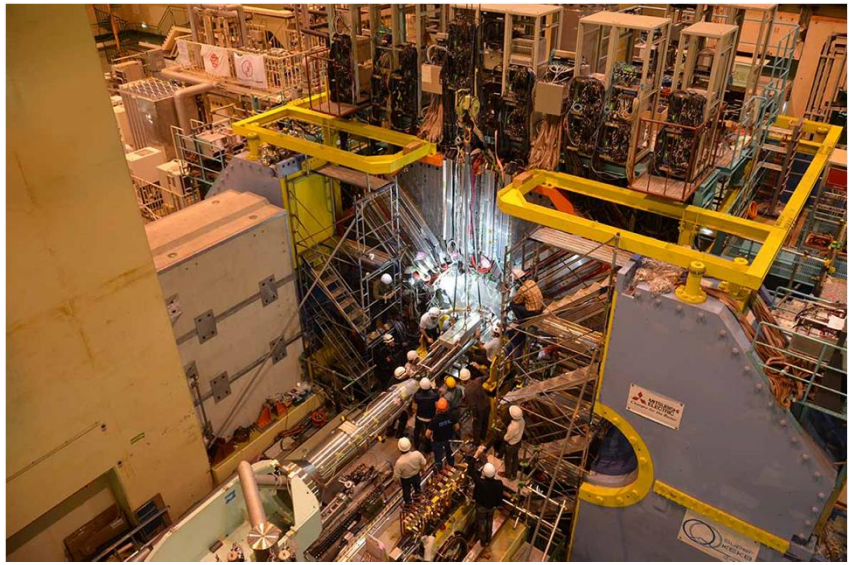
- Modules arrived at KEK in September 2017
- Attached to the beam pipe and integrated with the
- rest of the BEAST detectors during Sep-Nov
- Insertion inside Belle II in mid Nov



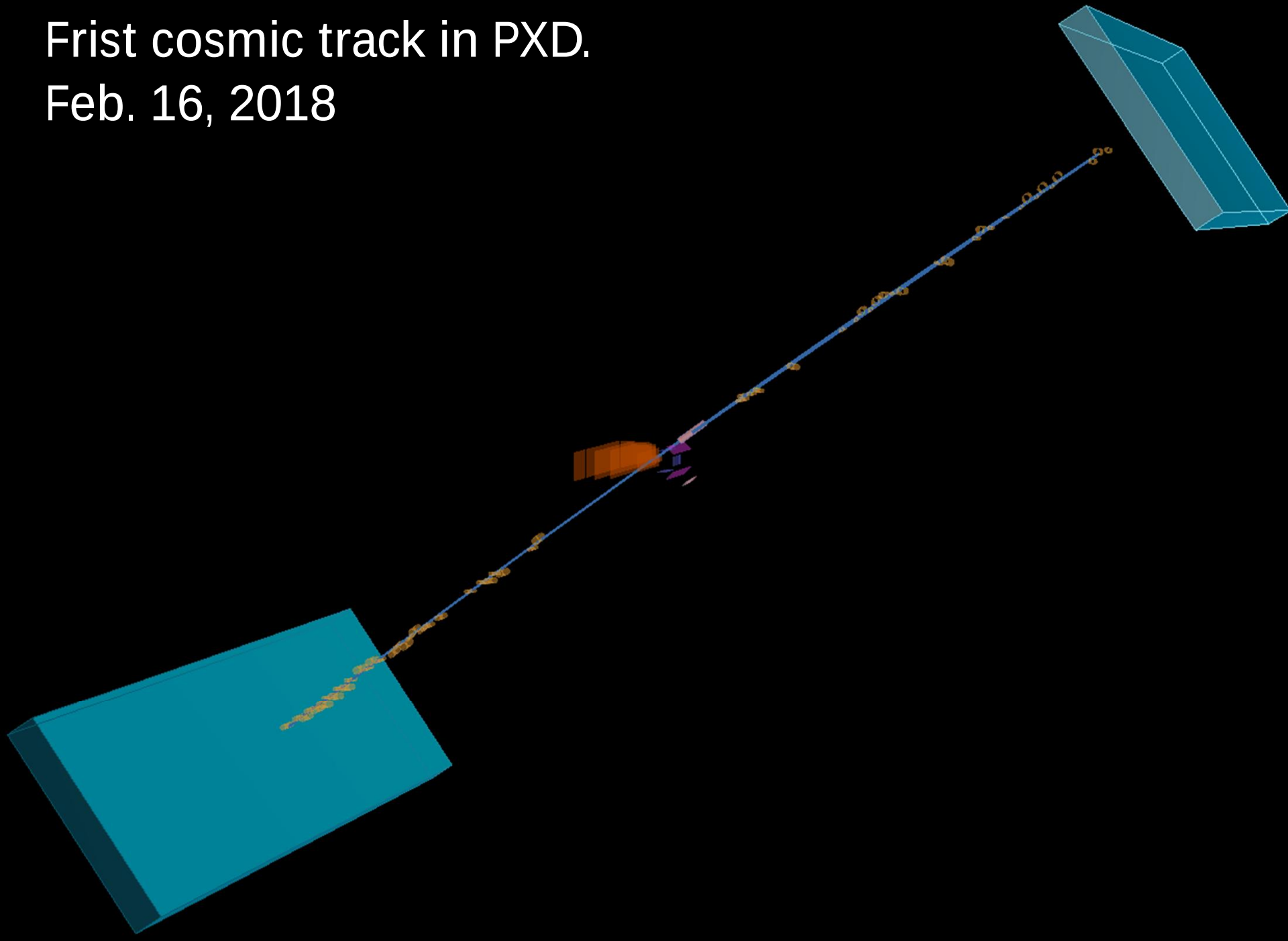
Transportation



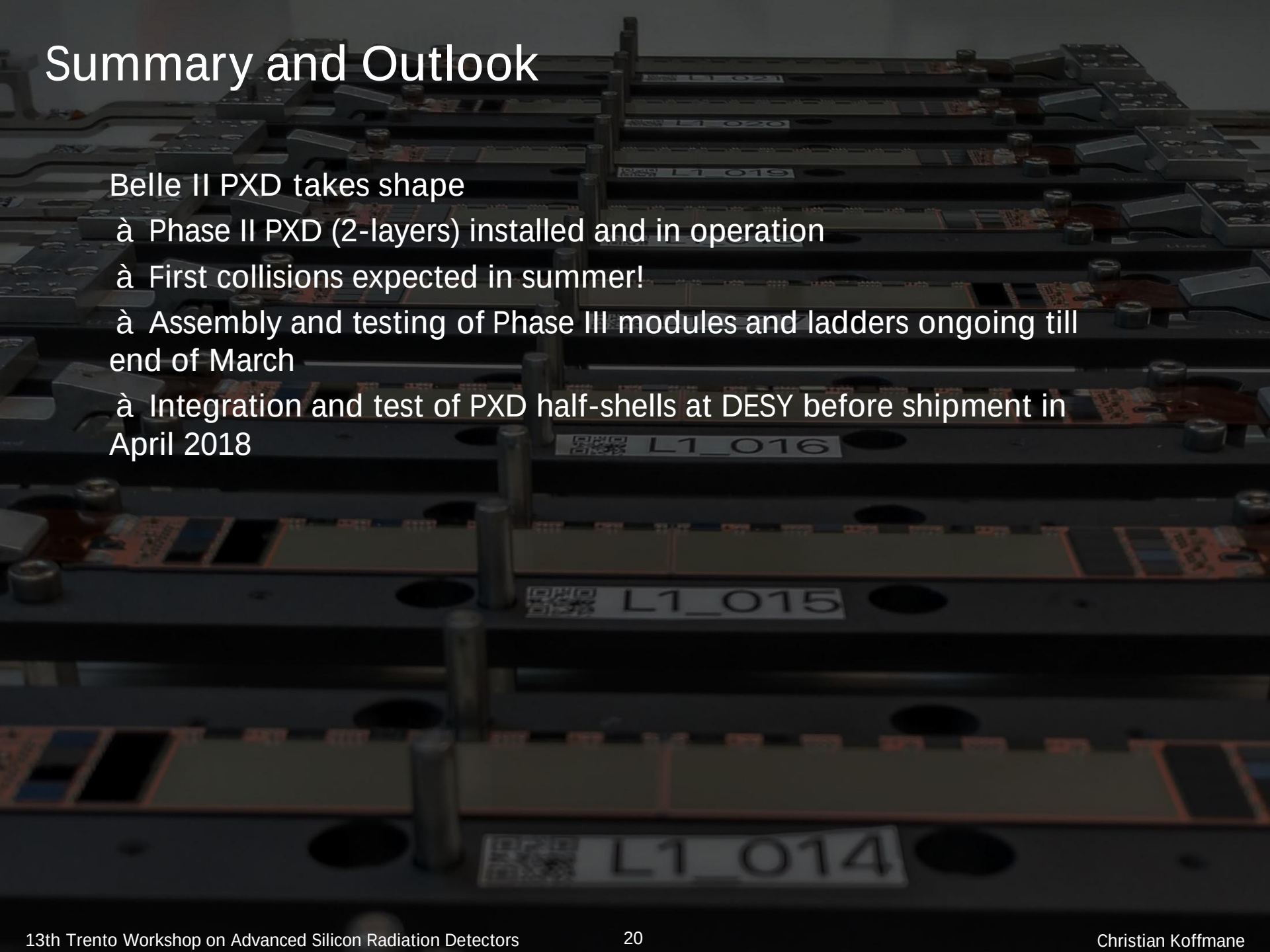




Frist cosmic track in PXD.
Feb. 16, 2018



Summary and Outlook

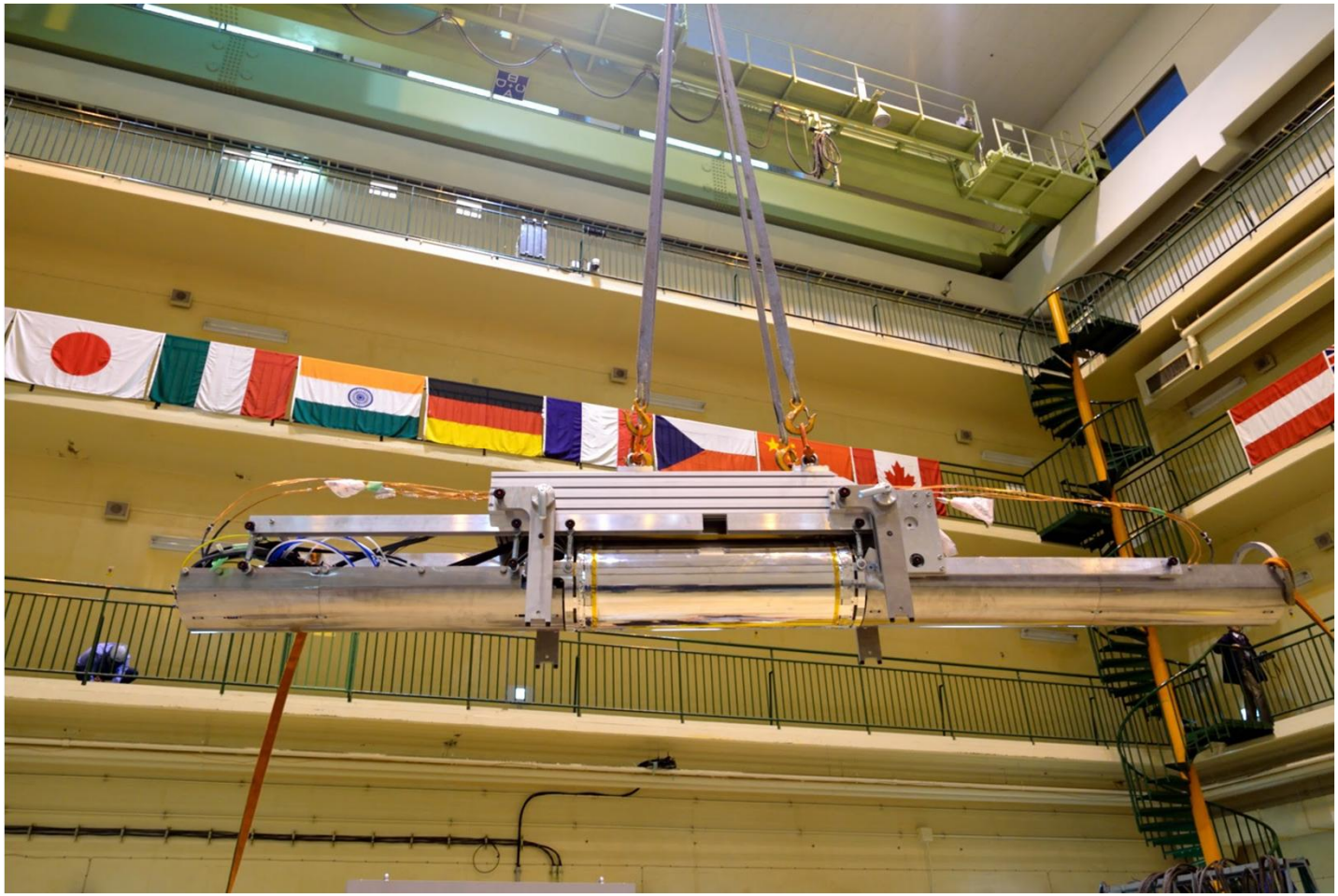


Belle II PXD takes shape

- à Phase II PXD (2-layers) installed and in operation
- à First collisions expected in summer!
- à Assembly and testing of Phase III modules and ladders ongoing till end of March
- à Integration and test of PXD half-shells at DESY before shipment in April 2018

Thank you

Transportation



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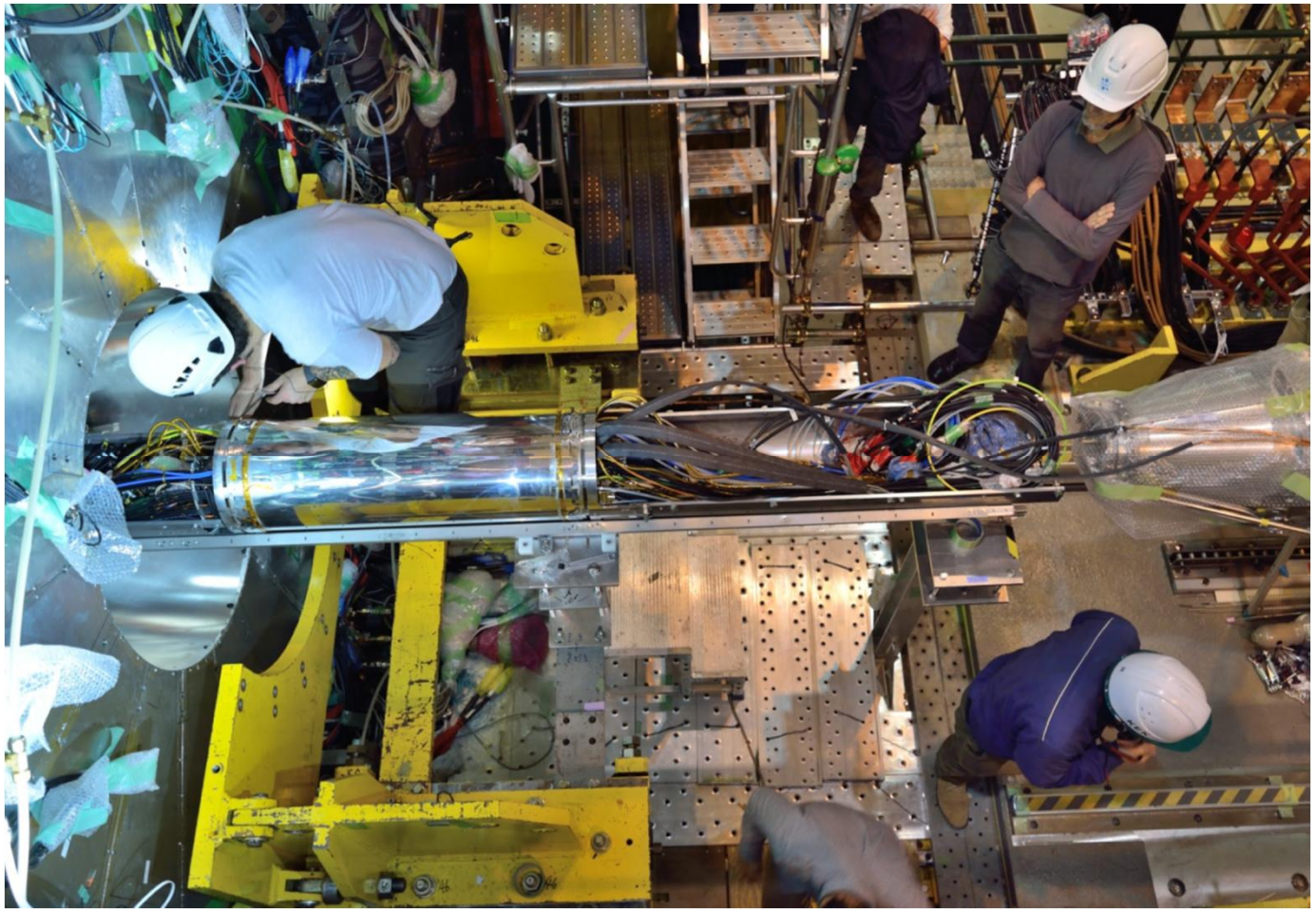
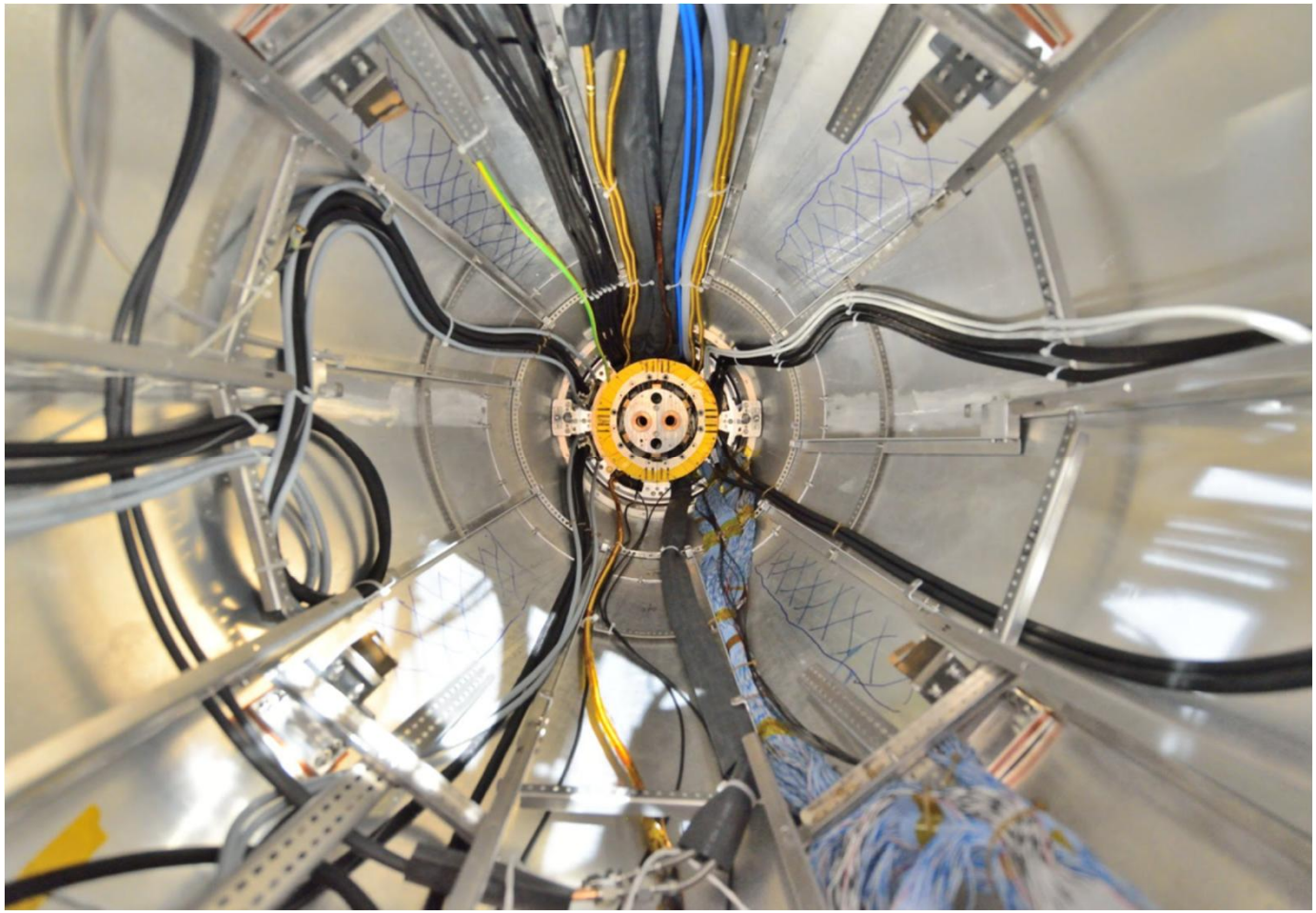
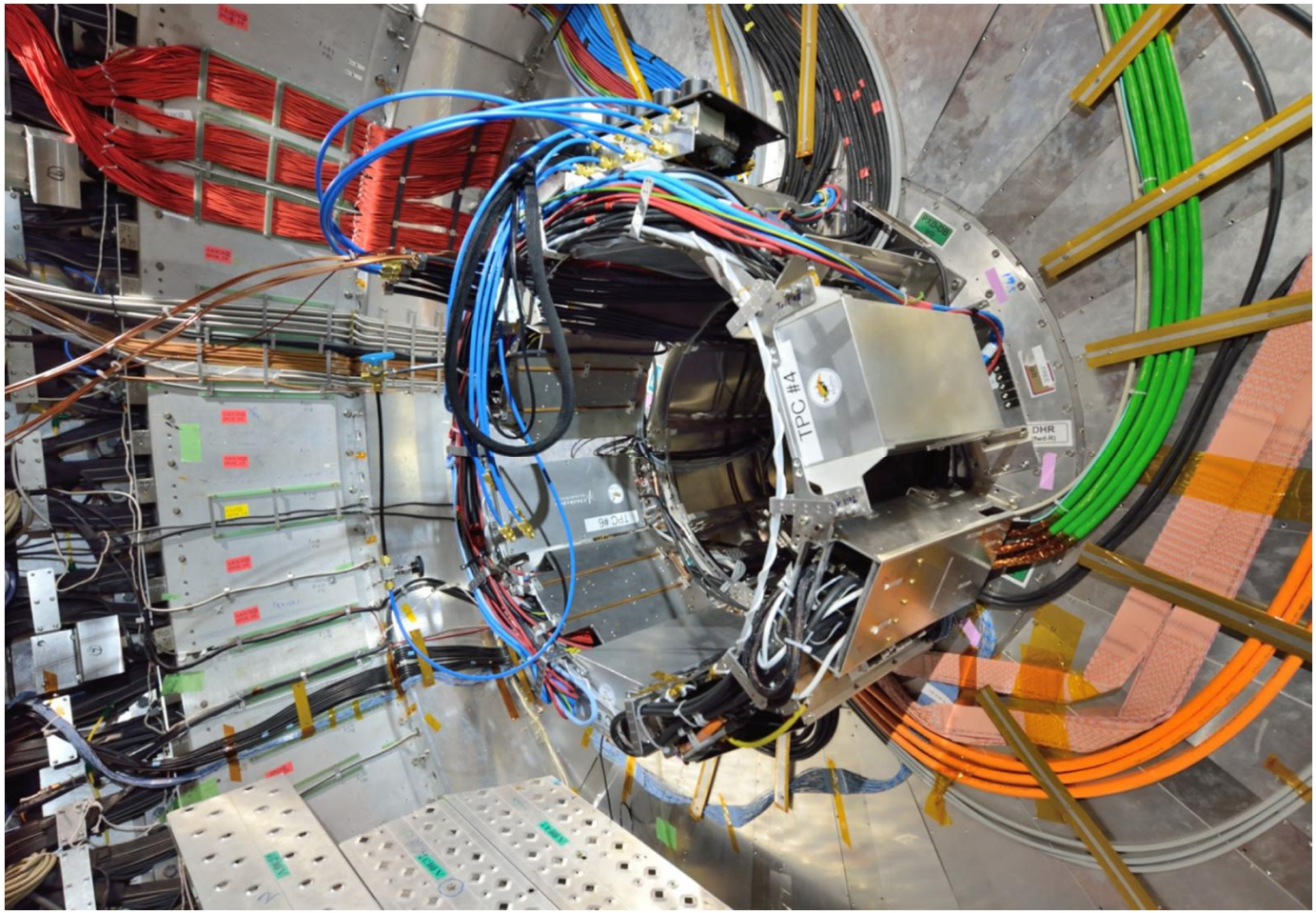


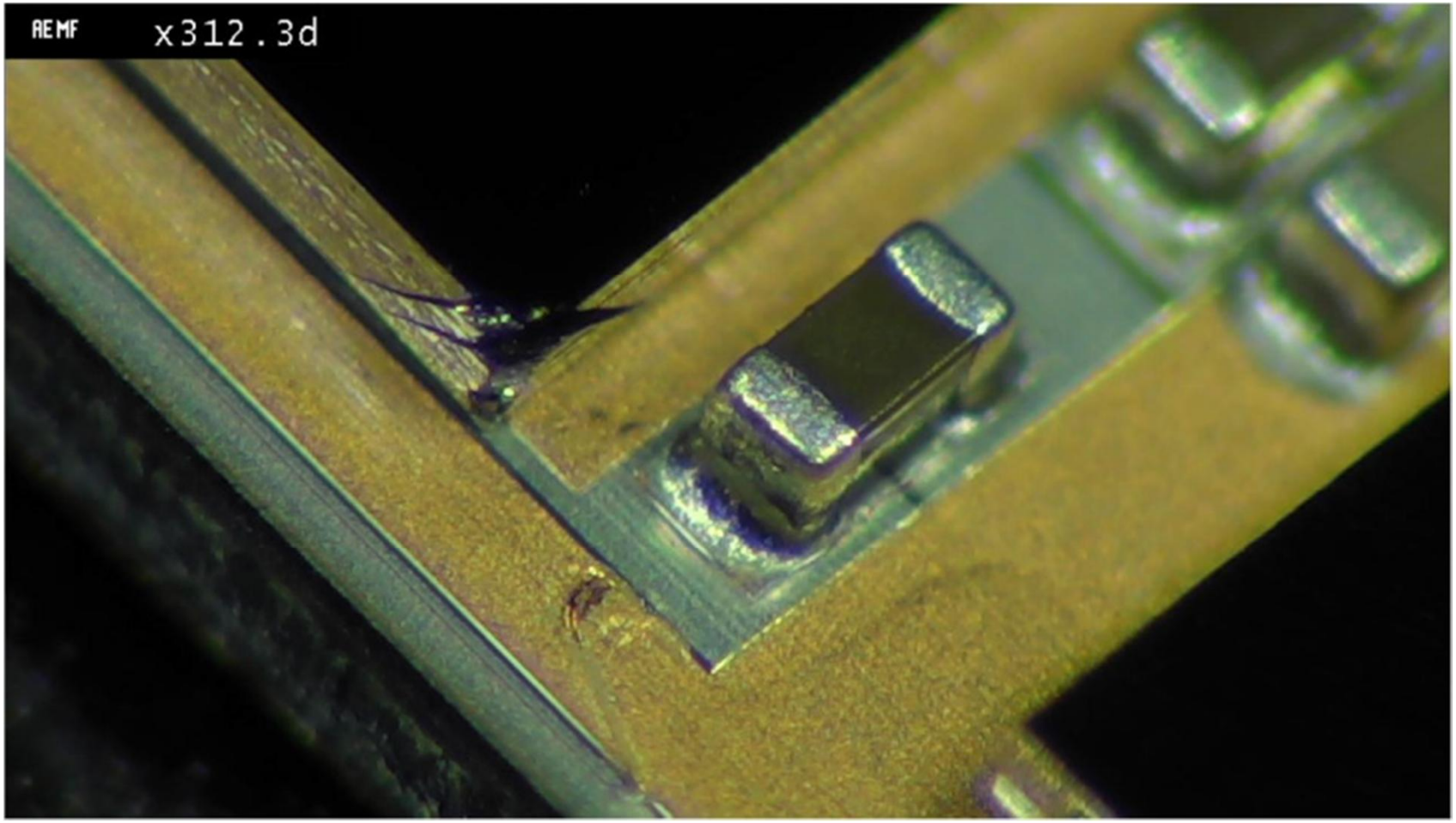
Cabling

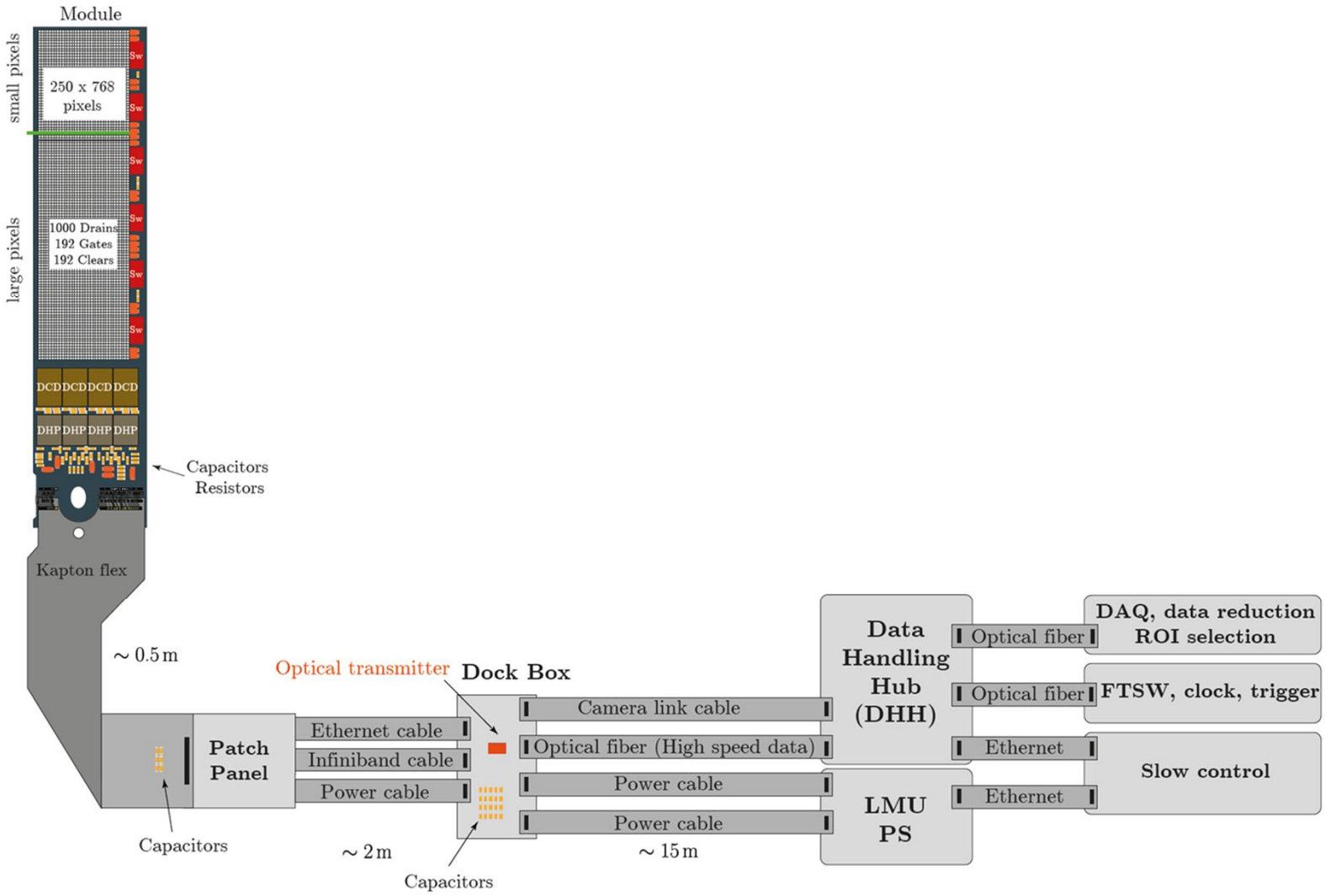


10 times less than in Phase 3

Cabling




AEMF
x312.3d


Module
small pixels
250 x 768 pixels
large pixels
1000 Drains
192 Gates
192 Clears
Sw
DCD DCD DCD DCD DCD
DHP DHP DHP DHP DHP
Capacitors
Resistors
Kapton flex
~ 0.5 m
Optical transmitter
Dock Box
Patch Panel
Ethernet cable
Infiniband cable
Power cable
Capacitors
~ 2 m
Capacitors
Camera link cable
Optical fiber (High speed data)
Power cable
Power cable
~ 15 m
Data Handling Hub (DHH)
LMU PS
Optical fiber
Optical fiber
Ethernet
Ethernet
DAQ, data reduction ROI selection
FTSW, clock, trigger
Slow control