Depleted monolithic CMOS pixels using column drain readout for the ATLAS Inner Tracker

13th "Trento" Workshop on Advanced Silicon Radiation Detectors

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IRFU CEA-Saclay
Y. Degerli, F. Guilloux and P. Schwemling
A new all-silicon Inner tracker will be installed @ ATLAS for the HL-LHC operation

- Stringent requirements for silicon pixels
  => Rad. level up to $10^{16} n_{eq}/cm^2$ & 1 Grad
  => High particle rate: occupancy, bandwidth, ...

Monolithic CMOS pixels are under evaluation for the outermost pixel layer

- Commercial process
- No need for fine pitch bump bonding

\[
d \sim \sqrt{\rho \cdot V}
\]
DMAPS – **Depleted** monolithic active pixel sensor

- Two different sensor design approaches pursued in this work

**Large fill factor – LFoundry 150nm CMOS**

- High res. (> 2 kΩ·cm) P-substrate
- Deep nwell as the charge collection node
- Full CMOS by isolating nw & deep nw
- Backside thinning & processing possible
  - Fully depleted 100 μm sensor available

**Small fill factor – TowerJazz 180nm CMOS**

- High res. (> 1 kΩ·cm) epi. layer (25 μm)
- Nwell as the charge collection node
- Full CMOS by using deep pw
- O(50 μm) thin detector possible
DMAPS – Depleted monolithic active pixel sensor

- Two different sensor design approaches pursued in this work

**Large fill factor – LFoundry 150nm CMOS**

- **Rad. hard => in line with ITk L4**
  - uniform field, short drift distance
- **Large sensor capacitance (200 - 400fF)**
  - non-negligible \( C_{pw} \)
  - noise & speed (power) penalties
  - x-talk: dedicated pixel design needed

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Two different sensor design approaches pursued in this work

Large fill factor – LFoundry 150nm CMOS

- High resistivity P-Substrate
- Very deep Nwell
- Deep Pwell
- Electronics (full CMOS)

Small fill factor – TowerJazz 180nm CMOS

- P stop
- P+ Epitaxial layer
- P++ Substrate
- PMOS
- NMOS

Rad. hard => in line with ITk L4
- uniform field, short drift distance

Large sensor capacitance (200 - 400fF)
- non-negligible $C_{pw}$
- noise & speed (power) penalties
- x-talk: dedicated pixel design needed

Very small sensor capacitance (< 10fF)
- low noise & power

Limited depletion, long sig. travel path
- dedicated efforts to enhance depletion
DMAPS – **Depleted** monolithic active pixel sensor

- Two different sensor design approaches pursued in this work

**Large fill factor – LFoundry 150nm CMOS**

- P stop
- Electronics (full CMOS)
- P stop
- C\text{pw}
- High resistivity P-Substrate

**Small fill factor – TowerJazz 180nm CMOS**

- Spacing
- PMOS
- NMOS
- Low dose N implant
- Depleted boundary
- P' Epitaxial layer
- P++ Substrate

**Rad. hard => in line with ITk L4**
- uniform field, short drift distance

**Large sensor capacitance (200 - 400fF)**
- non-negligible \( C_{pw} \)
- noise & speed (power) penalties
- x-talk: dedicated pixel design needed

- Modified process adding a planar N layer
  ⇒ significantly enhanced lateral depletion
  ⇒ maintain small sensor capacitance
  ⇒ no significant circuit change required
  ⇒ promising irradiation results

*talk by C. Riegel*

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Column drain readout architecture

- Similar to the current ATLAS pixel readout chip “FE-I3”
  - Particle rate @ L4 of ITk is similar to the current inner pixel detector
  - Sufficient rate capability with affordable in-pixel logic density for CMOS pixels

- BC ID (40 MHz) distributed in the column
- Hits read out sequentially in a shared bus
- Hit timing stamped in pixel
- ToT = TE - LE
Prototype design

Submitted: August, 2016
Received: January, 2017

Submitted: September, 2017
Received: January, 2018

Design by: LF-Monopix

Design by: TJ-Monopix
Chip design strategy

- Large scale demonstrate chip
  - 1 ~ 2 cm² chip size
- Simple periphery logic
  - Off-chip r.o. controller by FPGA
  - No trigger memory on chip
    => All hits r.o. sequentially in a serial link

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**On chip**
- Gray counter + Sense amplifiers + EoC logic
- Serializer + output driver
- Col./Pixel config.
- DACs
- Config. registers

**Off chip**
- R/O controller
- Serial Config. data
- Output data

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Pixel design: A functional view
Different sensor implementation concepts have strong implications on the pixel design (sensor geometry, FE circuit, pixel size, etc.)
Pixel design: LF-Monopix

- **Pixel size:** $50 \times 250 \, \mu m^2$
- **Fill factor** ~ 55%
- **CSA + Discri. with 4-bit DAC**
  - *Optimized for < 25 ns time walk*
  - *Static current ~ 20 \mu A/pixel*
- **Full-custom** dig. Circuit
  - *Minimized area => reduce C_d*
  - *Special low noise design, e.g. current steering circuit*
Pixel design: TJ-Monopix

- Pixel size $36 \times 40 \, \mu m^2$ => smaller than large fill factor design
- 2 $\mu m$ diameter diode + 3 $\mu m$ spacing
- Separate digital & analog region
- **Full-custom** digital design
  - Minimize area

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Pixel design: TJ-Monopix

- Front-end derived from the ALPIDE detector
  - Benefit from small $C_d$ (≈ 5fF)
  - Very compact and low power FE circuit
  - No need for in-pixel threshold trimming
- Circuit optimized for fast response
  - Power vs. speed trade-off

<table>
<thead>
<tr>
<th>Threshold</th>
<th>300 e-</th>
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<tbody>
<tr>
<td>ENC</td>
<td>7.1 e-</td>
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<tr>
<td>Thres. dispersion</td>
<td>10.2 e-</td>
</tr>
<tr>
<td>Time walk</td>
<td>&lt; 25 ns</td>
</tr>
<tr>
<td>Power</td>
<td>&lt; 1 μW</td>
</tr>
</tbody>
</table>
Key measurement results: LF-Monopix
**Test beam**

SPS CERN
- 180 GeV pion
- Sep. 20-28, 2017

ELSA Bonn
- 2.5 GeV electron
- Nov. 8-10, 2017

DUTs: 1 non-irradiated + 1 neutron-irradiated $10^{15}$n$_{eq}$/cm$^2$

- **DUTs**
  - MIMOSA $\times$ 6
    - Pixel size: 18.2 $\mu$m $\times$ 18.2$\mu$m
    - 1152 $\mu$s/frame (rolling shutter)
  - FE-I4 $\times$ 1
    - Pixel size: 250 $\mu$m $\times$ 50 $\mu$m
    - Timing resolution: 25ns
    - Triggered by scintillator + TLU

**ANEMONE telescope**
https://indico.desy.de/indico/event/18050/session/9/contribution/17/material/slides/0.pdf

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ELSA test beam: Efficiency

- Non-irradiated
  TH tuned by noise
  Columns: 16-20
  HV: -200V
  Temp: dry ice

- $1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$
  TH tuned by noise
  Columns: 16-20
  HV: -130V
  Temp: dry ice
Timing performance

Delay = (Monopix LE) - (Scintillator LE)

- Promising timing results from non-irradiated chip for 400 fF $C_d$
  - More precise measurement needed
- Time walk increased for irradiated chip, but results obtained @ default settings
  - Optimization of DAC settings, e.g. CSA/discriminator bias
  - Higher bias voltage + back side process
  - Time walk correction of “small” hits

TH: ~1700 e-
Columns: 16-20
HV: -200V (0 $n_{eq}/cm^2$) -130V (1 x $10^{15}n_{eq}/cm^2$)
DAC setting: default
Temp: dry ice

2bins=98.7 ± 0.9%
2bins=83.0 ± 0.8%, un-tuned!
SPS test beam

- Analysis finished on non-irradiated sample for the SPS test beam
  - Columns 8 - 11 & 24 - 27
  - Threshold ~ 2700 e-
  - Room temperature

99.7% @ -200V

I. Caicedo, Bonn

Uniform in-pixel efficiency @ -200V
Summary

• Two large scale DMAPS demonstrator chips developed for the ATLAS ITk
  – Aimed for the outermost pixel layer: cheap module, simple assembly
  – Different sensor concepts pursued: large & small fill factor
  – Column drain readout for sufficient rate capability with affordable in pixel logic density

• LF-Monopix, at least matrix-wise, is a fully functional LHC pixel chip
  – Fully monolithic readout, 40 MHz time stamping, tunable threshold, etc.
  – High efficiency ~99% after \(1 \times 10^{15}n_{eq}/cm^2\) @ very low noise occupancy < \(10^{-8}\)
  => meet the ATLAS spec.
  – Good timing performance already @ default setting => will be improved by tuning
  – Wafer thinned down to 100 μm and backside processed soon available (sent for dicing)
    => better charge collection after irradiation expected

• TJ-Monopix has been wire-bonded last Friday, results will come soon
  – Chip samples sent for neutron irradiation @ JSI Ljubljana
  – Test beam planned for April/May
Thank you!
Back up
LFoundry prototypes

CCPD_LF
- Subm. in **Sep. 2014**
- 33 x 125 µm² pixels
- Fast R/O coupled to R/O chip
- Standalone R/O for test

LF-CPIX (DEMO)
- Subm. in **Mar. 2016**
- 50 x 250 µm² pixels
- Fast R/O coupled to R/O chip
- Standalone R/O for test

LF-Monopix01
- Subm. in **Aug. 2016**
- 50 x 250 µm² pixels
- **Fast standalone R/O**
- Standalone R/O like LF-CPIX
Design challenges for LF-Monopix

- Large detector capacitance $C_d = C_{sub} + C_n + C_{pw}$
  - $C_{pw}$ tends to be dominant $\Rightarrow$ depends on electronics area & DNW/PW junction width
  - Timing
    $$\tau_{CSA} \propto \frac{1}{g_m} \frac{C_d}{C_f}$$
  - Noise
    $$ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_d^2}{\tau}$$
  - Cross talk $\Rightarrow C_{pw}$ directly couples the substrate noise into the sensor

• The minimum operation threshold may be affected

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Radiation tolerance evaluated with previous prototypes \(\Rightarrow\) in line with ITk L4

- Total ionizing dose

\[ \int \int_0^{\text{rad}} \text{Normalized gain} \, dTID \]

\[ \int \int_0^{\text{rad}} \text{Normalized noise} \, dTID \]

No significant performance loss after 50 Mrad

- NIEL

\[ \Phi = 0 \]
\[ \Phi = 1 \times 10^{13} \]
\[ \Phi = 5 \times 10^{13} \]
\[ \Phi = 1 \times 10^{14} \]
\[ \Phi = 5 \times 10^{14} \]
\[ \Phi = 1 \times 10^{15} \]
\[ \Phi = 2 \times 10^{15} \]

\[ 1 \times 10^{15} \, \text{n}_{\text{eq}/\text{cm}^2} \]

\[ > 100 \, \mu\text{m} \text{ depletion after} \, 10^{15} \, \text{n}_{\text{eq}/\text{cm}^2} \]
Improvement after back-side processing

E-TCT measurement on LF test structures thinned and Backside-processed to 200µm
I. Mandić, RD50 workshop 2017
Irradiation performance: TowerJazz

- **Modified process** (CERN TowerJazz collaboration) to improve depletion under pwell
  - *Adding a planar N-type layer*
  - *Beam test showed 98.5% efficiency after $10^{15}n_{eq}/cm^2*

  => *not possible with standard process*

H. Pernegger, et al., DOI: 10.1088/1748-0221/12/06/P06008
I-V curve: LF-Monopix

- Break down @ ~ -280 V
• Breakdown @ -280 V => up to ~ 300 μm depletion
• ToT calibrated with sources: $^{241}$Am, terbium
• Gain 10 -12 μV/e$^{-}$
• Typical ENC ~ 200 e$^{-}$
• Tunable threshold down to 1400 e$^{-}$
  – dispersion ~ 100e$^{-}$
ToT calibration: LF-Monopix

Injection vs. ToT

ToT vs. Inj, LF-MONOPIX01: Pix[26,10], TH = 0.855 V, VPFB=4

ΔV
Low feedback voltage (VPFB): Longer ToT (sampling with higher resolution)
10μs 35μs
64μs

- Low feedback current for CSA to have wider analog pulse
  => Larger ToT range to have better analog resolution for sensor characterization
- Injection capacitance is measured to be ~ 2.75 fF
  \[ C_{inj} = \frac{Q}{V_{inj}} \]

Response to source

Sources, LF-MONOPIX01: Pix[26, 10] \( TH = 0.855 \text{V} \), VPFB = 4

- 241-Am, Bias -70V
  \[ \mu = 79.078, \sigma = 2.879 \]
  \[ V = 0.966V, C_{inj} = 2.738fF \]

- Tb XR, Bias -70V
  \[ \mu = 48.304, \sigma = 2.811 \]
  \[ V = 0.711V, C_{inj} = 2.757fF \]

- Tb XR, Bias -70V
  \[ \mu = 63.256, \sigma = 2.685 \]
  \[ V = 0.827V, C_{inj} = 2.707fF \]
Gain: LF-Monopix

I. Caicedo, Bonn

Gain $10-12 \, \mu V / e^-$ in flavours with the V2 discriminator $\sim 10\%$ larger than those with V1
Noise: LF-Monopix

ENC 120-170 $e^{-}$ for flavours with external R/O logic or NMOS CSA

ENC $\sim$200 $e^{-}$ for flavours with in-pixel logic, CMOS CSA and V1 discriminator (plus 20-40 $e^{-}$ for those with V2 discriminator)
Threshold tuning: LF-Monopix

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Larger dispersion for discriminator V2 mainly due to smaller input transistors

Threshold dispersion after tuning is ~ 100 e⁻

Untuned threshold dispersion for flavours with the V1 discriminator ~400-600 e⁻ (plus 350-400 e⁻ for those with integrated pixel R/O logic and the V2 discriminator)
NIEL: LF-Monopix

- No breakdown after 200V
- Noise increase => 1 Mrad back ground?
Test beam

- SPS CERN
  - 180 GeV pion
  - Sep 20-28, 2017

- ELSA Bonn
  - 2.5GeV electron
  - Nov 8-10, 2017

Time structure of Beam

Plane: most upper stream MIMOSA plane
Analysis: noisy pixel removed, cauterized

**CERN**

![Graph showing time structure of Beam at CERN]

**ELSA**

![Graph showing time structure of Beam at ELSA]
Charge spectrum

- **ToT values of seed pixel**
  - Non-irradiated
  - 1 x $10^{15}$ $n_{eq}/cm^2$

- **Injection vs ToT**
  - Threshold: 1500 e
  - Bias: -200V (0 $n_{eq}/cm^2$)
  - **-130V** (1 x $10^{15}$ $n_{eq}/cm^2$)
  - Flavor: CMOS V1
  - DAC setting: Default
  - Source: 2.5GeV electron
  - Temperature: cooled by dry ice

- **Un-irradiated** ~20ke at -100V, irradiated ~4.5ke at -130V
- The MPV is decreased after neutron irradiation.
ELSA test beam: Noise occupancy

- Non-irradiated
  TH: tuned by noise + 4mV
  Columns: 16-20
  HV: -200V
  Temp: dry ice

- $1 \times 10^{15} \text{n}_{eq}/\text{cm}^2$
  TH: tuned by noise
  Columns: 16-20
  HV: -130V
  Temp: dry ice

Noise occupancy $<10^{-7}$
@ TH$\sim$1400e-

Noise occupancy $<10^{-8}$
@ TH$\sim$1700e-
ELSA test beam: In-pixel Efficiency

- N-well (collection well)
- P-well

- Non-irradiated

- $1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$
Efficiency @ SPS test beam: LF-Monopix

-200V SPS Efficiency

99.7%
@ -200V

99.0
97.5
96.0
94.5
93.0
91.5
90.0

-100V SPS Efficiency

99.7%
@ -100V

99.0
97.5
96.0
94.5
93.0
91.5
90.0

-5V SPS Efficiency

98.8%
@ -5V

99.0
97.5
96.0
94.5
93.0
91.5
90.0

Lower efficiency due to less signal @ low bias
=> Efficiency drop between pixels
Rate capability of TJ-Monopix – the matrix

- It is assumed that in the final prototype
  - 2 double columns per r.o. unit => 512 × 4 pixels
  - 20 MHz column bandwidth: 50 ns (2 BC) per hit readout
    => a simple math: max. allowed hit rate = 1/column bandwidth = 0.5 hit/r.o.unit/BC
- Inefficiency caused by trig. memory pileup not included here => pure matrix performance
- Data loss increases steeply beyond 600 MHz/cm² => ~ 0.44 hits/r.o.unit/BC
Pixel design: LF-Monopix

Pre-amplifier (CSA)

- NMOS input pre-amp.
- CMOS input pre-amp.
- Optimized for peaking time $\leq 25\text{ns}$
- Bias $\sim 17\ \mu\text{A}$

Discriminator (4-bit in-pixel DAC)

- 2-stage amplifier
- Bias $\sim 4.5\ \mu\text{A}$
- Complementary structure
- Self bias $\sim 4\ \mu\text{A}$

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Pixel design: LF-Monopix

- **Full-custom** digital circuit
  - Minimized area => for less $C_d$
  - Low noise circuit design for critical dig. blocks

*Token propagates while pixels are sensitive* => *Current Steering (CS) logic*
Pixel design: LF-Monopix

- Full-custom digital circuit
  - Minimized area => for less $C_d$
  - Low noise circuit design for critical dig. blocks

RAM cell R/O by source follower
=> Avoids high current injection into PW
We can move the in-pixel r.o. logic to the periphery

- Discriminator output r.o. by source follower
- Less area needed for in-pixel electronic => less $C_d$
- Almost no in-pixel digital transient
- Almost no signal distributed in the column
- One-to-one connection from pixel to R/O logic => Complex routing

} => less noise/cross talk
Pixel array: LF-Monopix

- Pixel array: $129 \times 36$
- 9 pixel designs
  - 7 with in-pixel logic
  - 2 w/o in-pixel logic
- 4 columns/design
Pixel design: TJ-Monopix

**PMOS reset**
- Used in previous TJ chips
- $I_{\text{RESET}}$ should be larger than max. leakage

**Adaptive PMOS reset**
- Reset PMOS adaptively biased by a feedback loop
- Less sensitive to leakage increase after irradiation

**Diode reset with HV bias**
- Front-side HV to further enhance the depletion
- Diode reset for HV compatibility
- Sensor AC coupled to the FE
• Pixel array $224 \times 448$, composed of equally divided 4 sub arrays

- PMOS reset
- In-pixel RAM r/o by \textit{gated} source follower

- PMOS reset
- In-pixel RAM r/o by source follower

- Adaptive PMOS reset
- HV + diode reset
- AC coupled to FE
• Pre-amplifiers => aimed at peaking time $\approx 25$ ns with $400 \, \text{fF} \, C_d$
  – NMOS input: modified from LF-CPIX in order to deal with the increased $C_d$
    - Bias current $\sim 17 \, \mu\text{A}$
    - Peaking time $\sim 20$ ns (4 ke$^-$ signal)$^1$
    - ENC $\sim 170$ e$^-$
  – CMOS input: same as LF-CPIX
    - Bias current $\sim 15 \, \mu\text{A}$
    - Peaking time $\sim 25$ ns (4 ke$^-$ signal)$^1$
    - ENC $\sim 135$ e$^-$
Time walk also depends on discriminator design

- Discriminator V1: same as LF-CPIX
  - 2-stage amplifier as comparator
  - Bias current: 4.5 μA
  - Slow at threshold edge

- Discriminator V2:
  - Two amplifiers load each other
  - Self biased: < 4μA
  - CMOS inverter as 2nd stage
Front-end simulation performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge threshold $Q_{th}$</td>
<td>300 e</td>
<td></td>
</tr>
<tr>
<td>Equivalent Noise Charge</td>
<td>7.1 e</td>
<td>threshold/noise &gt; 10</td>
</tr>
<tr>
<td>Channel-to-channel RMS</td>
<td>10.2 e</td>
<td>good threshold uniformity, no need for in-pixel tuning</td>
</tr>
</tbody>
</table>

![Graph](image)

**Time-Walk**

- $P_{analog} = 0.9 \mu W$

Thanushan Kugathasan - TWEPP 2017 - 14/09/2017
# LF-Monopix vs. TJ-Monopix

<table>
<thead>
<tr>
<th></th>
<th>LF-Monopix</th>
<th>TJ-Monopix</th>
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<tbody>
<tr>
<td><strong>Tech.</strong></td>
<td>LFoundry 150 nm CMOS</td>
<td>TowerJazz 180 nm CMOS</td>
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<tr>
<td><strong>Sensor concept</strong></td>
<td><strong>Large fill factor</strong></td>
<td><strong>Small fill factor</strong></td>
</tr>
<tr>
<td><strong>Chip size</strong></td>
<td>$\sim 1 \times 1\text{cm}^2$</td>
<td>$\sim 1 \times 2\text{cm}^2$</td>
</tr>
<tr>
<td><strong>Pixel array</strong></td>
<td>$129 \times 36$</td>
<td>$224 \times 448$</td>
</tr>
<tr>
<td><strong>Pixel size</strong></td>
<td>$50 \times 250\text{μm}^2$</td>
<td>$36 \times 40\text{μm}^2$</td>
</tr>
<tr>
<td><strong>Ana. current/pixel</strong></td>
<td>$\sim 20\text{μA/pixel}$</td>
<td>$&lt; 1\text{μA/pixel}$</td>
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<tr>
<td><strong>Pixel variants</strong></td>
<td>9</td>
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