Performance of the monolithic matrices of the H35DEMO chip before and after irradiation

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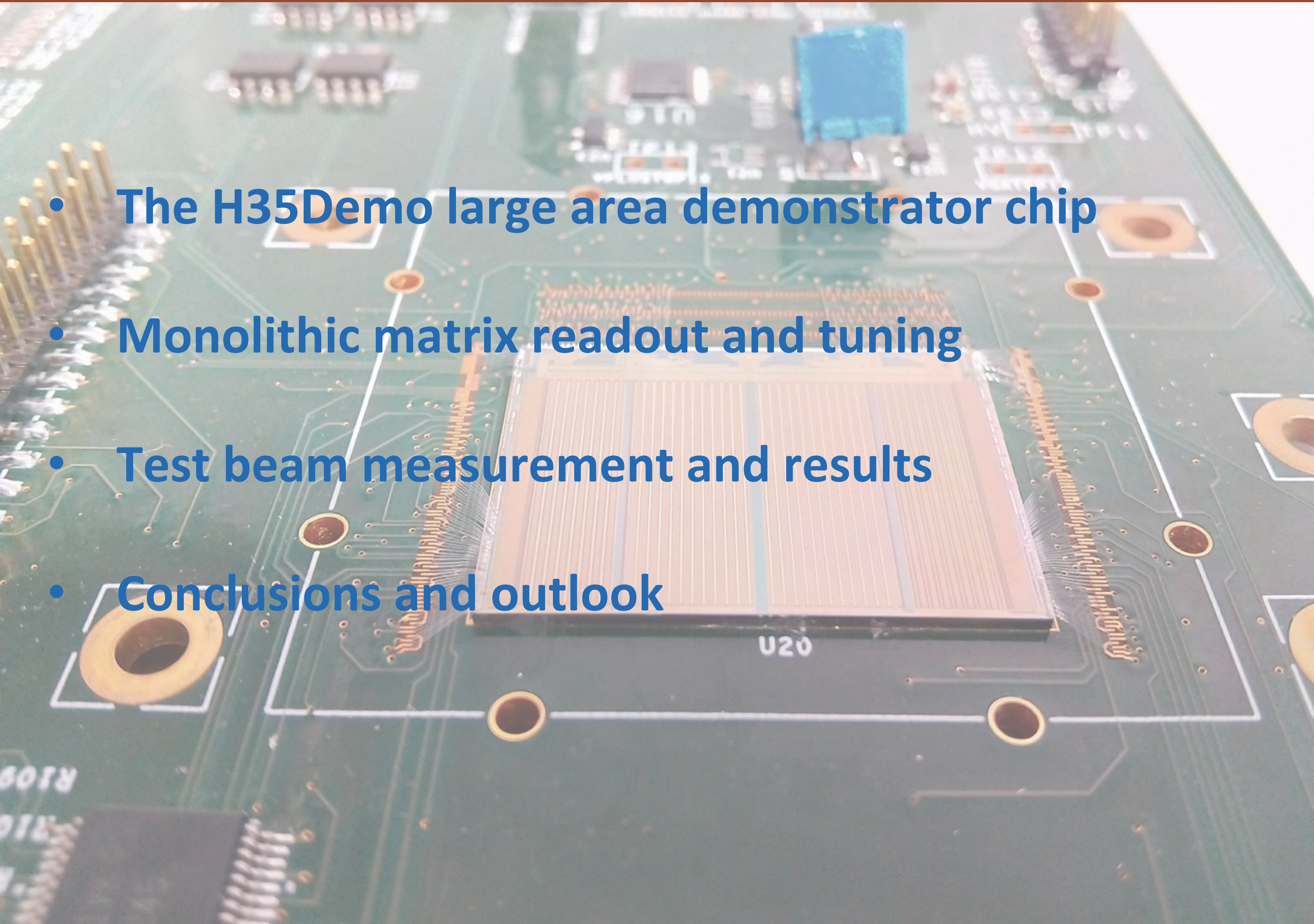
BIST Barcelona Institute of Science and Technology

Test beam measurements in collaboration with University of Geneva

UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

13th "Trento" Workshop
Munich, 20th February 2018

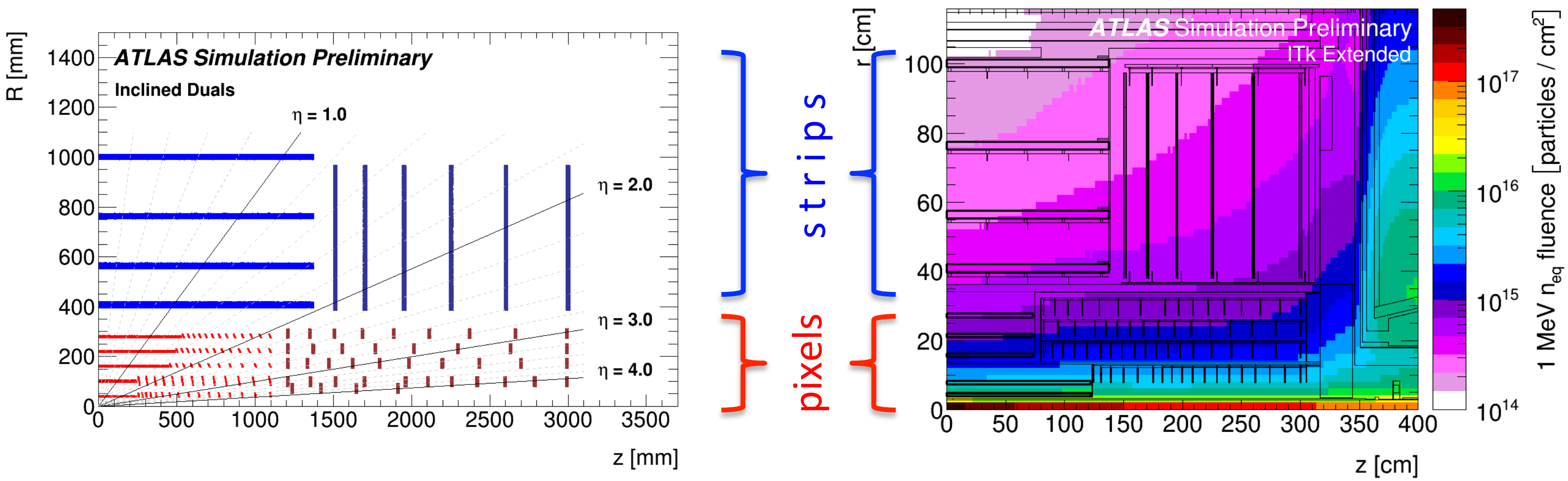
Outline



- The H35Demo large area demonstrator chip
- Monolithic matrix readout and tuning
- Test beam measurement and results
- Conclusions and outlook

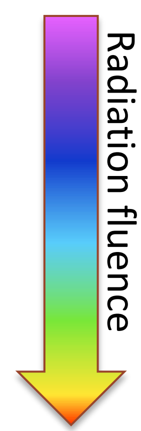
The ITk upgrade for HL-LHC

Replace the whole ATLAS Inner Detector with a new full-silicon Inner Tracker (ITk)



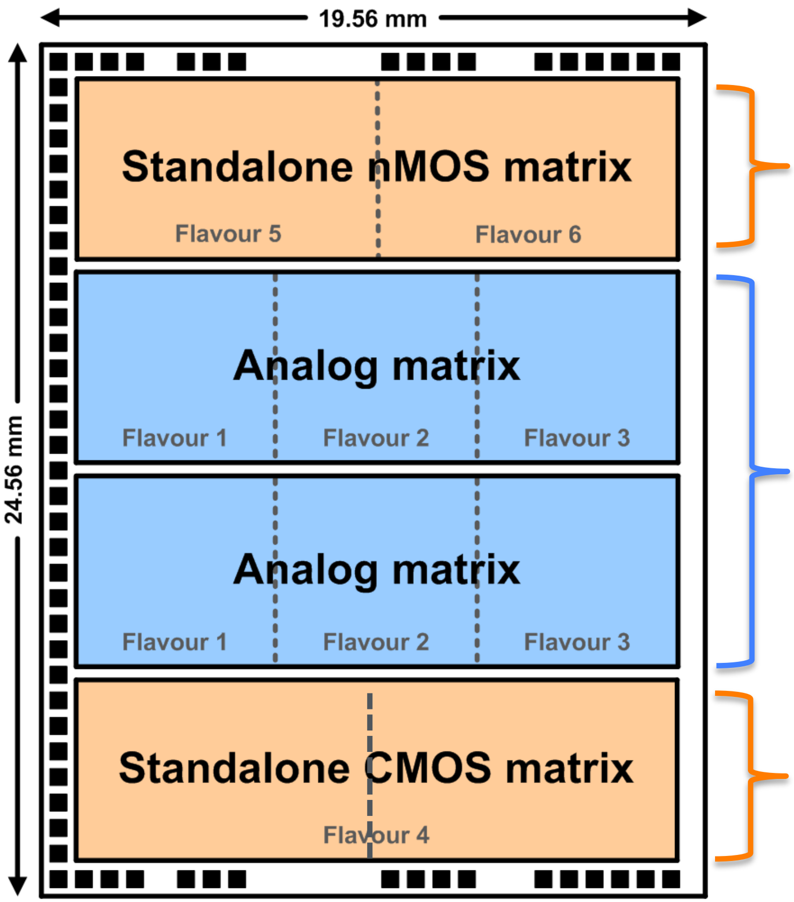
- New layout with 5 pixel barrel layers & large η coverage

- Sensor technologies under investigation:
  - Outer pixel layers (large area to cover)
    - HR/HV-CMOS pixel detectors ➔ 1.5e15 $n_{eq}cm^{-2}$
    - n-in-p planar silicon sensors (150 µm thick)
  - Inner pixel layers
    - Thin n-in-p planar silicon sensors (100 µm thick)
    - 3D silicon sensors (baseline for the innermost layer)



The H35 Demonstrator

AMS 350 nm High Voltage CMOS: different ρ: 20–80–200–1000 Ωcm



Designed by KIT, IFAE and Univ. of Liverpool

Standalone nMOS matrix:

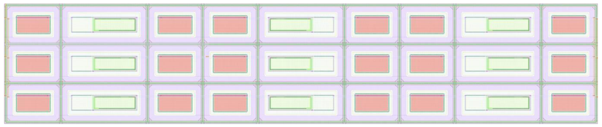
- Digital pixels with in-pixel nMOS comparator
- Two flavors: with and without Time Walk (TW) compensation

Analog matrices (2 arrays):

- To be Capacitive Coupled (CC) to FE-I4 readout chips

Standalone CMOS matrix:

- Analog pixels with off-pixel CMOS comparator



+ test structures without electronics for TCT studies

see D M S Sultan, M. Franks & A. Fehr talks

The H35 Demonstrator

AMS 350 nm High Voltage CMOS: different ρ: 20–80–200–1000 Ωcm

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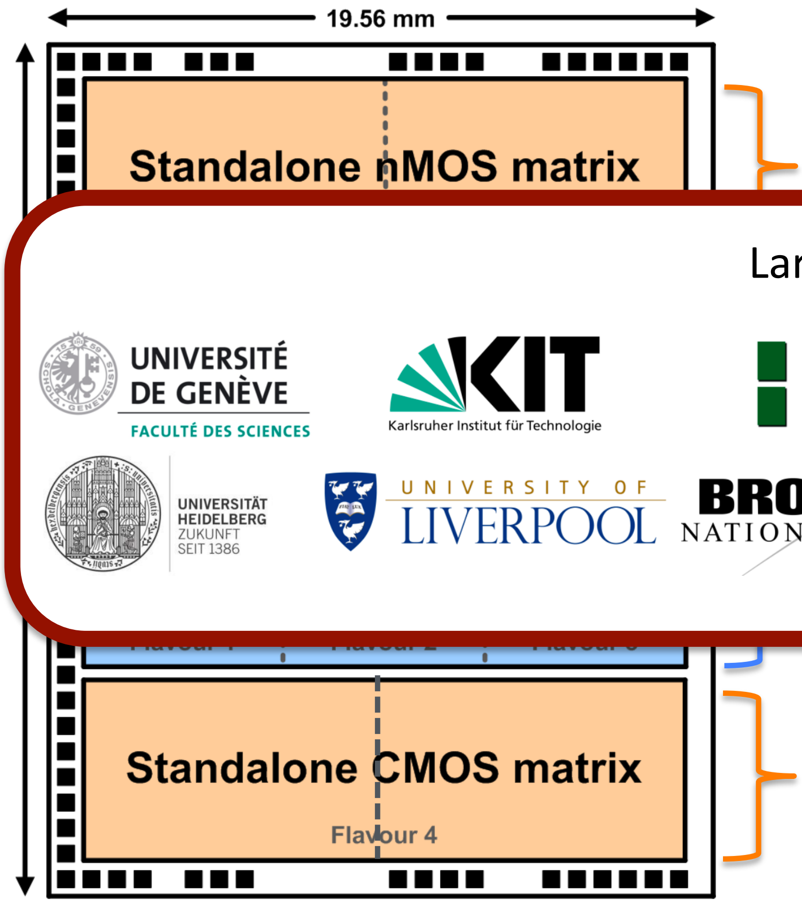


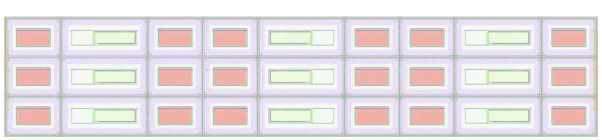
Standalone nMOS matrix:

Large collaboration

UNIVERSITÉ DE GENÈVE – FACULTÉ DES SCIENCES · KIT Karlsruher Institut für Technologie · IFAE · u^b UNIVERSITÄT BERN – AEC ALBERT EINSTEIN CENTER FOR FUNDAMENTAL PHYSICS · Argonne NATIONAL LABORATORY · JSI · UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386 · UNIVERSITY OF LIVERPOOL · BROOKHAVEN NATIONAL LABORATORY · CERN · 筑波大学 University of Tsukuba

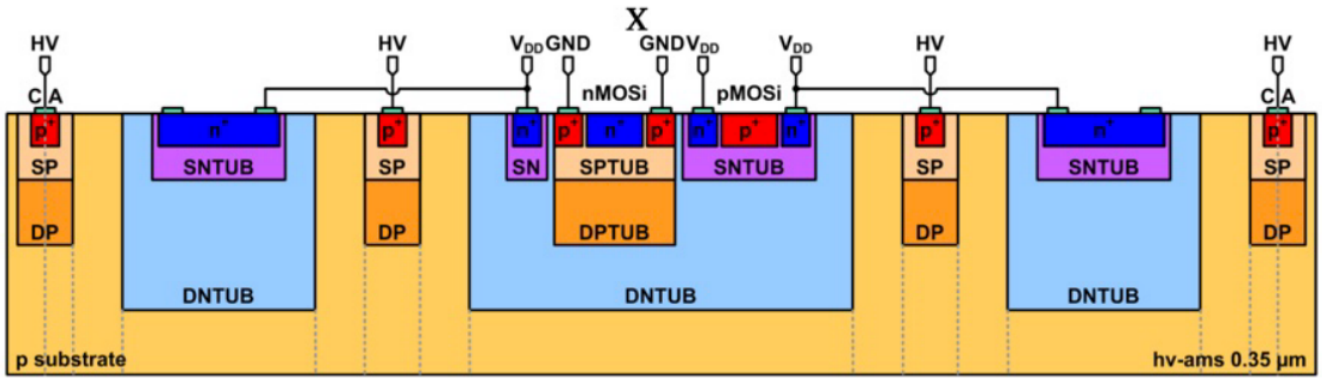
Standalone CMOS matrix:

- Analog pixels with off-pixel CMOS comparator



\+ test structures without electronics for TCT studies
see D M S Sultan, M. Franks & A. Fehr talks

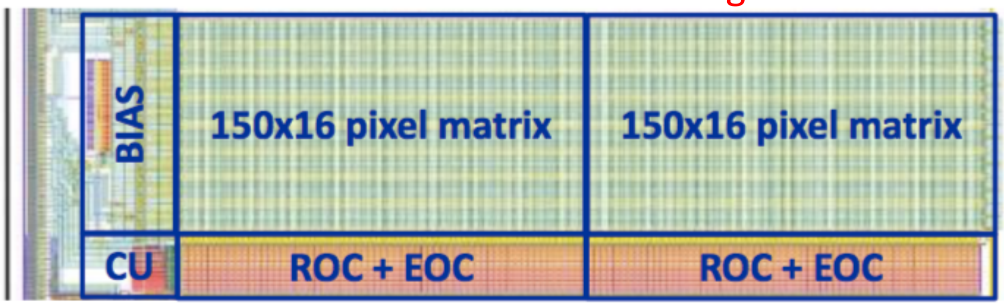
The H35 pixel structure

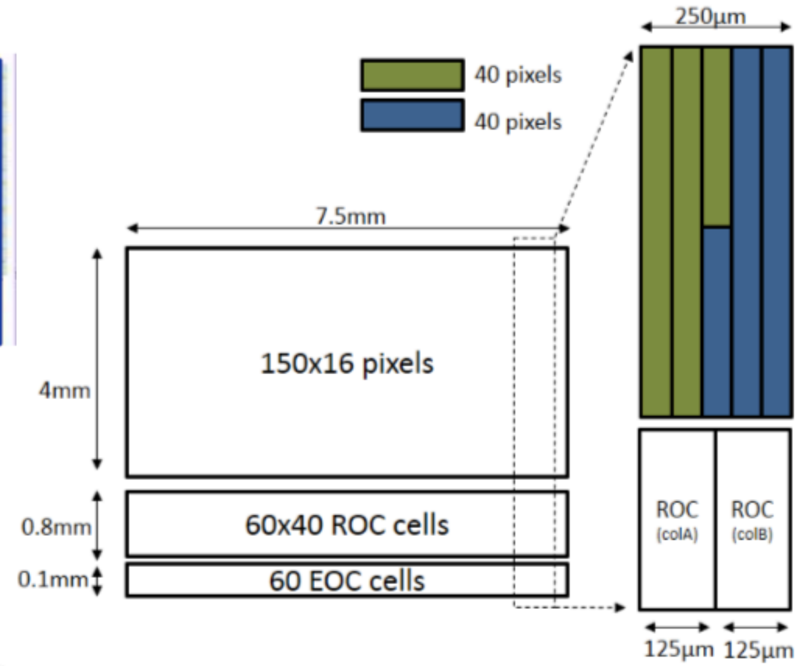


- Pixel size: 50x250 µm^2
- Large fill factor:
  - nMOS and pMOS transistors embedded in the same deep n-wells acting as collecting electrodes
    - p-substrate + 3 separate deep n-wells* to reduce the large capacitance
  - Full depletion & more uniform electric field
  - Short drift
- Bias voltage applied from the top
  - Single side processing
  - Bias voltage > 150 V

*all matrices but monolithic nMOS

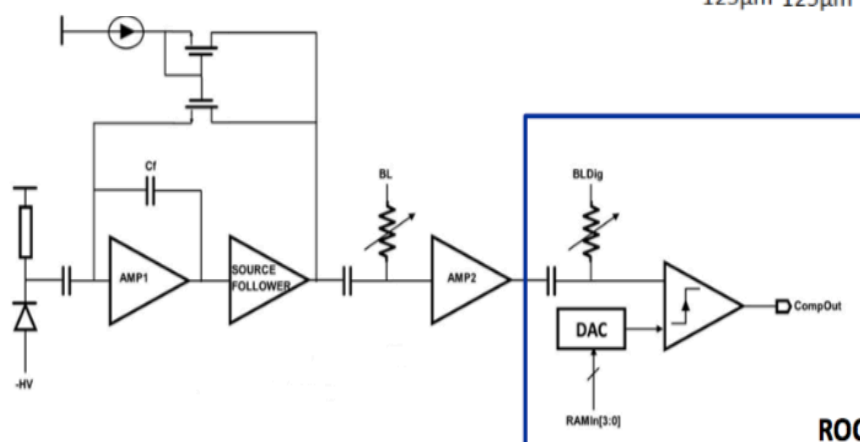
The monolithic CMOS matrix





- Analog electronics on pixel

- Digital electronics in the periphery
  - ReadOutCell (ROC)
  - End Of Column (EOC)
  - Control Unit (CU)



- Off-pixel discriminators in the ROC:
  - 1 in the Left part
  - 2 the Right part (additional time-stamp for better timing)

- Column drain readout architecture with priority encoding
  - Trigger-less readout

Monolithic matrix readout at IFAE

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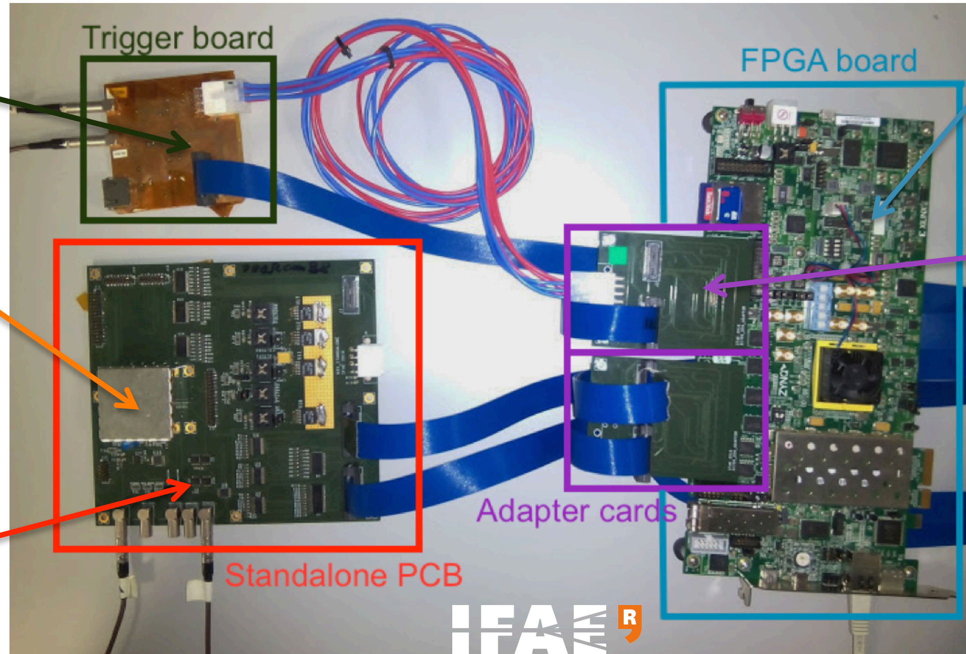
Trigger board
- Trigger in
- Busy out
- RJ45

H35demo chip
- Both CMOS and nMOS matrices wire-bonded

H35demo PCB
- Voltage regulators
- Sensor bias input
- Injection pulse input
- Analog signal output



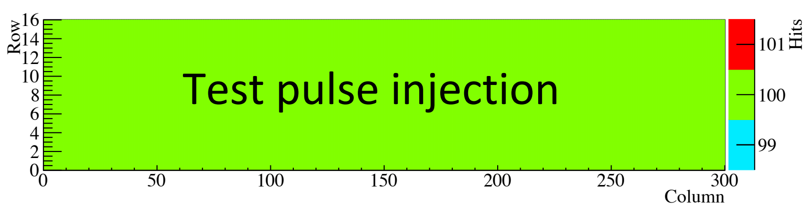
FPGA board
- Xilinx ZC706

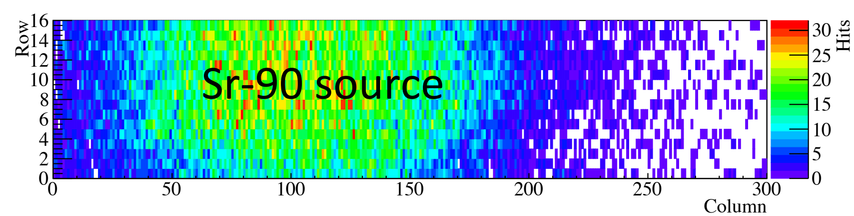
Adapter PCBs
- 1x H35 PCB
- 1x test signals
- 1x trigger board

External
- Pulse generator
- Power supplies

S. Terzo et al., JINST 12 (2017) no.6, C06009

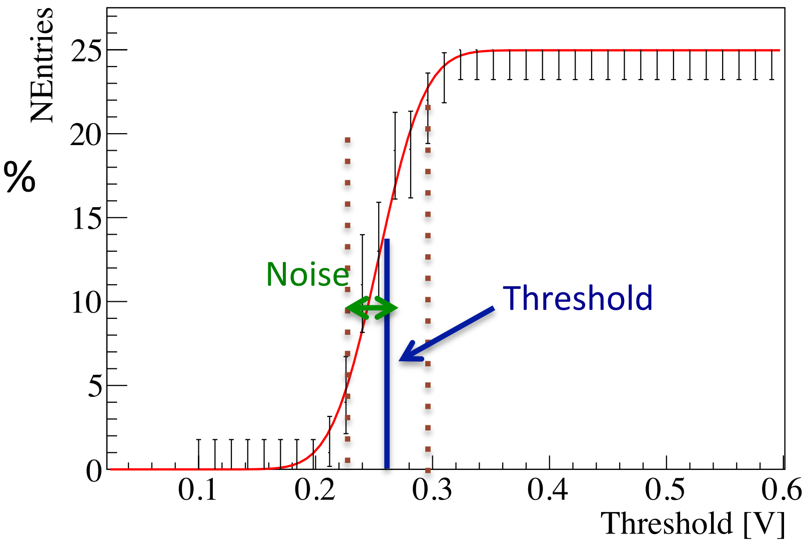
PCBs, FPGA firmware and software developed at IFAE

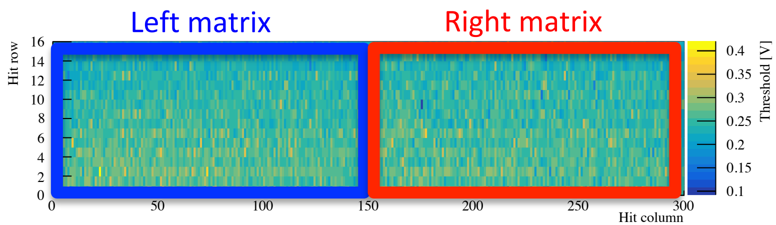


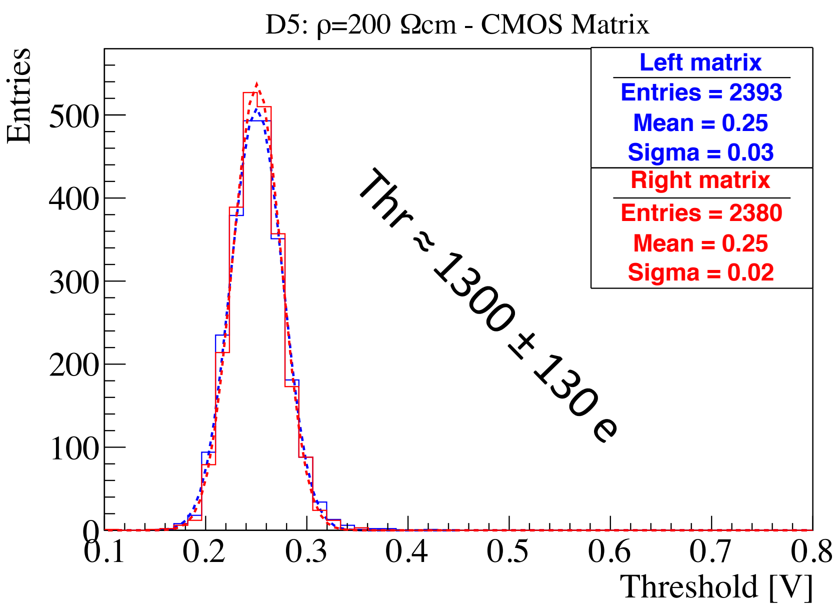


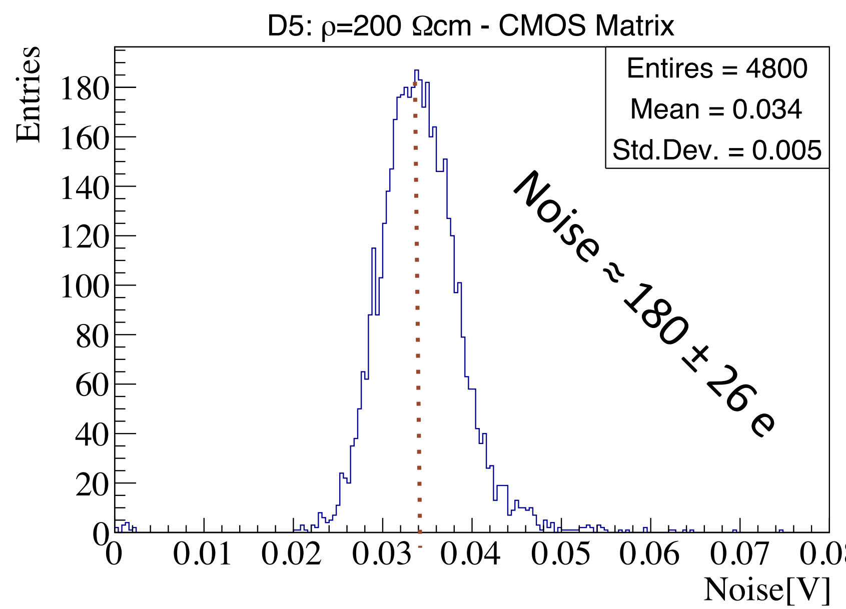
Monolithic matrix tuning

- CMOS matrix tuning (not irradiated):
  - Min. achieved threshold: 1300 ± 130 e
  - Threshold noise = 180 ± 26 e
  - Noise occupancy in 25 ns with less than 1% of pixel masked: $N_{occ} < 2\times10^{-7}$









CMOS matrix tuning (irradiated)

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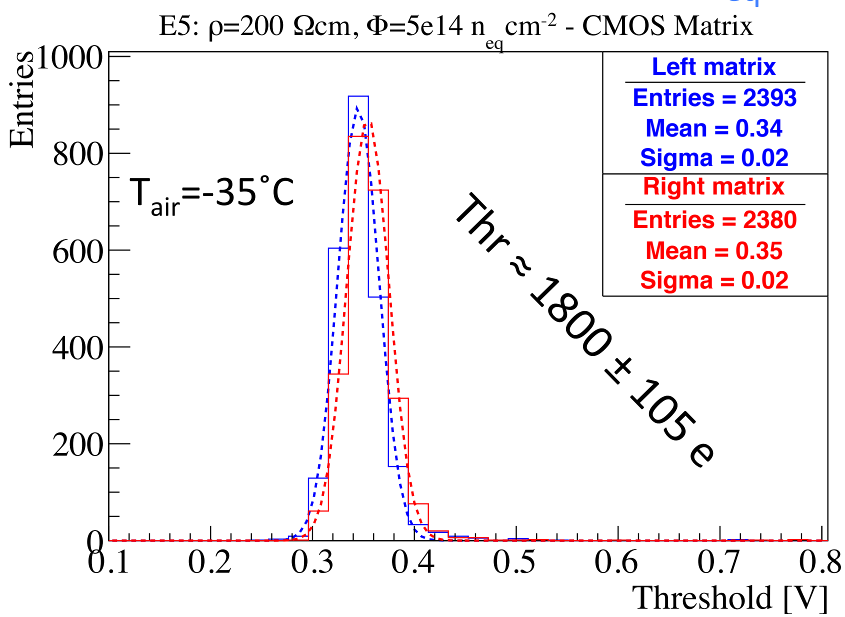
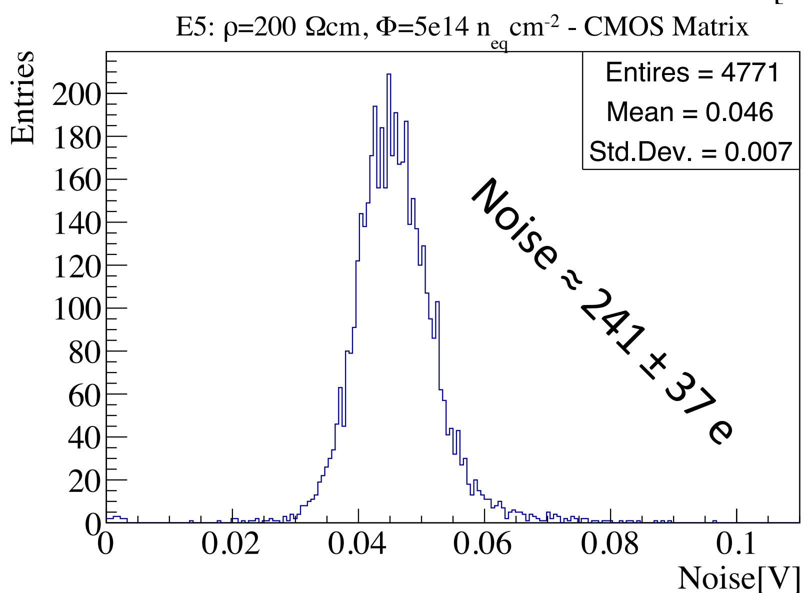
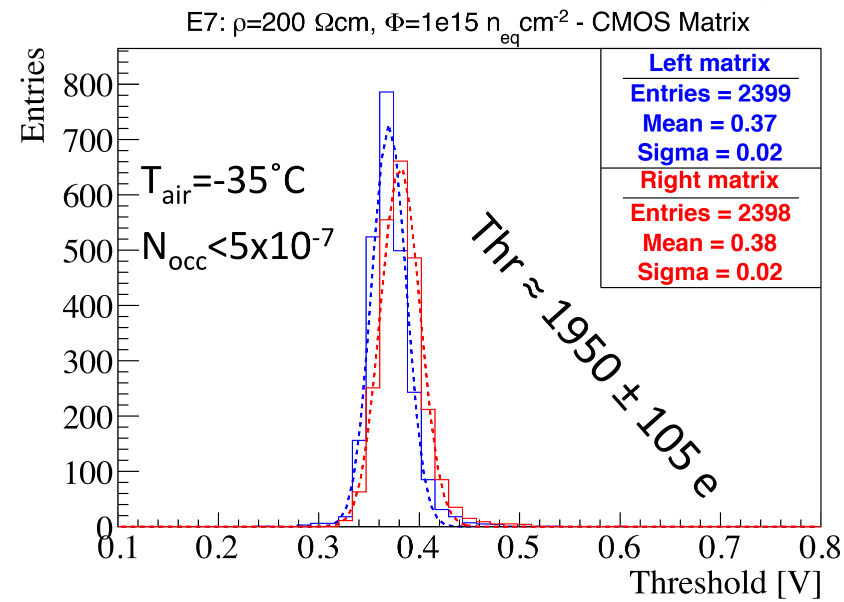
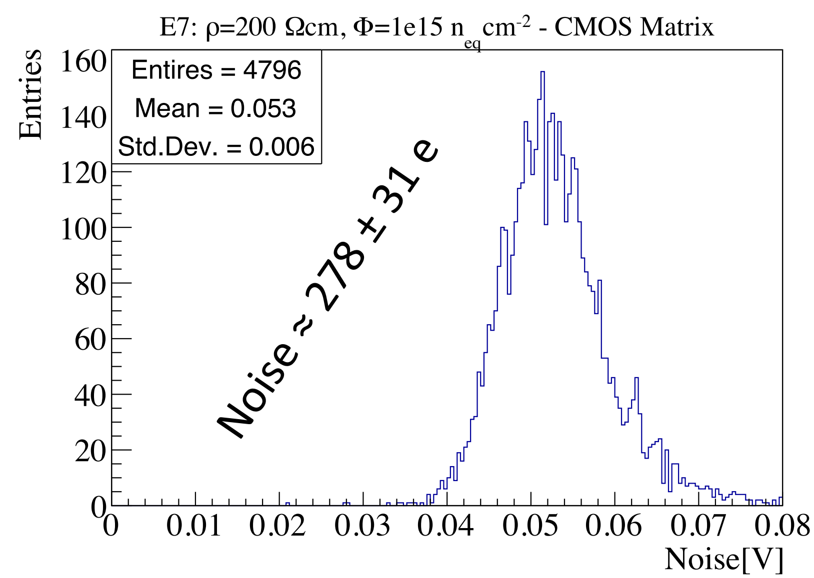
Irradiated with neutrons to 5e14 $n_{eq}cm^{-2}$





Irradiated with neutron to 1e15 $n_{eq}cm^{-2}$





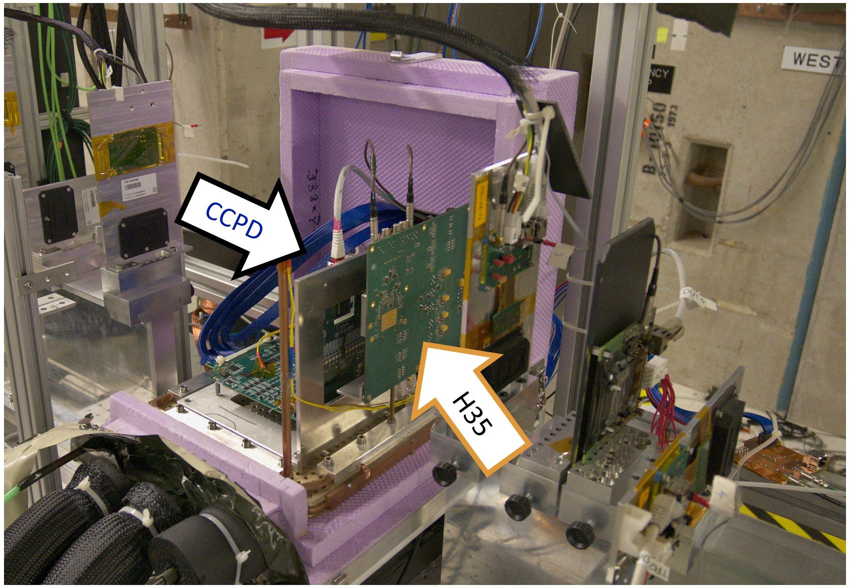
Beam test campaign in 2017

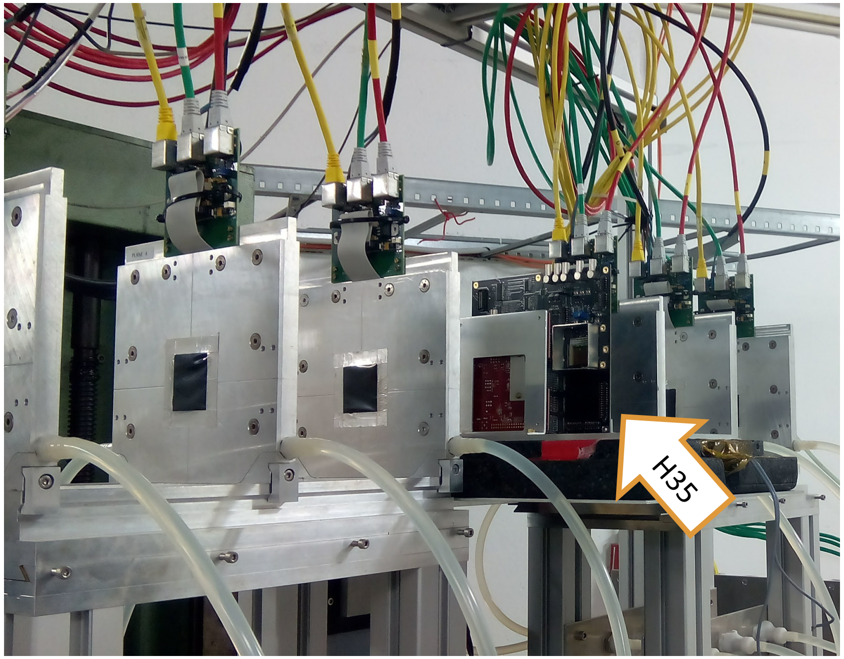
- Fermilab in April
  - 120 GeV protons
  - IFAE in collaboration with UniGe & Argonne Lab
  - UniGe FE-I4 telescope* + IFAE readout**
  - Not irradiated (20,80,200 Ωcm) + very first time irradiated 200 Ωcm

- CERN SpS in September
  - 180 GeV pions
  - IFAE in collaboration with UniGe
  - UniGe FE-I4 telescope* + IFAE readout**
  - 200 Ωcm neutron irradiated (@JSI) up to 1e15

- DESY in November
  - 4 GeV electrons
  - With ATLAS ITk group
  - EUDET telescope + IFAE readout**
  - 200 Ωcm neutron (@JSI) and proton (@KIT) irradiated up to 2e15

Analysis ongoing

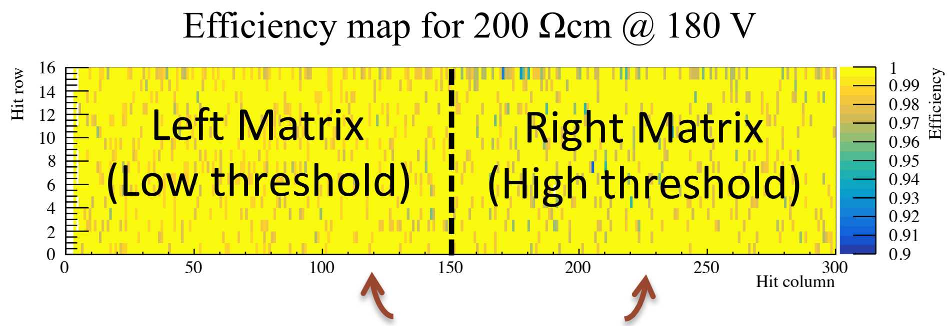




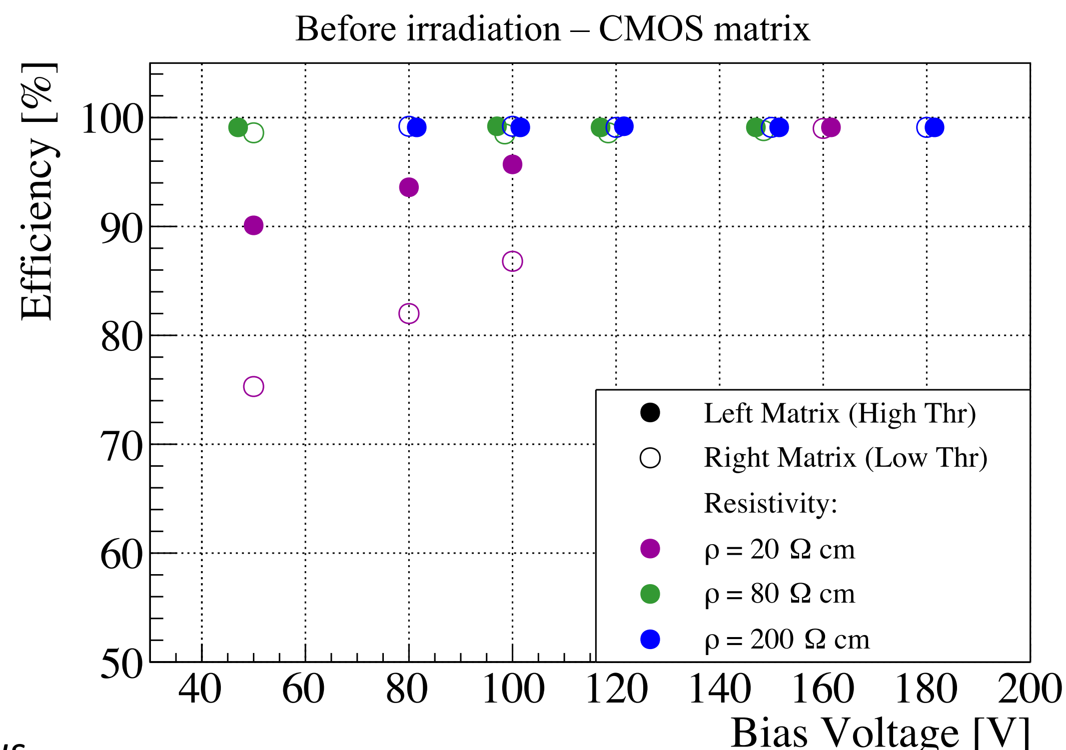
*M. Benoit et al., JINST 11 (2016) no.7, P07003
**S. Terzo et al., JINST 12 (2017) no.6, C06009

Hit efficiency results

- H35demo CMOS matrix:
  - Different resistivities:
    - 20 – 80 – 200 Ωcm
  - Thresholds ≈ 1300−1800 e
  - Analysis performed with the Proteus* framework



Efficiency calculated separately for the left and right part of the matrix due to the different off-pixel comparator settings



Efficiency of >99% for sensors with resistivity >= 80 Ωcm

20 Ωcm samples need about 160 V to reach full efficiency

*https://gitlab.cern.ch/unige-fei4tel/proteus

Efficiency results from SpS beam test

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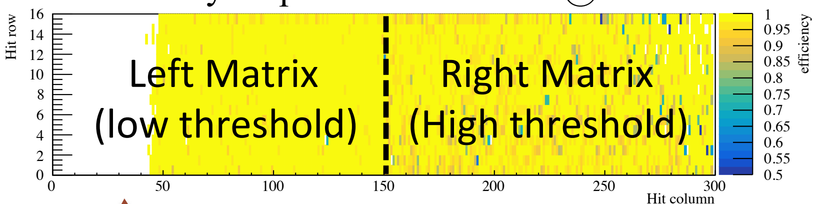
200 Ωcm sample irradiated with neutrons at JSI

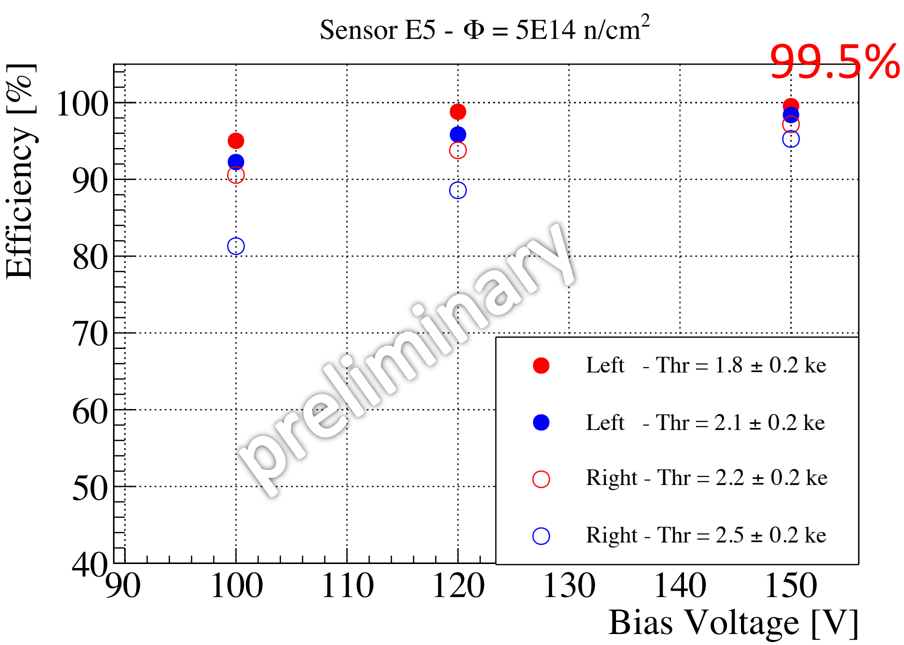
5e14 $n_{eq}cm^{-2}$

Depleted region of ≈50-60 μm at 120-150 V (from E-TCTs)

Efficiency map lowest threshold @ 150 V



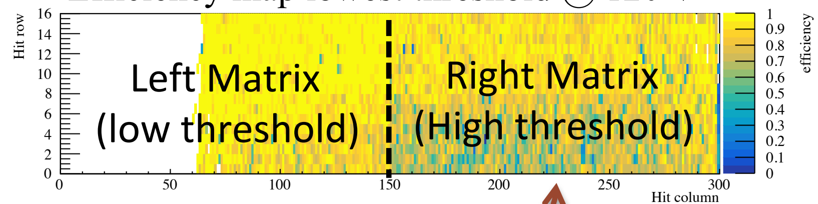
Cut due to the trigger window size



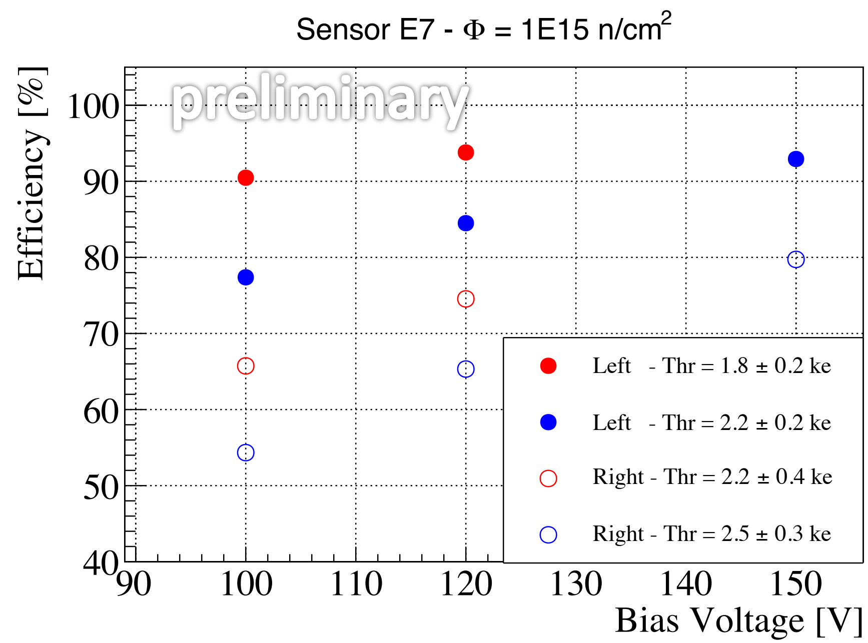
1e15 $n_{eq}cm^{-2}$

Depleted region of ≈60-70 μm at 120-150 V (from E-TCTs)

Efficiency map lowest threshold @ 120 V



Up/down asymmetry not yet understood



Efficiency results from SpS beam test

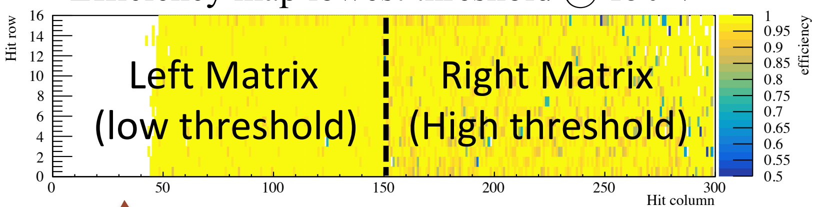
IFAE Institut de Física d'Altes Energies

200 Ωcm sample irradiated with neutrons at JSI

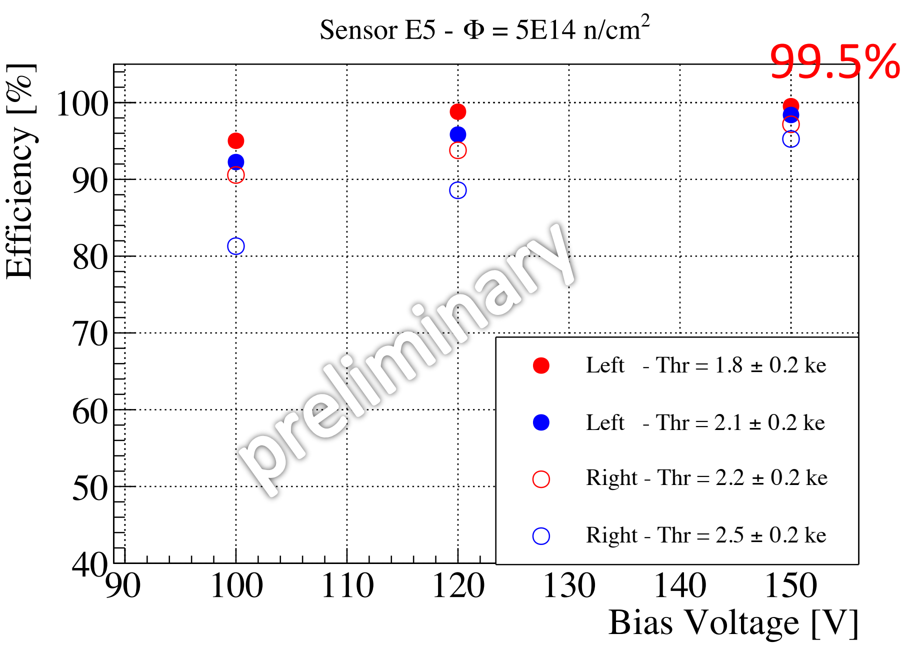
5e14 $n_{eq}cm^{-2}$

Depleted region of ≈50-60 µm at 120-150 V (from E-TCTs)

Efficiency map lowest threshold @ 150 V



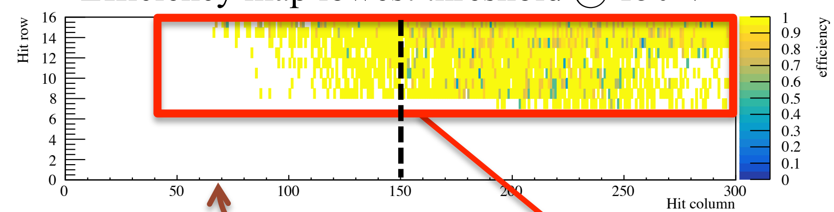
Cut due to the trigger window size



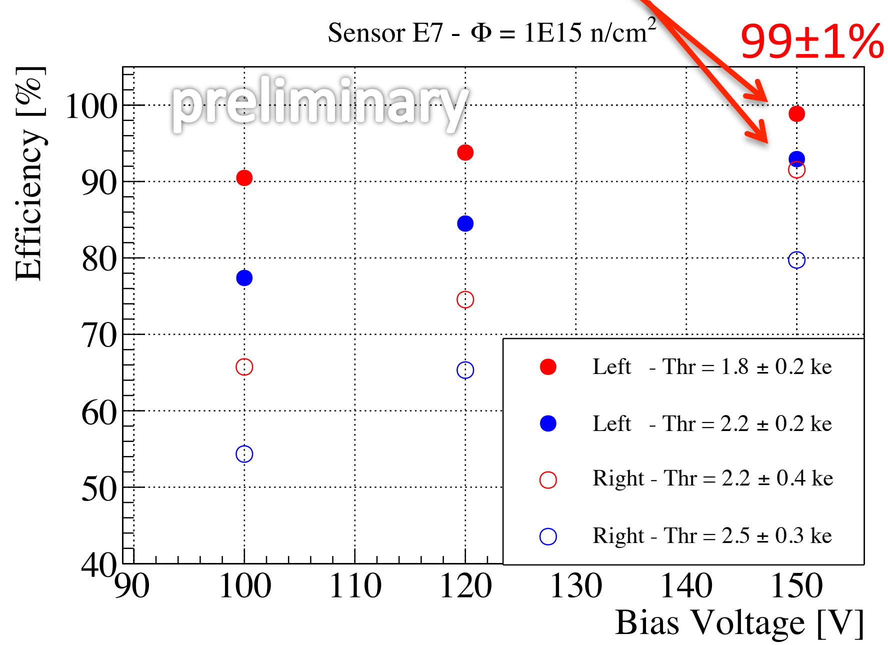
1e15 $n_{eq}cm^{-2}$

Depleted region of ≈60-70 µm at 120-150 V (from E-TCTs)

Efficiency map lowest threshold @ 150 V



Beam accidentally displaced

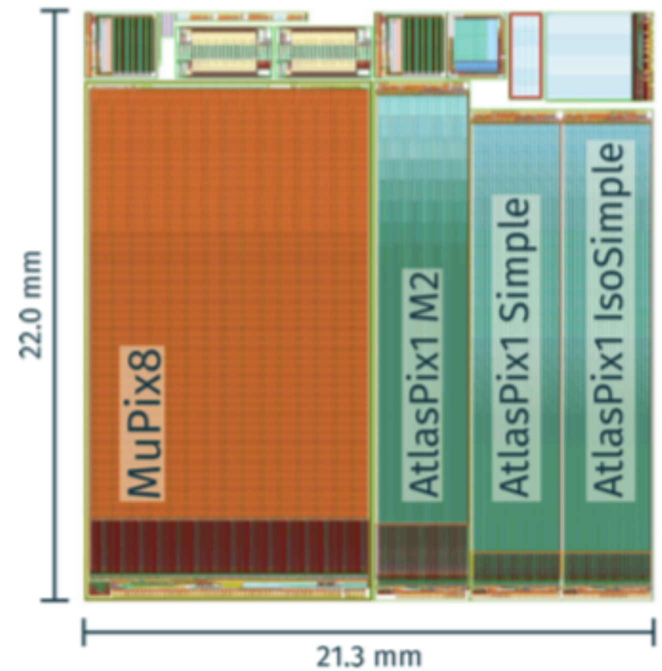


The ATLASPix prototype

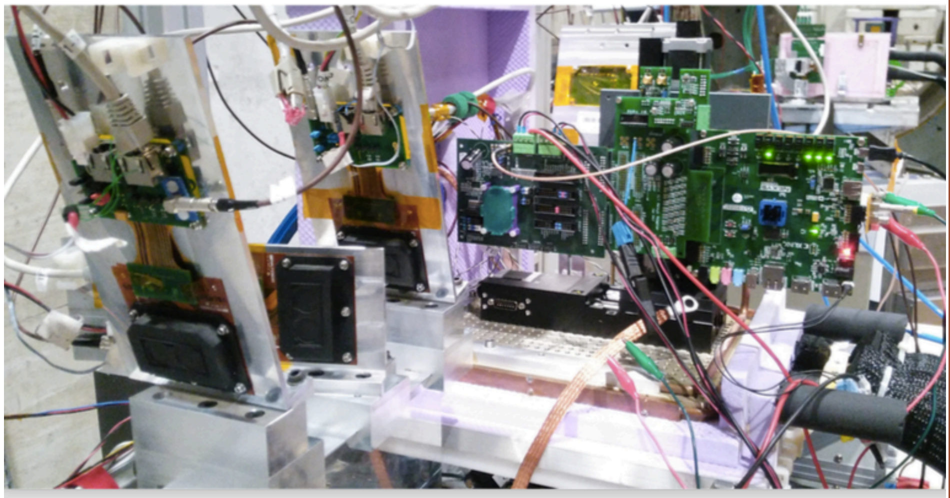
- Full scale monolithic prototype
  - AMS 180 nm CMOS process
  - Large fill factor
  - Designed at KIT, IFAE, Geneva, Heidelberg, Liverpool

- First Atlaspix1 chip:
  - M2 matrix:
    - Parallel-pixel-to-buffer architecture
    - 56x320 pixels
    - 60x50 μm^2 pitch
  - Simple & IsoSimple matrices
    - Column-drain architecture
    - 25x400 pixels
    - 130x40 μm^2 pitch

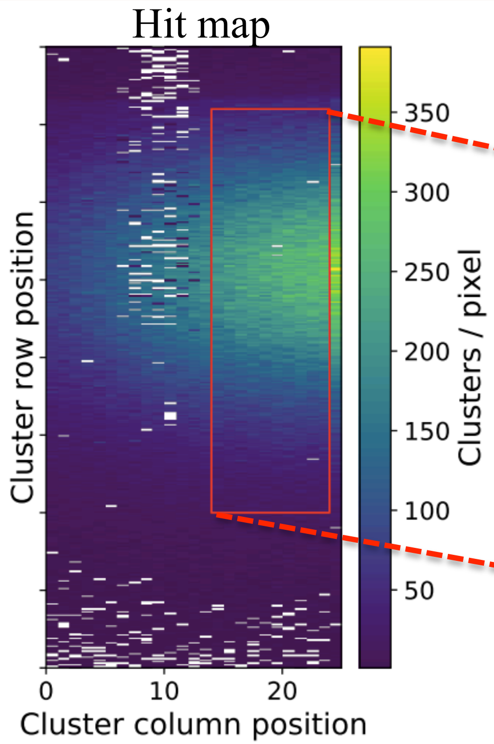
- First beam test of the Simple matrix
  - CERN SpS in November 2017
  - Collaboration of KIT and UniGe
  - UniGe FE-I4 telescope + KIT readout system
  - Chip operated at 10 MHz, 100 ns period



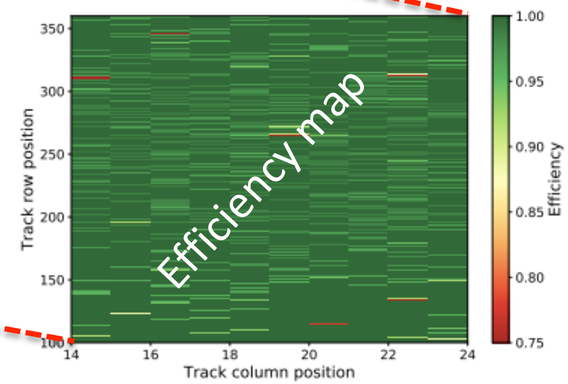
KIT DAQ system & Geneva telescope I. Peric et al.

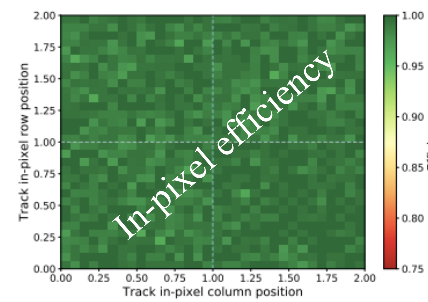


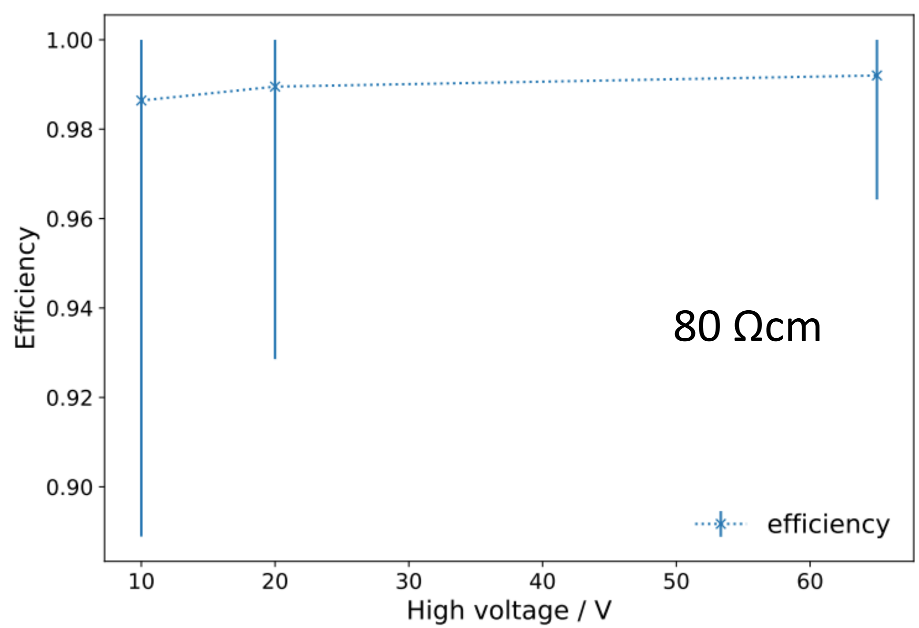
ATLASPix1: beam test results



- Region of Interest
  - Avoid tuning issues
  - Avoid low-statistic pixels







Efficiency of >99%

Already high efficiency at low voltage

Conclusion & outlook

- Characterization of the H35Demo chip
  - New readout system developed at IFAE for the monolithic matrices
    - ➢ Tuning and readout at 320 MHz clock (25 ns events)
  - Full efficiency measured before irradiation for chips with resistivity >=80 Ωcm with a bias voltage >= 50 V
- Result of irradiated fully monolithic HV-CMOS pixel detectors for
  - Measured 200 Ωcm samples after neutron irradiation to 1e15 $n_{eq}cm^{-2}$
    - ➢ High efficiency with a bias voltage >120 V and threshold of 1800 e
    - ➢ Preliminary results show the possibility of reaching an efficiency of about 99% operating the detectors with a bias voltage of 150 V
- First promising results before irradiation of the new AtlasPix1 chip

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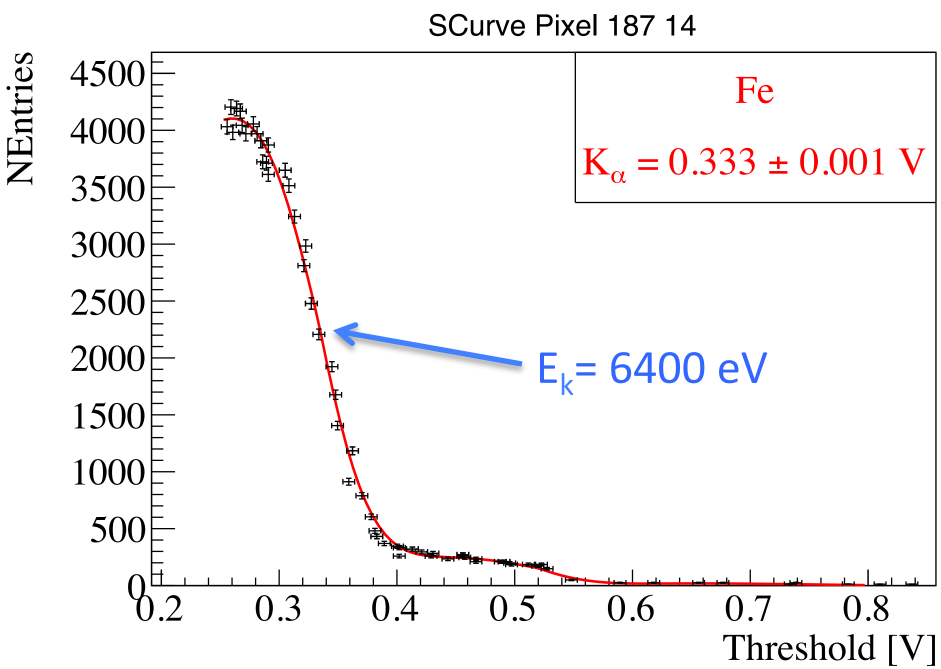
- What's next:
  - Analysis of H35Demo test beam @ DESY:
    - ➢ Neutron irradiated chips up to 2e15 $n_{eq}cm^{-2}$
    - ➢ Proton irradiated chips up to 1e15 $n_{eq}cm^{-2}$
  - Further characterization of the new ATLASPix designs in 180 nm before and after irradiation

Backup

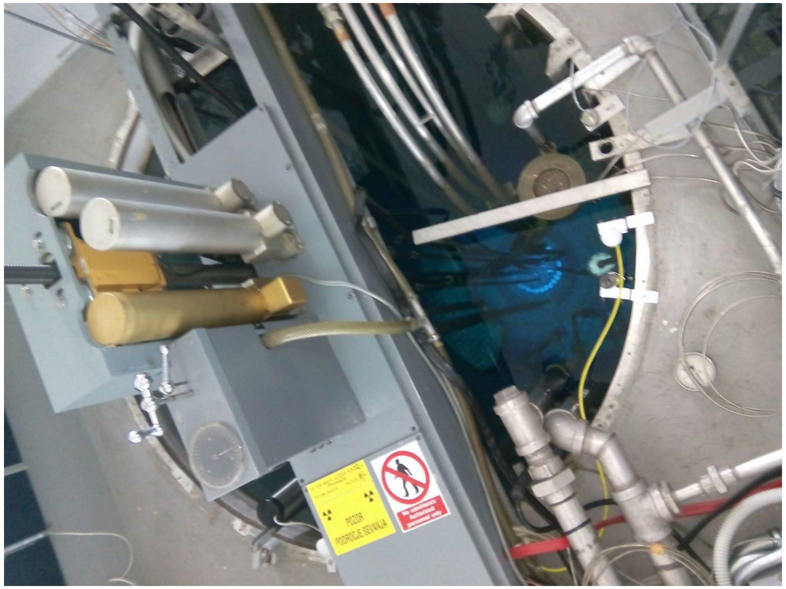
H35 injection capacitance measurement

- First estimation of the injection capacitance for the CMOS matrix of the H35DEMO chip was obtained from simulations: 0.84 fF
- Measured also with the X-ray fluorescence setup at CERN
  - Very first estimations in agreement with the simulated value



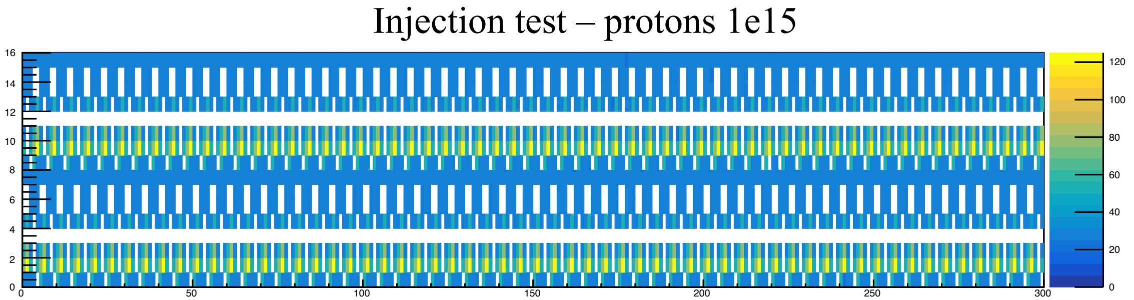
Further irradiations

- 200 Ωcm chips have been irradiated with neutrons in the TRIGA reactor in Ljubljana up to 2e15 $n_{eq}cm^{-2}$

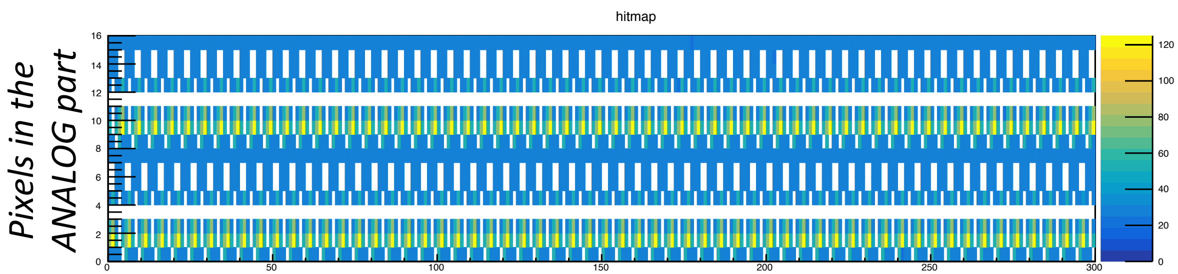


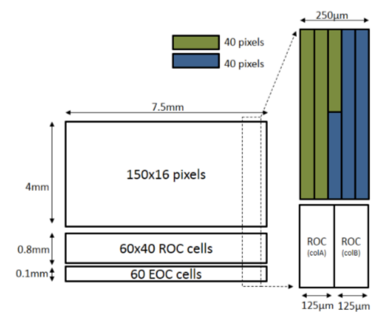
- And at KIT with 23 MeV protons up to 1e15 $n_{eq}cm^{-2}$

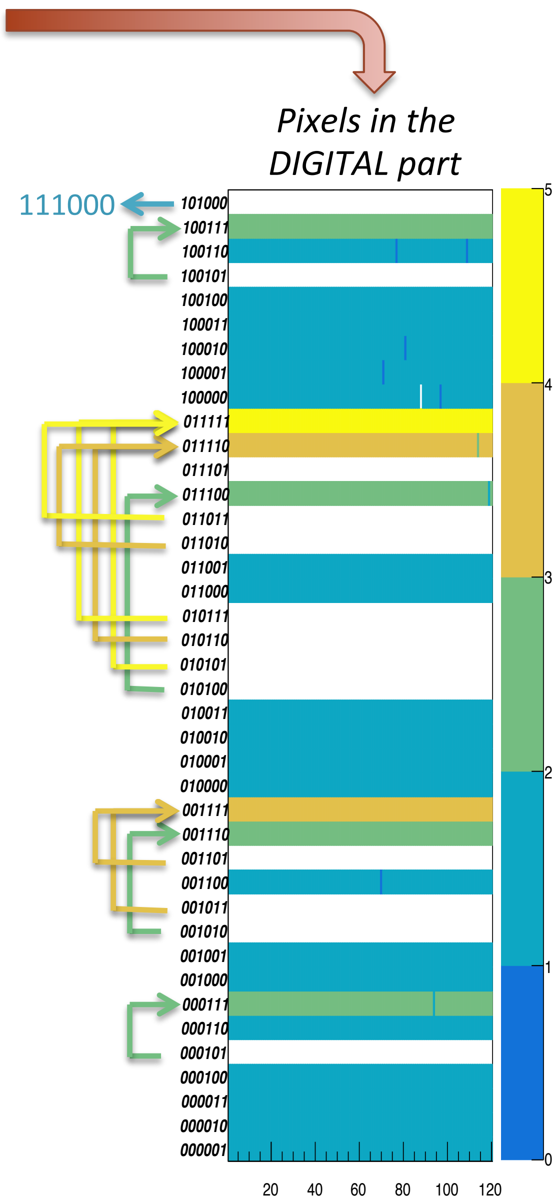
- We observed a digital pattern in the injection test:
  - After proton irradiation >=1e14 $n_{eq}cm^{-2}$
  - After neutron irradiation >=1e15 $n_{eq}cm^{-2}$ at low temperature
- The number of pixel misbehaving increases with the fluence and it is particularly enhanced for proton irradiations



Address crosstalk







- The 16x300 analog pixels in the CMOS matrix are connected one-to-one to 40x120 pixels in the digital periphery

- The addresses are generated in the periphery with adjacent transistors

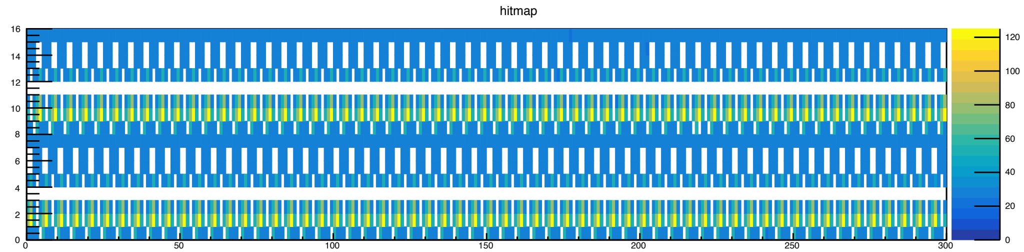
- Due to strong capacitive couplings between adjacent lines it is possible to have crosstalk between addresses

- This has been corrected in the design of the H18 ATLASPix1 by adding additional capacitors between the lines

1 0 1
1-> 0 <-1
1 1 1

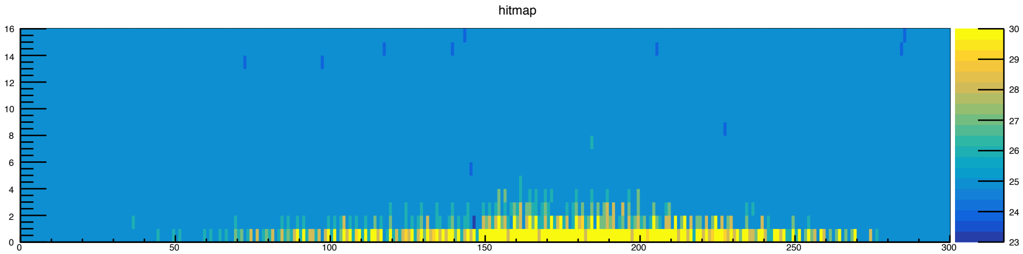
Solution

- Standard settings of the digital voltage: VDDD = 3.3V



- Increasing VDDD from 3.3V -> 5V

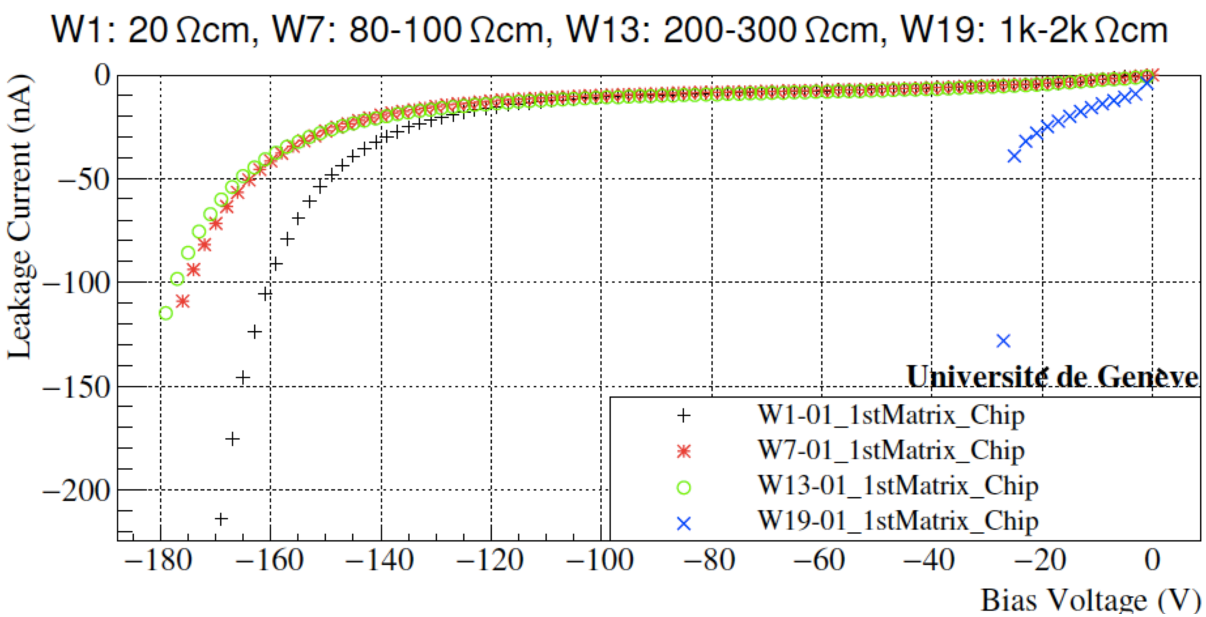
+1.7V

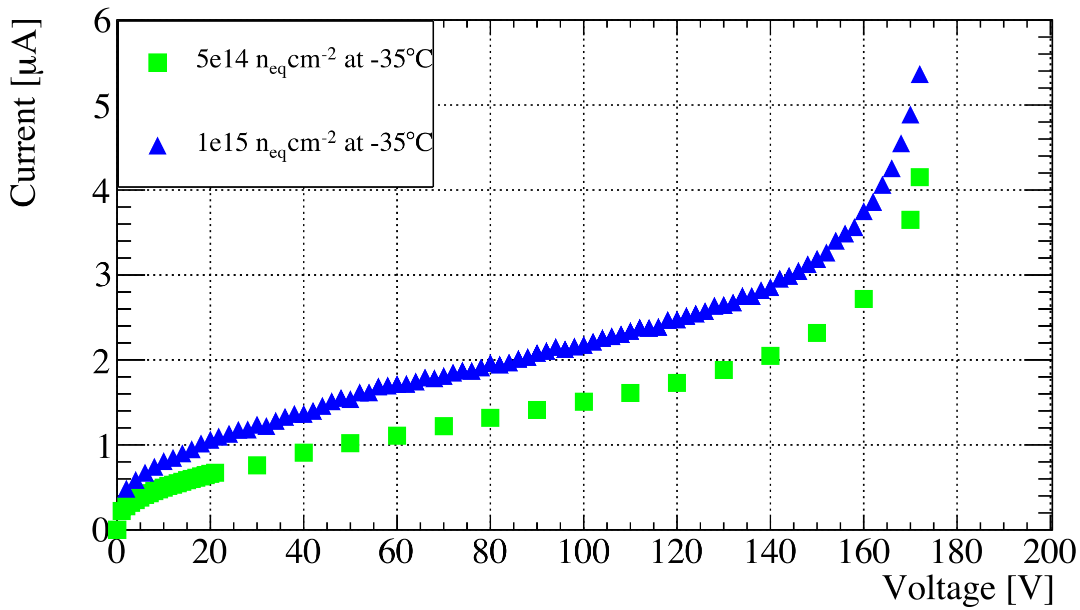


Noisy pixels in the first rows

- The digital voltage needs to be increased depending on the irradiation levels:
    - Proton irradiated samples require very high VDDD which lead to a noise increase
    - Neutron irradiated samples require instead moderate VDDD increase (less than 4V)

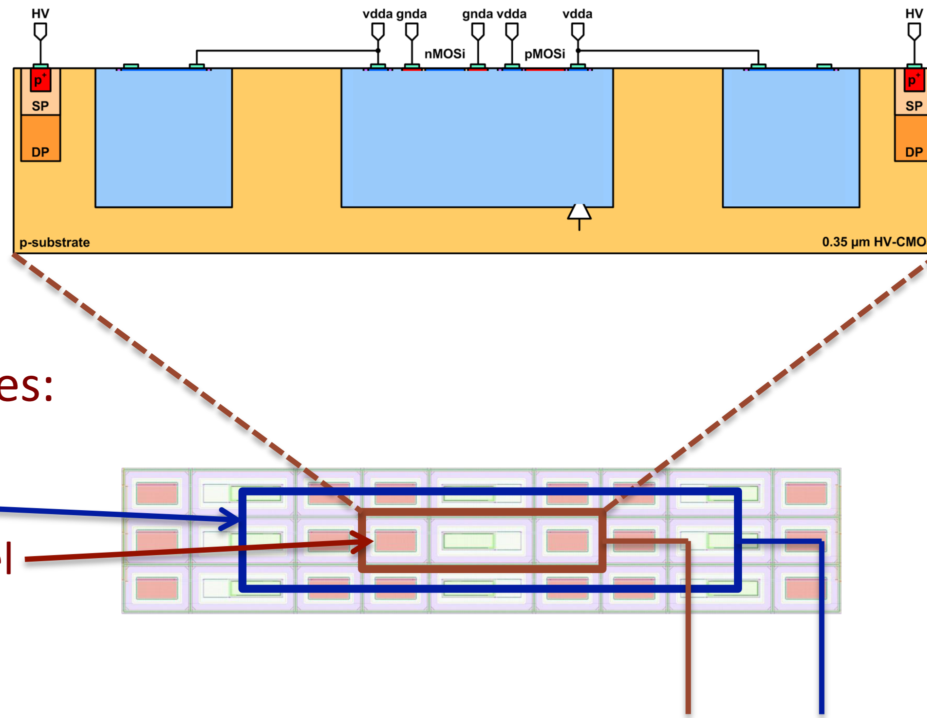
H35 – matrix IVs





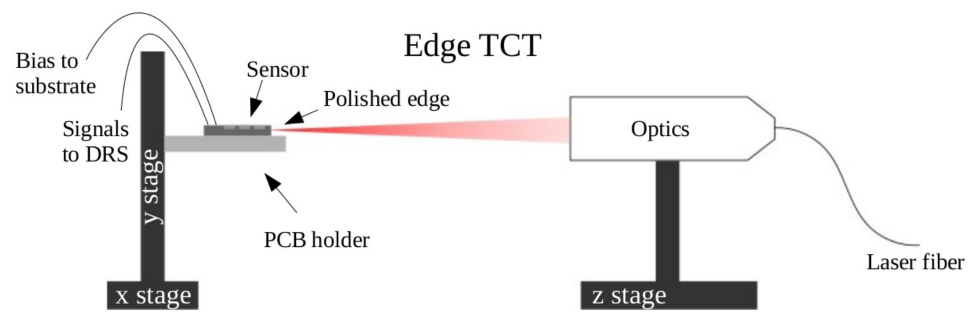
Sensor characterization

- H35 pixel cell structure
  - p-substrate + 3 deep n wells
    - ➢ Lower capacitance (noise, timing)
    - ➢ Reduce trapping
  - Bias from the top -> single sided



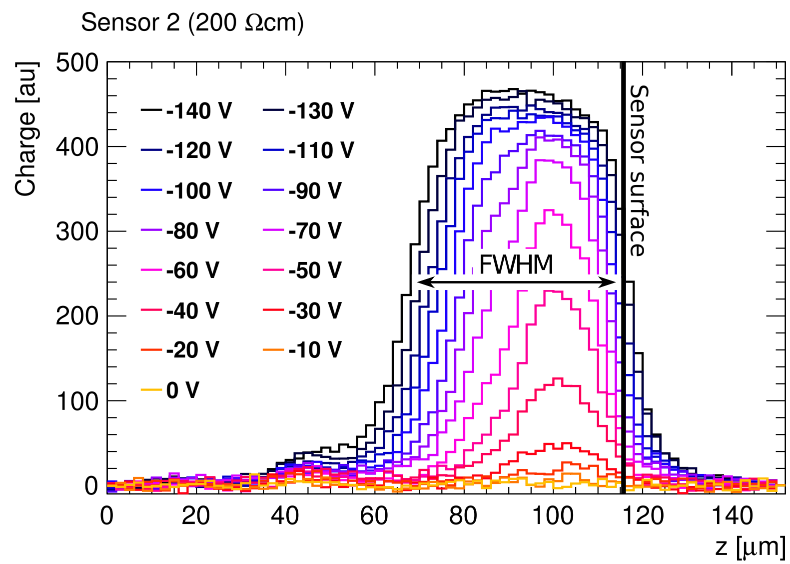
- Characterization of H35 test structures:
  - 3x3 pixel structures w/o electronics
  - External pixels shorted together
  - Separate readout of the central pixel
  - ρ= **80 Ωcm** – **200 Ωcm** – **1 kΩcm**

- The Edge-TCT setup:
  - Infra-red laser (1064 nm)
    - Beam spot about 10 µm FWHM
    - Pulses of about 500 ps
  - Readout: DRS4 evaluation board
    - 700 MHz bandwidth
    - 5 GSPS
    - 200 ns sampling depth
    - Four channels: 1 × trigger, 1 × beam monitor, 2 × readout



Depletion: before irradiation

- Depletion depth is defined by the FWHM of the charge collection profile

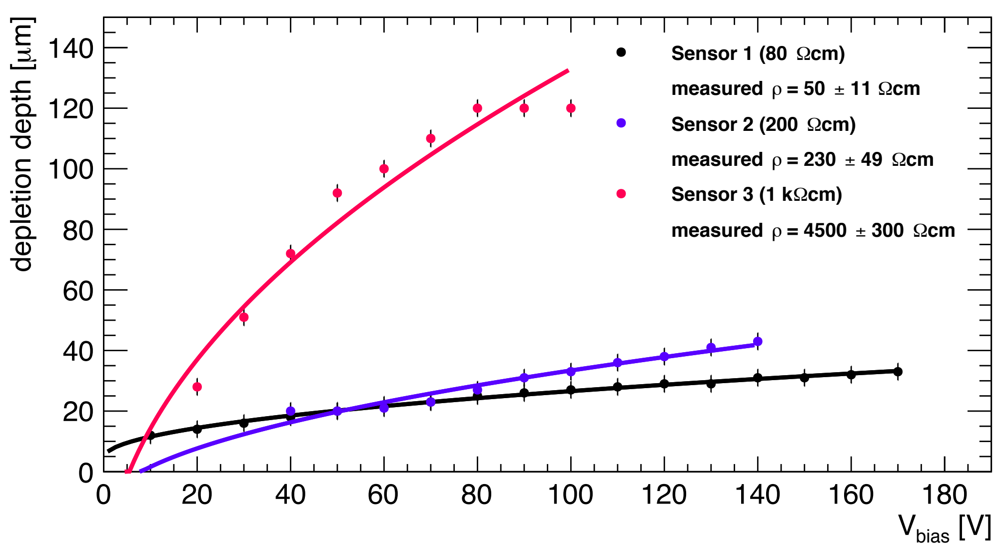


- Resistivity obtained fitting the depletion depth as a function of the bias voltages

$$d(V) = d_0 + \alpha\sqrt{\rho V}$$

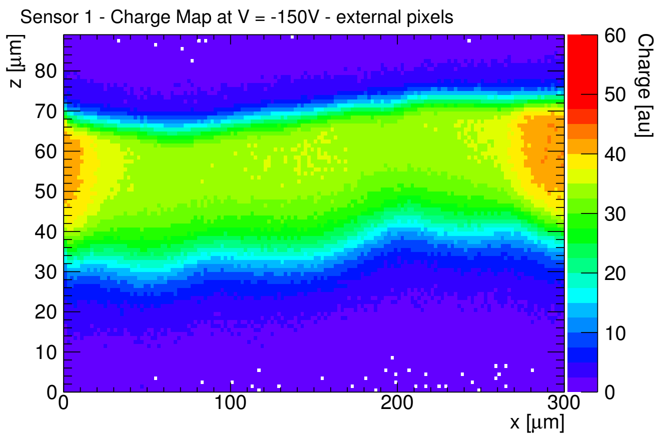
with $\alpha = \sqrt{2\varepsilon\varepsilon_0\mu}$

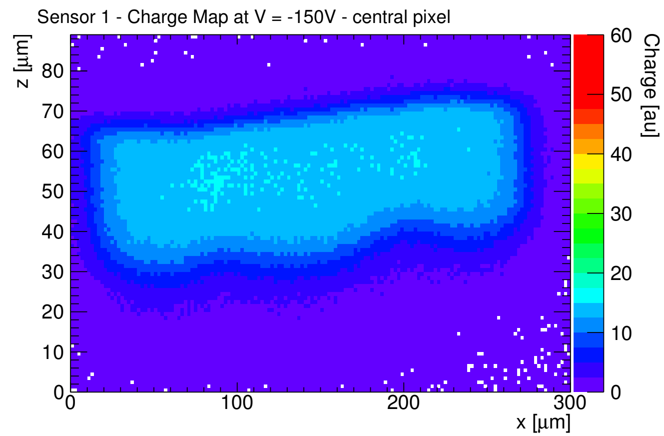
	ρ nominal	ρ measured
Sensor 1	80 Ωcm	50 ± 11 Ωcm
Sensor 2	200 Ωcm	230 ± 49 Ωcm
Sensor 3	1000 Ωcm	4500 ± 300 Ωcm

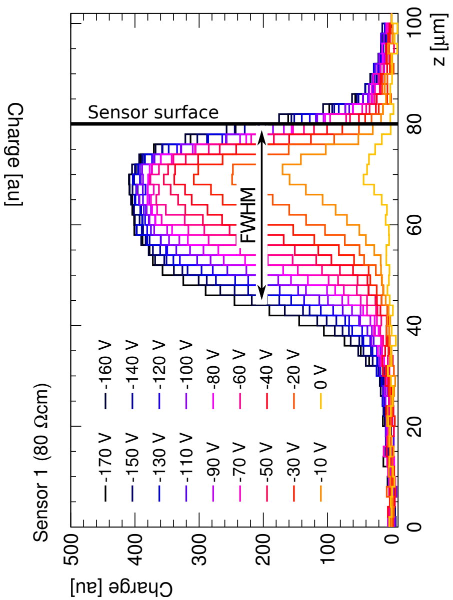


Depletion: before irradiation

80 Ωcm



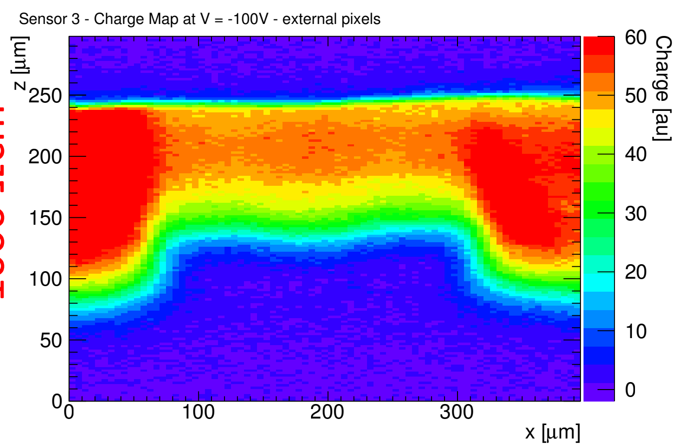


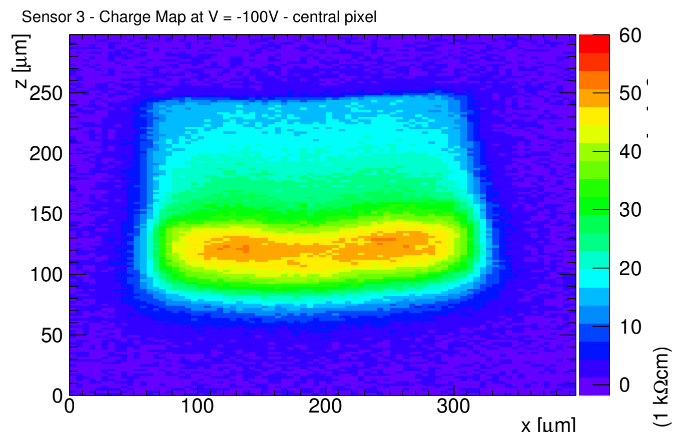


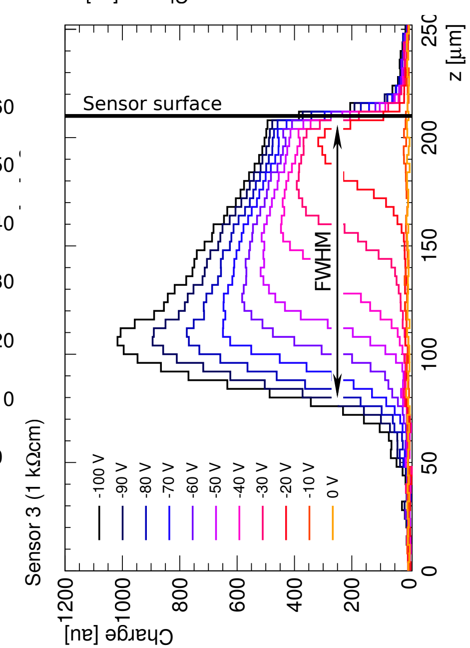
External pixels

Central pixel

1000 Ωcm



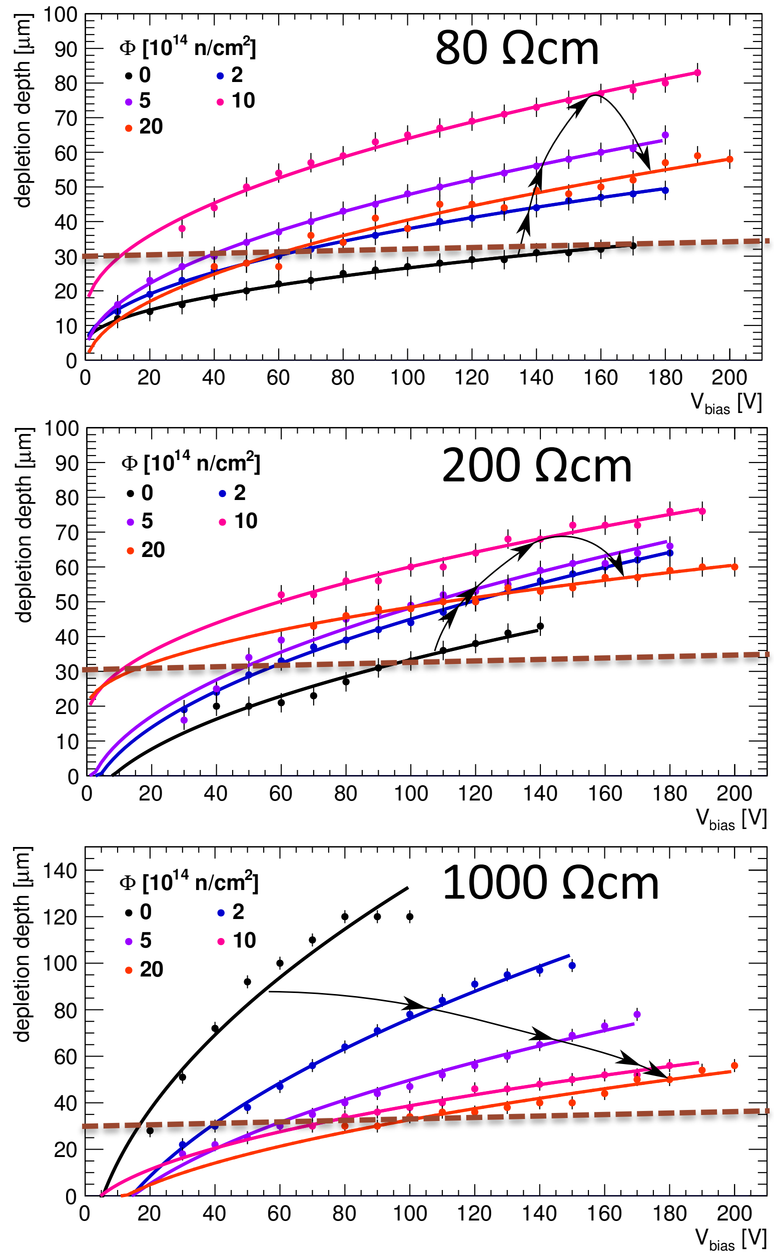




When depletion gets larger of 100 µm the central pixel starts to collect charge from the neighboring pixels

Depletion: after irradiation

- Irradiation at the TRIGA neutron reactor at JSI, Ljubljana:
  - Now: **2e14**, **5e14**, **10e14**, **20e14** $n_{eq}cm^{-2}$
  - Next steps: 5e15 and 1e16 $n_{eq}cm^{-2}$
- Acceptor removal effect visible for lower substrate resistivities which leads to an increase of the depletion depth after irradiation up to 2e15 $n_{eq}cm^{-2}$
- Due to the low initial acceptor concentration in the 1000 Ωcm sample the creation of stable acceptors dominates and the depletion depth decreases after irradiation

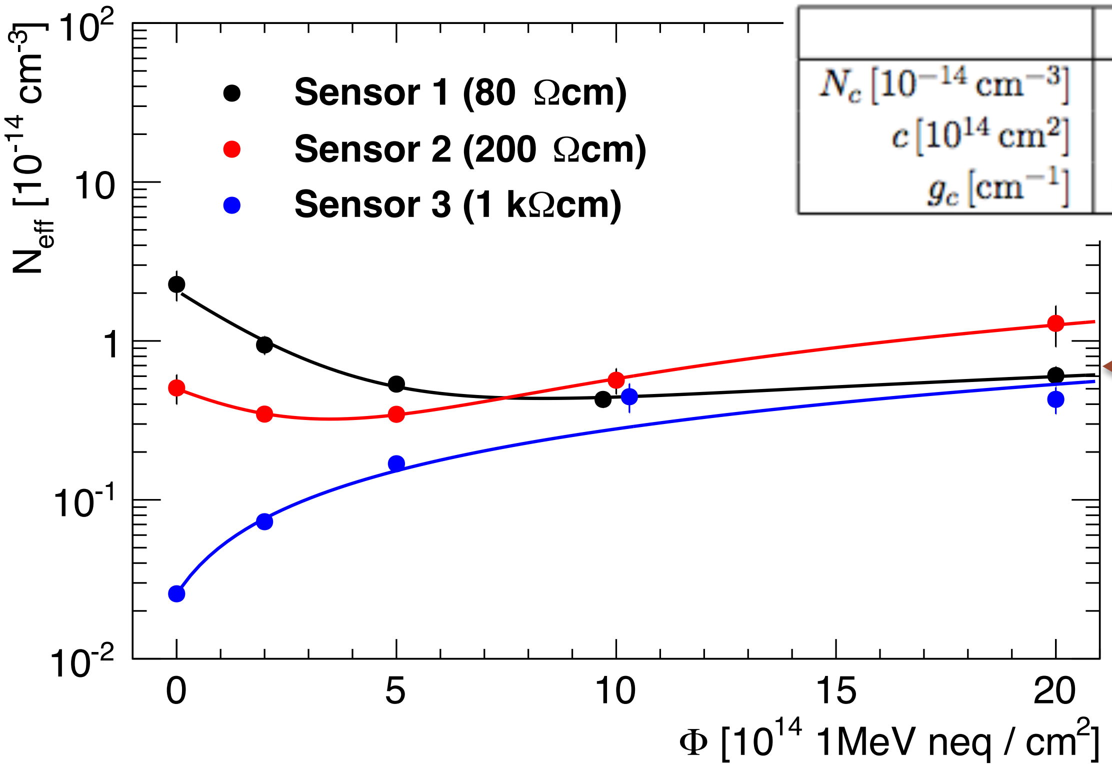


Effective doping concentration

- Effective doping concentration obtained from:

$$d(V) = d_0 + \alpha\sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V}$$

$$N_{eff} = \underbrace{N_{eff0}}_{\text{Initial doping}} - \underbrace{N_c \cdot (1 - exp(-c \cdot \Phi_{eq}))}_{\text{Acceptor removal}} + \underbrace{g_c \cdot \Phi_{eq}}_{\text{Acceptor introduction}}$$

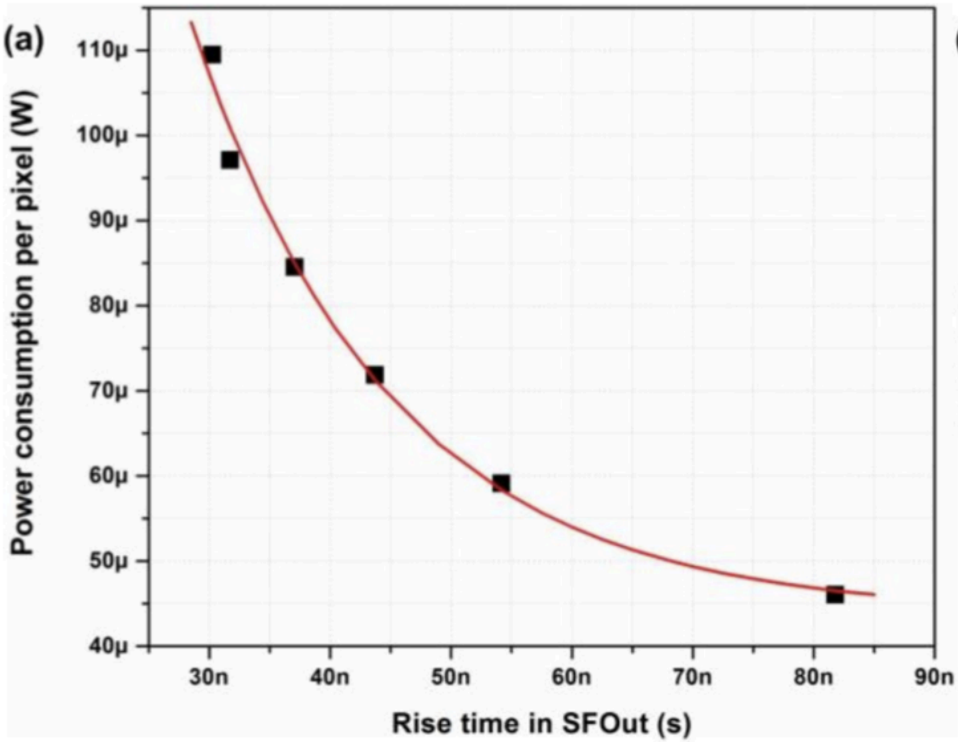


	Sensor 1	Sensor 2	Sensor 3
$N_c\,[10^{-14}\,\mathrm{cm}^{-3}]$	1.8 ± 0.4	0.7 ± 0.5	–
$c\,[10^{14}\,\mathrm{cm}^2]$	0.5 ± 0.2	0.3 ± 0.3	–
$g_c\,[\mathrm{cm}^{-1}]$	0.02 ± 0.01	0.07 ± 0.04	0.03 ± 0.02

After about 1e15 n_{eq}/cm^2 N_{eff} tends to the similar values for all resistivities

E.Cavallaro et al., JINST 12 (2017) no.01, C01074

Power vs. rise time



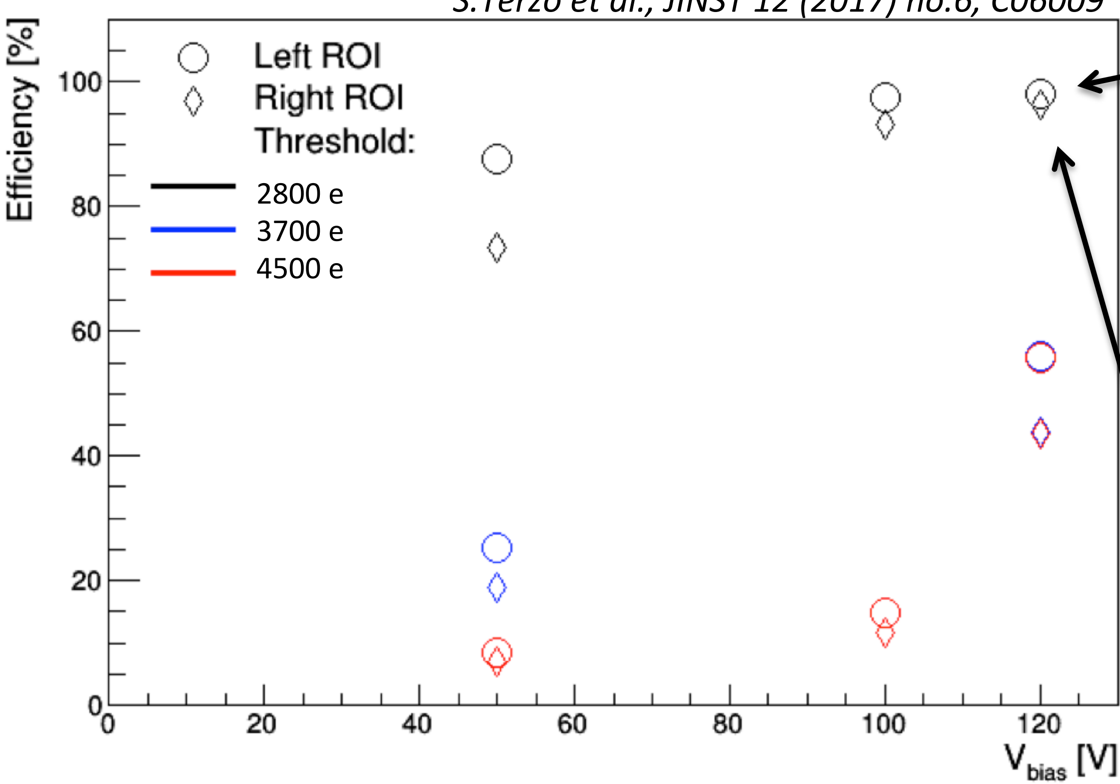
- Simulation of the power consumption as a function of the rise time for analog pixels with high gain
- For low gain pixels (-p-tub +extra capacitor) the rise time can go down to 20 ns with aggressive settings

E. Vilella et al. JINST11 (2016) C01012

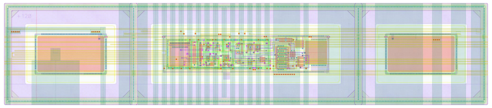
Test beam @ SpS in 2016

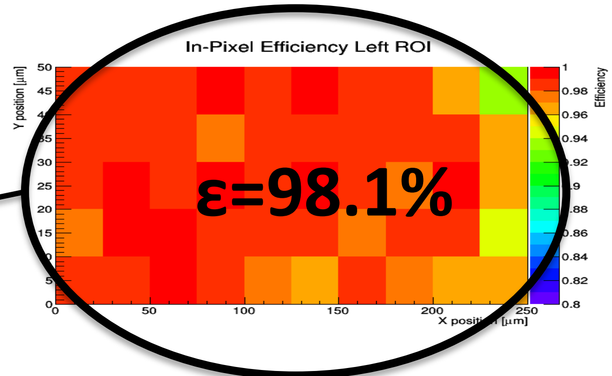
- Efficiency saturation depends on the threshold
  - Higher threshold requires more bias
    ➔ increase the depletion depth
- Higher efficiency in the left matrix
  - Mean threshold right > mean threshold left
  - Right matrix: efficiency lost close to pixel edges

S.Terzo et al., JINST 12 (2017) no.6, C06009

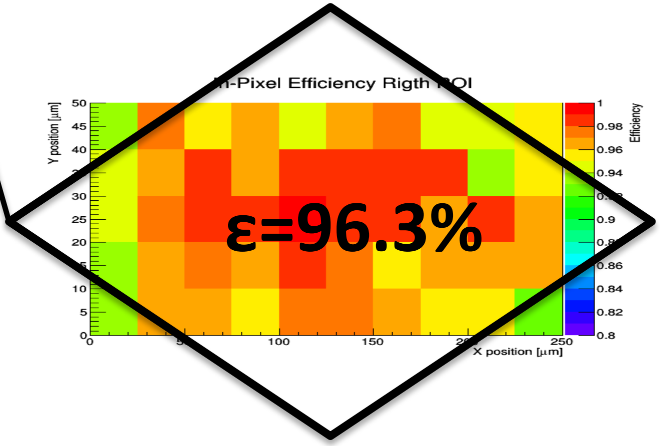


In-pixel efficiency maps
at 120 V and Thr: 2800 e





Left matrix



Right matrix