TCAD simulation of RD53A compatible pixel cells and sensor productions by MPP

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Max-Planck-Institut für Physik (Werner-Heisenberg-Institut)

Overview



1. TCAD simulation of RD53A compatible pixel cells

- optimization of pixel implant size
- looking at AC simulations to simulate pixel capacities
- CCE before and after irradiation

2. Sensor productions by MPP

- SOI4 production at MPG-HLL
- development of temporary metal for quality assurance

3

Introduction ATLAS ITk upgrade

Inner Tracker (ITk) upgrade in preparation for the ATLAS experiment facing the High Luminosity phase of the Large Hadron Collider (HL-LHC)

- harsher conditions leading to
 - higher track density: smaller pixel cells to keep a low occupancy
 - **higher fluence**: thin sensors improve radiation hardness
 - → Simulate thin sensors with small pixels for design optimisation
- punch-through (PT) structures to test sensors before interconnection induce significant performance degradation after irradiation

→to enable testing for final productions replace PT by a temporary metal technology





of RD53A compatible pixel cells

- use a 3D TCAD model for the investigation of properties of small pixel cells with different implant sizes
- because of symmetry, simulation of ¼ pixel is sufficient
 - four quarter pixels used in this study allowing for correct description of Ramo potential and inter-pixel capacitance
- investigate IV / CV / CCE of different implant sizes
 - radiation damage simulated with Perugia 2017 model¹ (1x10¹⁵ n_{eq}/cm²)
 - bulk damage: 2 acceptor, 1 donor trap, different e/h cross sections and introduction rates
 - surface damage: fixed oxide charge of 5×10¹⁰cm⁻² for not-irradiated and 1×10¹²cm⁻² for irradiated sensors
 - interface traps according to Perugia 2017 model



² F. Moscatelli et al., Combined Bulk and Surface Radiation Damage Effects at Very High Fluences in Silicon Detectors: Measurements and TCAD Simulations

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structure of interest





high resistivity p-type bulk material (5×10^{12} cm⁻³)





















influence of implant size: general



- the new RD53 read-out chip will have a $50 \text{x} 50 \mu \text{m}^2$ grid
 - pixel implant size and shape can be modified within this boundary condition
- larger implants theoretically:
 - + have higher breakdown voltages
 - + have better charge collection efficiency
 - have higher inter-pixel capacity (-> higher noise)





influence of implant size: breakdown behaviour



IV, $\Phi = 0$, Comparison of pixel sizes



- larger pixel implants shield the p-spray from the backside potential
 - smaller potential difference between pspray and pixel implant
 - higher breakdown voltage



influence of implant size: pixel capacity





- minimal threshold (600e) is guaranteed up to 50 fF
- inter-pixel capacity outweighs pixel-bulk capacity by far
 - inter-pixel capacity determined by implant size and p-spray doping concentration





-> measurements indicate capacity between 20-40 fF

C2V, $\Phi = 0$, pixel capacity 40um implant

- charge collection before irradiation is equal for all implant sizes from 25-45µm after depletion
- at low voltages, significantly more charge collected by larger pixel implants
- larger pixel implants have earlier depletion voltages





TCAD Simulation influence of implant size: charge collection efficiency

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- larger pixel implants have earlier depletion voltages
- 10µm shows that very small pixel cells can not be used due to much later depletion







influence of implant size: charge collect

- charge collection before irradiation is equal for all implant sizes from 25-45µm after depletion
- at low voltages, significantly more charge collected by larger pixel implants
- larger pixel implants have earlier depletion voltages
- 10µm shows that very small pixel cells can not be used due to much later depletion
- charge amplification at 45V for 10 μ m implant size



charge collection efficiency after irradiation

25-45µm

- no difference between 50 and 200V
- small differences at 25V
 - larger implants beneficial
- very small differences at 250V
 - smaller implants beneficial (charge multiplication)





charge collection efficiency after irradiation

25-45µm

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10µm

- much lower collected charge below 100V
- charge multiplication above 100V



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Sol4 production at MPG-HLL





- latest production at MPG-HLL: SOI4
- 4 wafers (100 μ m) and 5 wafers (150 μ m) in SOI technology
- production to investigate:
 - different bias rail potential
 - RD53 compatible geometries
 - $25x100 \ \mu m^2 \ / \ 50x50 \ \mu m^2$
 - PT and PT with Al overhang and no PT
 - 250 μm / 450 μm edge
 - FE-I4 compatible quad sensors
 - process optimization: p-spray concentration
 - temporary metal technology



Sensor productions by MPP





temporary metal technology

Standard:

- copper is used as UBM as it is very reliable and well known
- copper is electroplated on a seed-layer of TiW in openings of a photoresist layer
- photoresist and TiW are removed after finishing the process New:
- TiW is patterned after copper deposition to cover only the active area of the sensor
- a needle in the TiW layer connects to all pixels
- a standard etching after testing removes the TiW layer





 TiW in the pixel matrix, no TiW elsewhere



 etching the TiW layer away leaves isolated pixels behind

for most of the structures: before/after • variations compatible with typical spread between repeated measurements

• will have to wait for structures without PT flip-chipped to read-out chips for final conclusions

- disentangle
- interplay of PT and TiW is difficult to
- no significant failure detected before or after removal of TiW
- so far only structures with PT could be tested after removal of TiW since the wafers are still to be diced and flipchipped
- ×10* Current [A] With TiW layer Wafer 6 50×50µm² split BR 50×50µm² float BR 25×100um² float BR 25×100µm² around BR With punch through 50×50µm² split BR 50×50um² float BR 25×100um² float BR 25×100um² around BR

100

150

200

Sensor productions by MPP temporary metal technology





Wafer 7



×10

With TiW laver

50×50µm² split BR 50×50µm² float BR

25×100um² float BR

With punch through

50×50µm² split BR 50×50µm² float BR

25×100µm² float BR

25×100um² ground BR

25×100um² ground BR

90E

80Ê

70F

Durrent [A]



Sensor productions by MPP Outlook: SOI5 production





- SOI5 production at HLL with ~20 wafers
- processing identical to SOI4:
 - Cu UBM and BCB deposition at HLL
 - thinning and dicing at IZM
 - low-dose p-spray for whole production
- focus on RD53A compatible sensors:
 - 6 pseudo-quad sensors
 - $25x100\mu m^2$ and $50x50\mu m^2$ pixel cells
 - mostly without PT -> use TiW testing method
 - PT sensors have floating/split/grounded bias rail
 - different implant sizes to validate the simulations



Summary & Outlook



- TCAD simulation of RD53A compatible pixel cells
 - larger pixel implants lead to lower depletion voltages, thus collecting more charge after irradiation at the same voltage
 - effect at $1 \times 10^{15} n_{eq}/cm^2$ smaller than expected, what will happen at higher fluences?
 - measurements on RD53A modules and test-structures planned
 - capacity drastically increasing for increasing implant size
 - dependence of noise on input capacity of RD53A will determine the signal-to-noise ratio
- sensor productions at MPP
 - several design possibilities will be evaluated with the latest productions SOI4/5
 - new testing technique for sensors without biasing structure is being developed to avoid charge losses after irradiation









Noise vs input capacity

A. Andreazza,

Progresses on the ATLAS pixel detector, Nuclear Instruments and Methods in Physics Research Section A, Volume 461, Issues 1–3, 2001, Pages 168-171,







• text



Title subtitle





-600

-500

-300

-400

-200





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