Status of 3D Detector Development at SINTEF for ITk Upgrade

Ozhan Koybasi¹, Marco Povoli¹, Angela Kok¹, Anand Summanwar¹, Lars Breivik¹, Trond Hansen¹, Nicolas Lietaer¹, Ole Rohne², Heidi Sandaker²

¹ Microsystems and Nanotechnology (MiNaLab), SINTEF Digital
²HEPP, University of Oslo
The most advanced laboratory in Norway for micro- and nanotechnology, situated on the campus of University of Oslo

- Clean room facilities of 800 m²
- General cleanroom area of class 1000 and mini environments of class 10 for sensitive processes
- Complete Si processing line for 150 mm (6 in) wafers with state-of-the-art production equipment
- Another line for Non-CMOS compatible materials
- Throughput of 10,000 wafers per year
- ISO 9001-2008 (Quality Management system) and ISO 14001-2004 (Environmental Management system) certified
EQUIPMENT and KEY PROCESSES

- High temperature processes in furnaces at 400 - 1200 °C (thermal oxidation, gas phase doping, annealing, LPCVD of SiN and polysilicon)

- Deposit various thin layers on the surface (sputter, PECVD, PLD, ...)

- Etch thin layers (RIE, wet etch)

- Making patterns on the wafers (automated photolithography line, NIL)

- **Etch 3-dimensional structures in the silicon wafer (state of the art DRIE, anisotropic wet etch)**

- Various characterization equipment (4-point probe, automatic inspection, probe stations, ellipsometer, interferometer, profilometer, SEM)

- SEM, WLI, automated wafer prober/visual inspection, probe stations, ellipsometer, profilometer4-probe)

- Bond wafers to form a stack (anodic, fusion, metal, adhesive)

- Packaging (wafer dicing, wirebonding)

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## History of 3D detector development @SINTEF for HEP

<table>
<thead>
<tr>
<th>Year</th>
<th>Project</th>
<th>Wafer</th>
<th>Sensor thickness</th>
<th>Hole (3D electrode) diameter</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006</td>
<td>Run 1</td>
<td>4” SOI</td>
<td>230µm</td>
<td>~15µm</td>
<td>N-type wafers, most wafers broke</td>
</tr>
<tr>
<td>2008</td>
<td>Run 2</td>
<td>4” SOI</td>
<td>230µm</td>
<td>~15µm</td>
<td>Reasonably good yield (~50%)</td>
</tr>
<tr>
<td>2010</td>
<td>Run 3</td>
<td>4” SOI</td>
<td>230µm</td>
<td>~15µm</td>
<td>Only 2 out of 24 wafers worked</td>
</tr>
</tbody>
</table>
| 2017 | Run 4*  | 6” Si-Si| 50µm 100µm  | ~4µm                         | • Completed in December 2017  
• Yield factors in previous run identified and resolved  
• Very good electrical characteristics and yield |
| 2018 | Run-5*  | 6” Si-Si| 100µm 150µm  | ?                            | Fabrication will commence in Spring 2018 |

*Funding from Norwegian ATLAS R&D*
Other relevant R&D activities

- Edgeless and slim edge detectors
- 3D silicon microdosimeters
- Through silicon vias (TSV) and 3D neutron detectors
## 3D Detector Run-4: Layout

<table>
<thead>
<tr>
<th>Sensor type</th>
<th>Description</th>
<th># of sensors</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE-I4_1</td>
<td>Standard IBL (2E, active edge incl. bias pad)</td>
<td>16</td>
</tr>
<tr>
<td>FE-I4_2</td>
<td>2E, active edge excl. bias pad</td>
<td>2</td>
</tr>
<tr>
<td>FE-I4_3</td>
<td>1E, punch-tru bias return</td>
<td>2</td>
</tr>
<tr>
<td>FE-I3</td>
<td>3E</td>
<td>4</td>
</tr>
<tr>
<td>RD53</td>
<td>50x50µm², 1E</td>
<td>2</td>
</tr>
<tr>
<td>FE-65</td>
<td>50x50µm², 1E</td>
<td>16</td>
</tr>
<tr>
<td>CMS</td>
<td>2E</td>
<td>4</td>
</tr>
<tr>
<td>Medipix</td>
<td>55x55µm², 1E</td>
<td>4</td>
</tr>
<tr>
<td>Strip</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>Planar diode</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>Edgeless planar diode</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>3D diodes</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Run-4 Layout: FE-I4

**Standard FE-I4 (IBL, 2E)**

- Standard FEI4 geometry and bump pattern (pixel size 50x250µm²)
- 2E configuration, 67 µm electrode distance
- Active edge, enclosing bias pad

**FE-I4 punch-tru bias return (1E)**

- Standard FEI4 geometry and bump pattern
- 1E configuration, 130 µm electrode distance
- Active edge
Run-4 Layout: CMS, Medipix, FE-I3

<table>
<thead>
<tr>
<th></th>
<th>CMS</th>
<th>Medipix</th>
<th>FE-I3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size (µm²)</td>
<td>100x150</td>
<td>55x55</td>
<td>50x400</td>
</tr>
<tr>
<td># of N+ electrodes per pixel</td>
<td>2E</td>
<td>1E</td>
<td>3E</td>
</tr>
<tr>
<td>N+ to P+ pitch (µm)</td>
<td>63</td>
<td>39</td>
<td>71</td>
</tr>
<tr>
<td>Edge design</td>
<td>All feature active edges</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Run-4 Layout: RD53

Features:
- $50 \times 50 \, \mu m^2$ cell
- 1E configuration
- $400 \times 192$ pixel matrix
- double width edge column
- active edge, excluding bias pad

Also smaller $64 \times 64$ FE65-style matrix
Run-4: Substrate and processing

- 6" Si-Si wafers
- 100 µm and 50 µm sensor thicknesses
- Active edge
- ~4 µm DRIE holes
- Full p-type, partial n-type electrodes

11 wafers completed
All processing steps except p-spray doping carried out in-house
Key processing steps

1. Si-Si wafer with p-spray

2. DRIE of n-type columns

3. Phosphorus doping and polysilicon filling

4. Phosborous doping of surface

5. DRIE of p-type columns and active edge

6. Boron doping and polysilicon filling

7. Boron doping of surface

8. Metallization

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Processing challenges and lessons learned

• Make sure DRIE mask robust enough to survive the harsh DRIE process
  - Limit the duration of DRIE to ~1 hour (design dimensions accordingly)

• Make sure trench corners are rounded in the design
  - Otherwise, larger opening and incomplete removal of polysilicon at corners

• Selective removal of polysilicon residues on wafer surface with photomasks
  - better control on yield
  - minimal re-opening of holes and trenches during surface polysilicon removal

• Further design optimizations to facilitate processing and measurements
Temporary metal test results: 3D Diodes (pre-and post-sintering)

Leakage current drops significantly after sintering!
Temporary metal test results: FE-I4

Criteria:

- $I_{\text{leakage}}@25V < 2\mu A/cm^2$
- $V_{\text{breakdown}} > \sim 50V$

Overall FE-I4 yield (11x20=220 sensors): 73%!

Metal not sintered
Temporary metal test results: CMS, Medipix, FE-I3

Overall CMS yield (11x4=44 sensors): 98%!

Overall Medipix yield (11x4=44 sensors): 77%!

Overall FE-I3 yield (11x4=44 sensors): 98%!
Temporary metal test results: RD53, FE-65

- Test pads constrained by closely fitting active edge trench
- Considerable risk of surface damage
- IV scans omitted RD53 on production wafers
- Temporary metal test on four FE65 sensors

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## Run-4 Hybridization and testing, University of Oslo

### UBM at IZM
- eight wafers shipped beginning of January
- expect 12 weeks processing time

### Flip-chip assemblies
- contract on flip-chip 40 assemblies
- considering diverting some die to AdvaCam
- flip-chip with LETI Cu-pillars

### RD53 die
- 8 x 2 die available
- good yield expectations
- also a number of FE65-sized die

## Lab characterization
- IV/CV on test structures after UBM
- Pulsed laser/TCT scanning
- Acquiring source test capabilities

## Test beam
- ISC cards in-hand
- wirebonding in Oslo
- still to figure out irradiation access (Karlsruhe, Ljubljana, CERN PS, OCL)

## Irradiation
- Aim to irradiate, rerun test beam during 2018 season
- Karlsruhe protons might be the most convenient
- IRRAD1 and/or Ljubljana
- Local OCL option, similar to Karlsruhe

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Run-5 Project plans

### Funding and timeline
- Funding from Norwegian ATLAS R&D
- Launching now, CERN Case-B rules
- SiSi wafers on order from IceMOS (UK)
- Fabrication 48 weeks, starting 2018Q2

### Foundry qualification goals
- Focus on 150 μm active thickness
- Layout 26 identical FEI4 die
- Apply Specification and Acceptance Criteria for 3D Sensors

### RD53 layouts
- Might dedicate a sub-lot (12 wafers) to R&D
- Consider dual or quad designs
- Or full reticle geometry (if available)
Conclusions and outlook

- Run-4 fabrication successfully completed
- Yield at +75 %
- Expect 40 SC assemblies for test beam and irradiation
- 16 RD53-die for early testing
- Run-5 launching now
- Focus on qualification
- Expect new parts 2019Q1