

13th "Trento" Workshop on Advanced Silicon Radiation Detectors



Hon-HEP Applications II

EDET 80k – A DEPFET based Ultra High Speed Camera System for TEM Direct Electron Imaging

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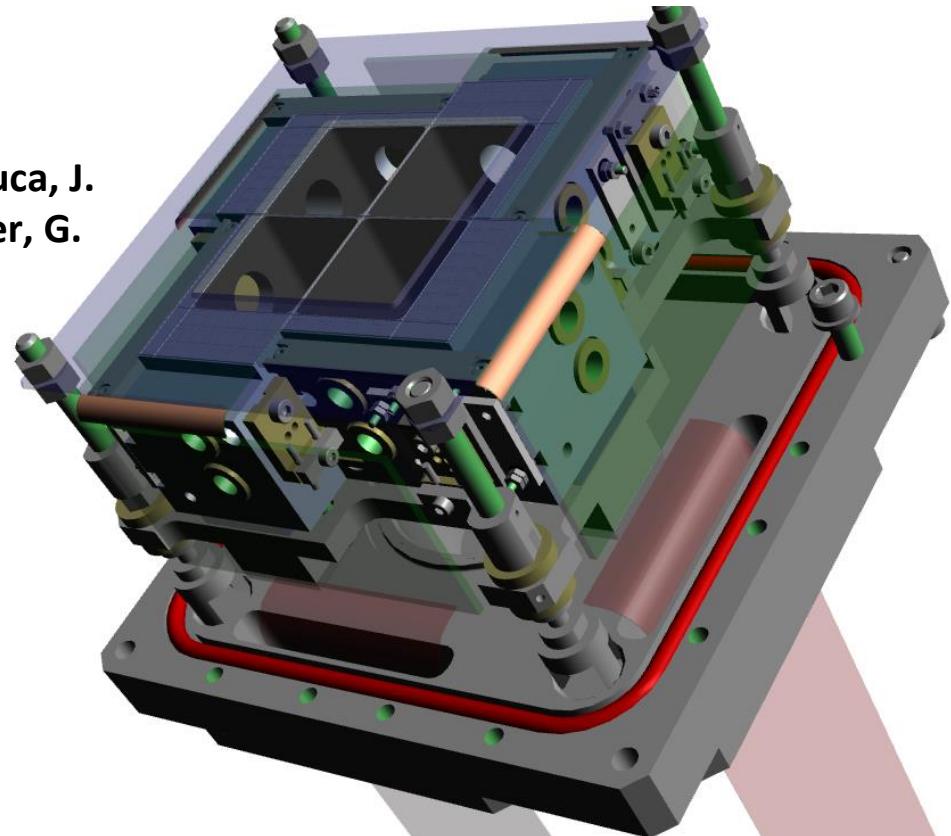
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KIT Karlsruhe



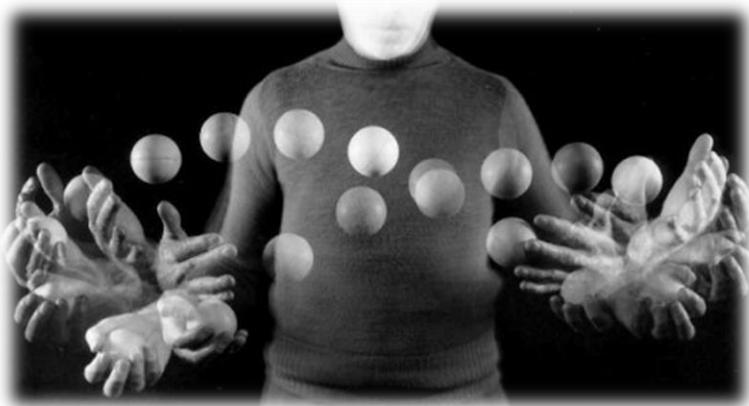
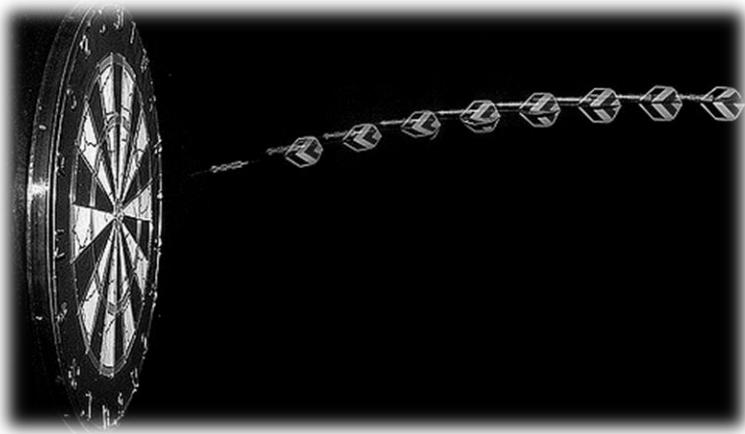
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Contents

- Introduction to the instrument
- DEPFET pixels
- ASM
- Module structure
- System structure
- CAD impressions
- Summary & Outlook



Introduction



Stroboscopic imaging provides insight to the dynamics of processes

Introduction

"Normal" imaging:

- Continuous illumination w/ fixed intensity
- Exposure period "gated" by shutter
- Exposure time defines image contrast
- Tradeoff between image contrast and impact of motion blur
- Defined by the dynamics of process



"Stroboscopic" imaging:

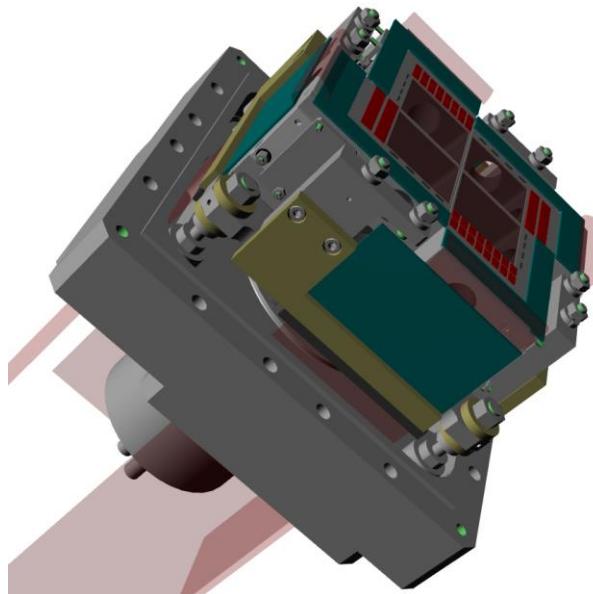
- Short, discrete illumination periods with high intensity (flashbulb)
- Pulse intensity defines image contrast
- Decouples exposure time, image contrast and motion blur
- Frequency of illumination defines time resolution
- Pulse duration defines impact of motion blur



Introduction

Stroboscopic imaging in TEM world is challenging:

- Stroboscopic illumination → Pulsed electron source
- Real space imaging → Large sensitive area
- High intensity → High dynamic range
- Direct electron detection → Thin substrate
- High pulse frequency → High framerate
- "Grey scale" image → No data reduction possible



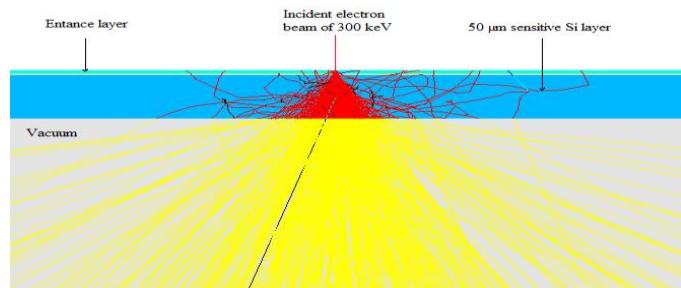
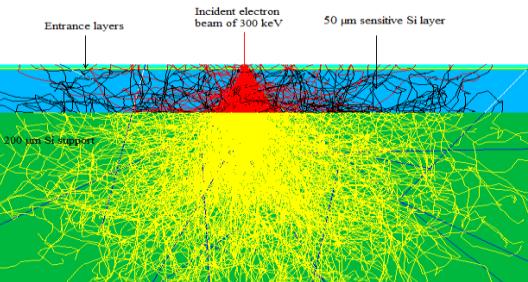
The instrument:

- Detector FPA consisting of 4 individual, independent modules ("tiles") capable of stand-alone operation.
- Mounted in TEM focal plane (narrow environment)
- Small sensitivity gap between tiles (1.2 mm)
- DEPFET arrays with $60 \times 60 \mu\text{m}^2$ pixel size
- Tile ray size 512×512 pixels
- 1 MPixel for complete FPA
- Thinned substrate with $50 \mu\text{m}$ and $30 \mu\text{m}$ thickness
- ASM complete with passives and FEE (DCD / DMC)
- Readout in rolling shutter mode
- Readout time 100 ns / row, 4 rows in parallel
→ $12.8 \mu\text{s}$ / frame
- Framerate max. 80 kHz
- FEE allows buffering of bursts (movies) with 100 frames
- Maximum burst rate 100 Hz

Introduction

Challenges:

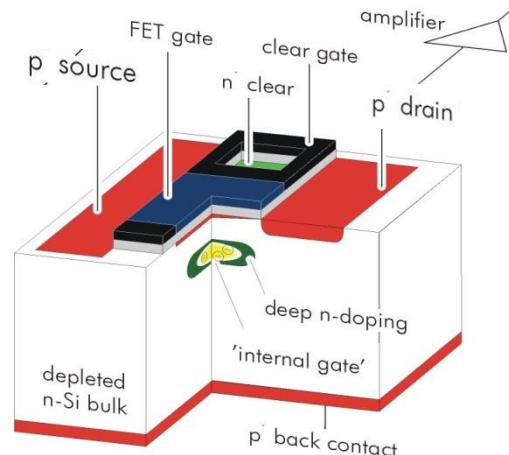
- Data rate
 - Max. burst frequency 100 Hz (100 frames each)
 - Digitization with 8 bit resolution
 - Tile module data rate 2.9 GByte / s gross
 - Total data rate ~ 11.6 GByte /s gross
 - Data reduction / zero suppression difficult
- Dynamic range
- Single primary electron sensitivity
 - Primary electron @ 300 keV on 50 μm Si
 - Distinguish 8k e- from noise
 - 50 (better 100) primaries per pixel to provide enough contrast
 - 800k signal electrons to be stored in pixel
- Operation in vacuum:
- Small volume / extremely compact setup
 - Cooling / thermal stabilization
- Multiple scattering:
- Thin sensitive detector substrate
 - No support layer
 - Highly efficient beam dump for traversing electrons
 - Advanced thermal support



DEPFET Pixel

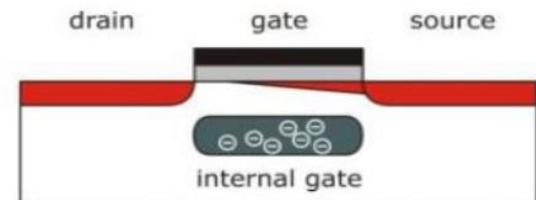
DEPFET integrated amplifier

- p-channel FET on depleted n-bulk
- Signal charge collected in potential minimum below FET channel
- "Internal gate"
- FET current modulation ≥ 300 pA/el.
- Reset via clearFET
- Low capacitance & noise
- Charge storage, readout on demand
- Rolling shutter mode



EDET pixels:

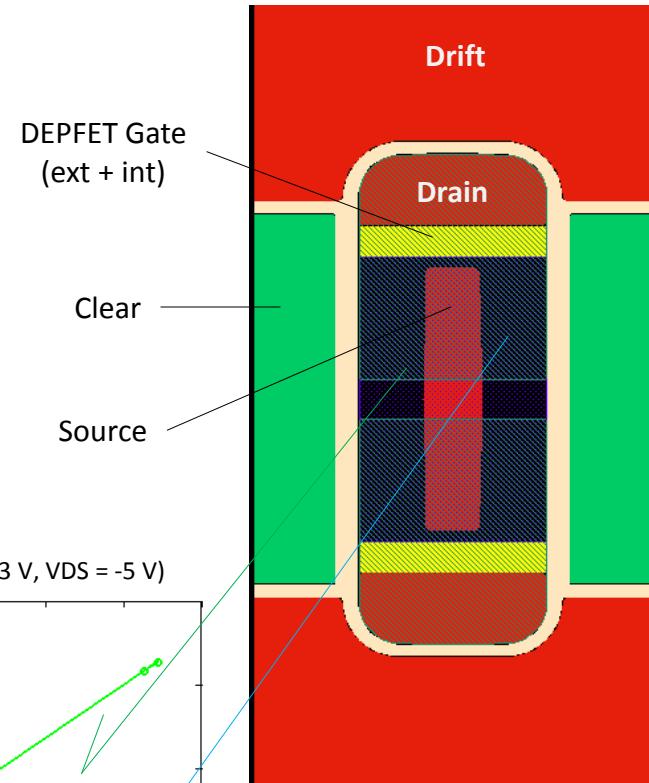
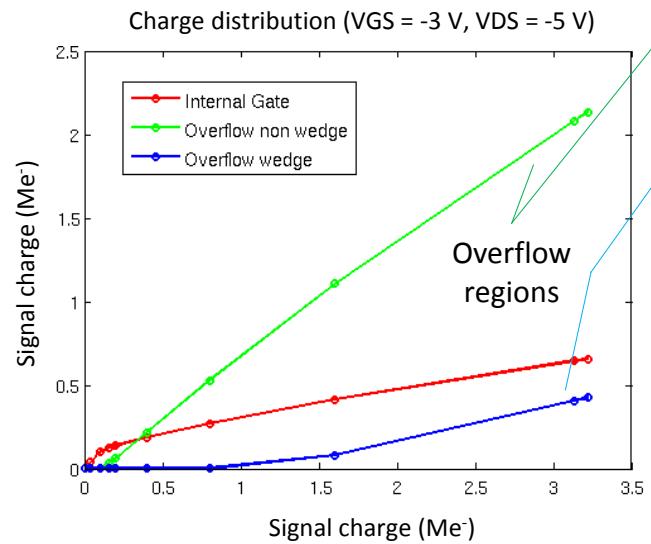
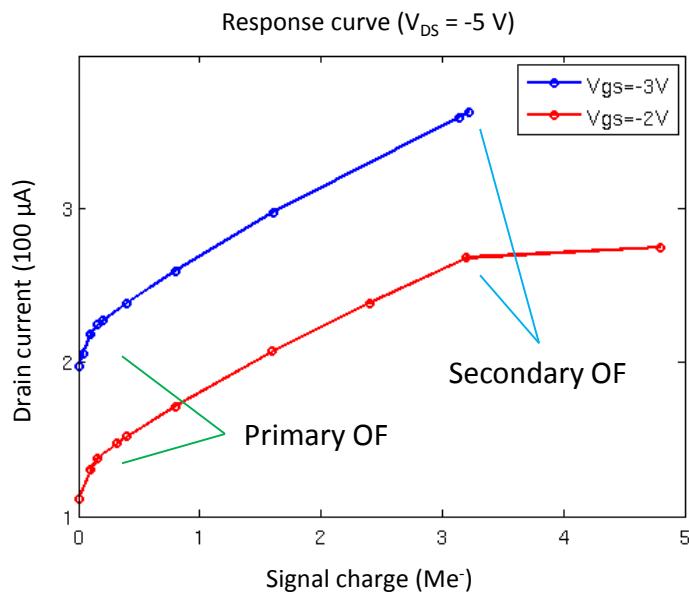
- Dynamic range problem
- Implement signal compression in pixel
- Overflow to source to tailor dynamic range



DEPFET Pixel

EDET pixels:

- Shape of source implant creates 2 overflow regions
- Different onset points of overflow
- Large dynamic range
- Sensor w/ integrated signal compression



Detector ASM

ASM:

- High integration density requires integration of Detector matrix, front-end ASICs and supporting passives on common substrate
- "PCB on silicon" → All-Silicon module (ASM)
- Substrate thinned down to 50 -30 µm thickness in sensor region
- Supporting window bars

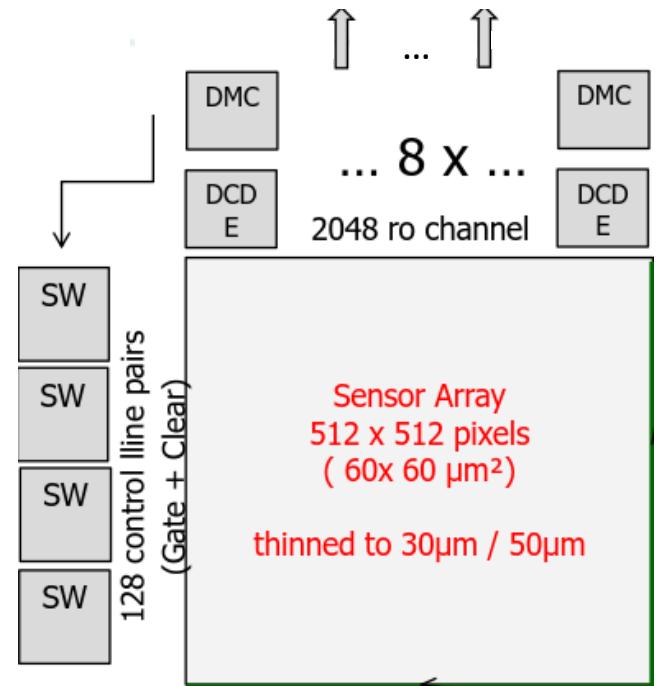
Direct Current Digitizer for EDET (DCD-E)

- UMC 130 nm technology
- 256 channels read in parallel
- 8 bit digitization, 100 ns conversion
- 64 parallel data output links @ 320 MBit/s

DEPFET Movie Chip (DMC)

- TSMC 40 nm technology
- Data buffer, serializer & sequencer for all DCDs and Switchers
- Fast data transfer to periphery using 8 parallel 320 Mbit /s LVDS outputs

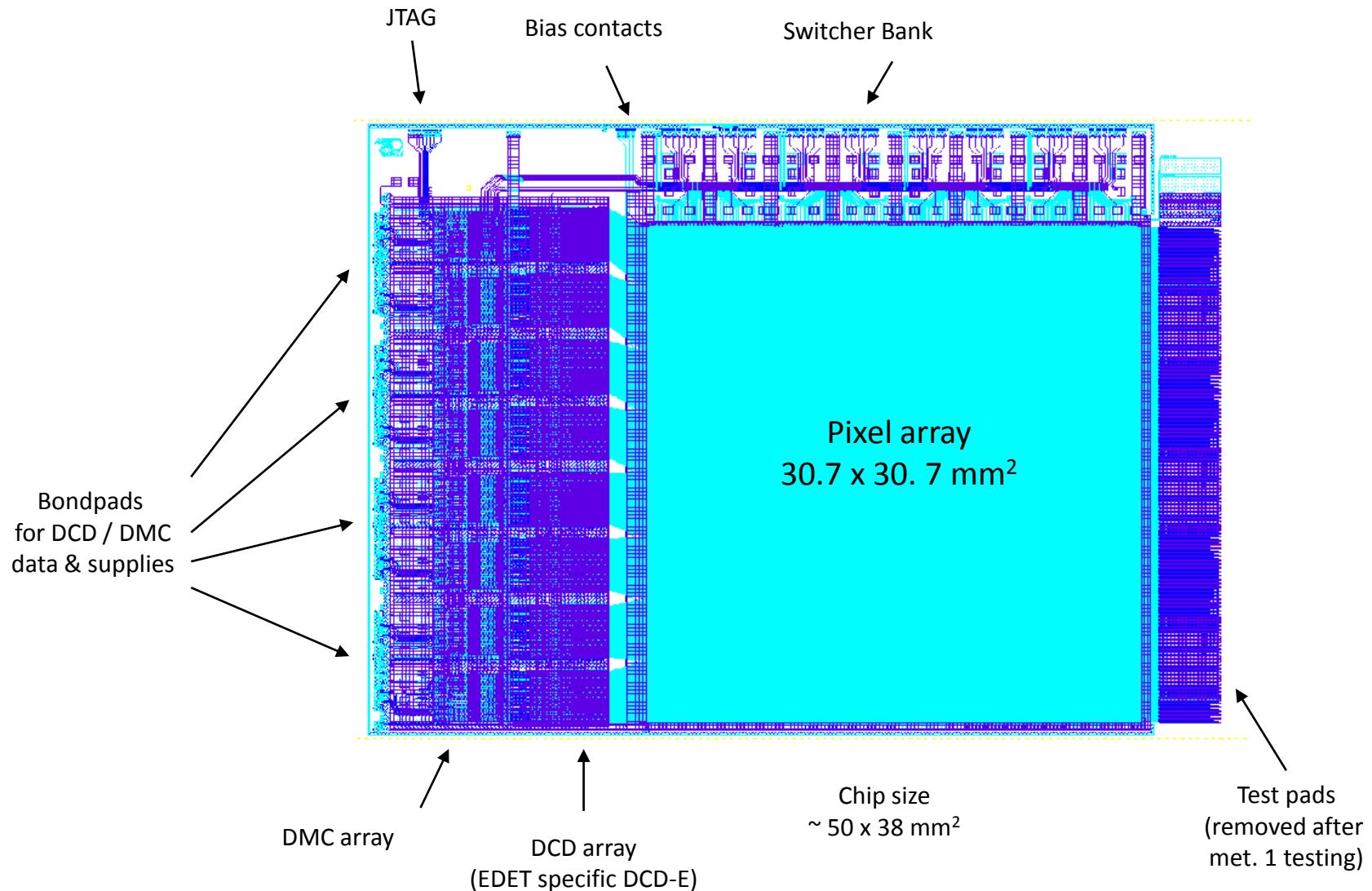
up to 8 serial links (@320 Mbit /s)



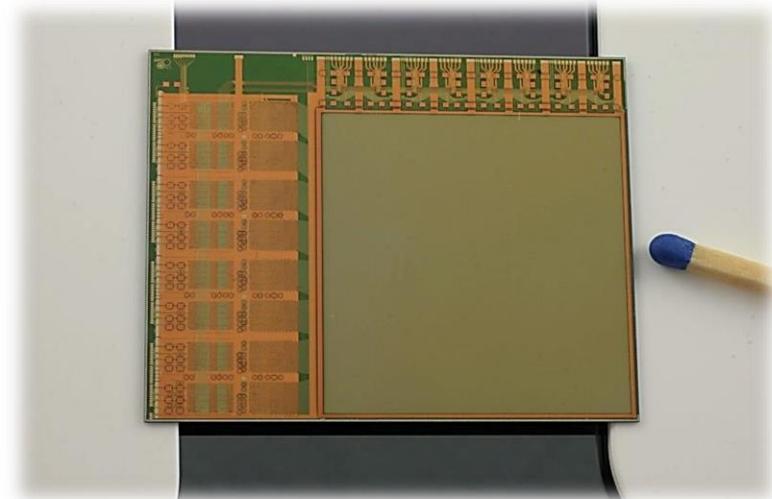
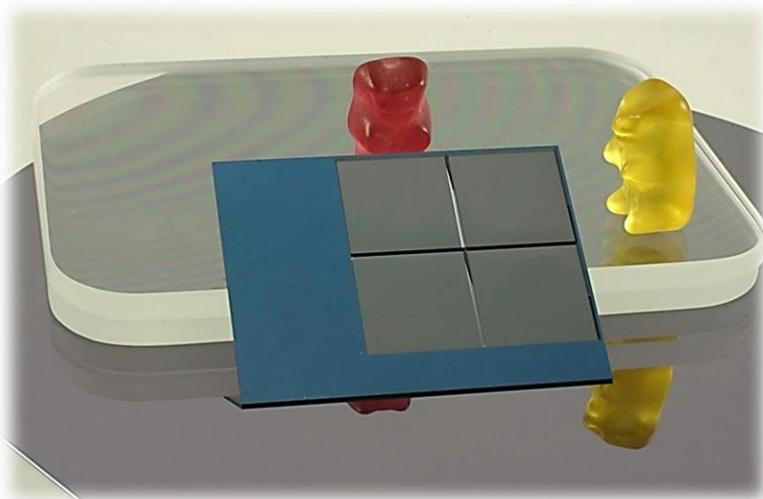
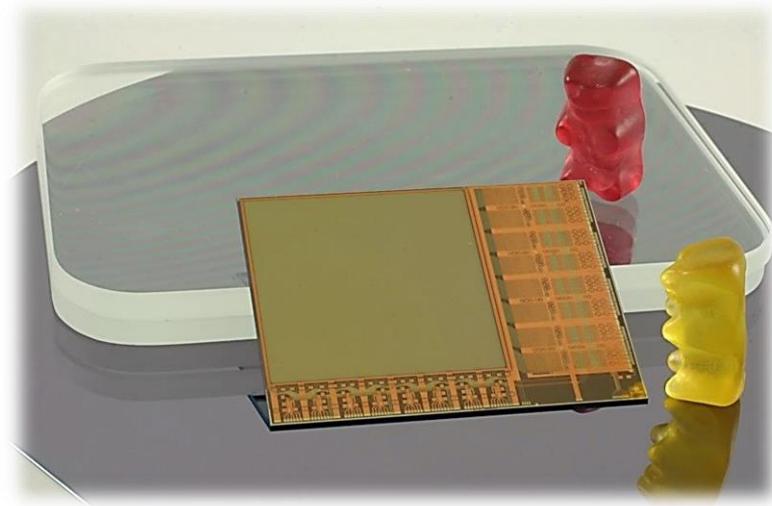
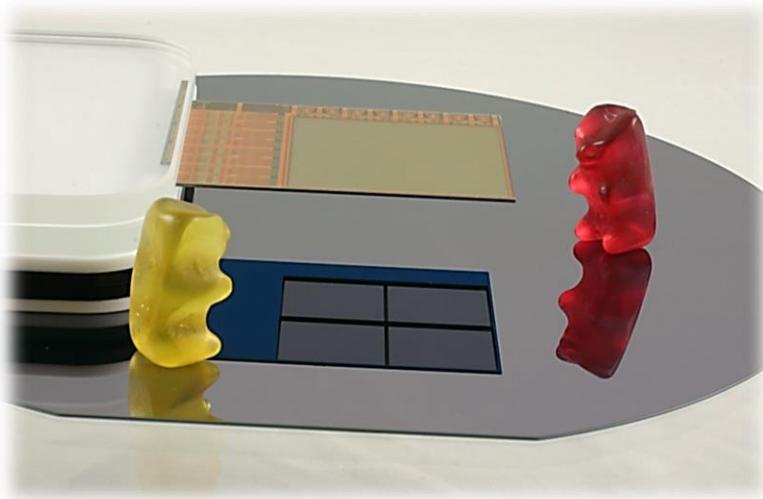
Switcher-B:

- AMS H18 HV technology
- Controller IC, 32 channels
- Each channel driving gate and clear lines of 4 ASM pixel matrix rows in parallel

Detector ASM



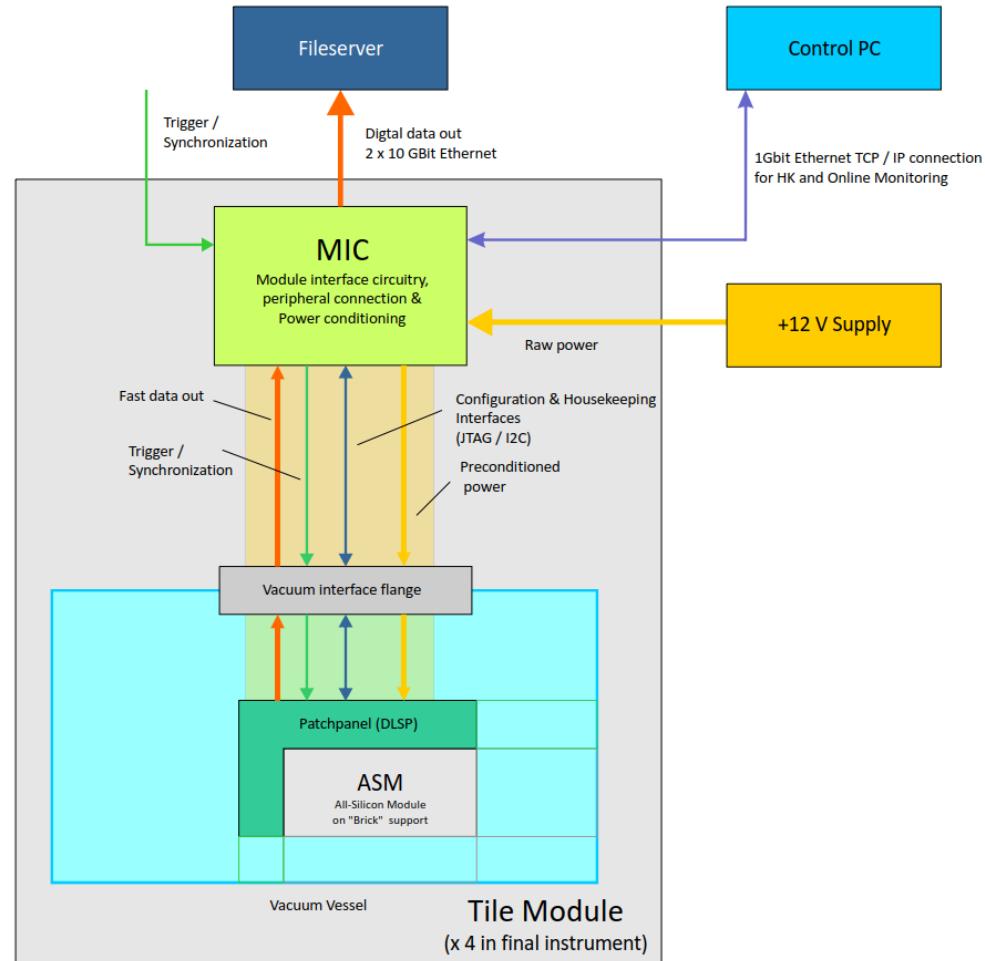
ASM – bare die



Module structure

Module components:

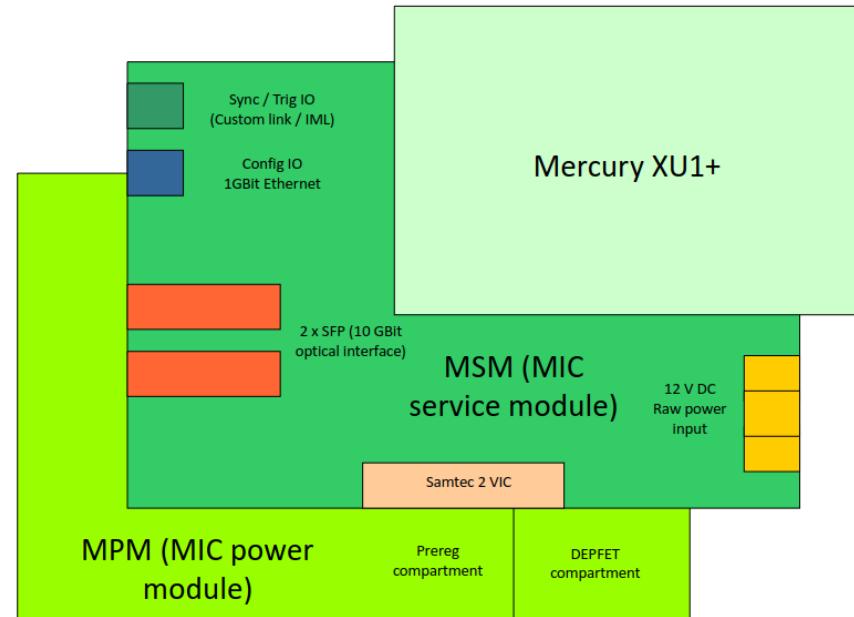
- ASM: All-Silicon module
- Brick support: Mechanical and thermal support for ASM and interface to main heatsink
- Patch panel: Wire bond adapter, local power conditioning and housekeeping circuitry
- Integrated with 3 other tile modules on main heatsink in vacuum vessel
- Vacuum interface flange with flexlead for electrical connection
- Connected to Module Interface circuitry for peripheral connection
- All hardware components of tile module
- Communication w/ control PC for housekeeping and online monitoring using 1 GBit Ethernet interface
- Trigger input from TEM and synchronization clock
- Fileserver system for fast data storage, data transfer using 2 x 10 GBit optical interface (UDP stream)
- Supplied with a single 12 V raw power supply



Module structure

Module Interface circuitry (MIC) :

- Peripheral interconnect based on modular stack of 3 modules
- MSM: Service module hosting physical interfaces & interconnects
 - Housekeeping & configuration
 - Fast data transfer
 - Trigger inputs
 - Connectors for Mezzanine cards
- MPM: Power module hosting Preregulators and biasing circuits for ASM
- Provides for supply of entire module w/ a single 12 V DC power supply
- MBM: Brain module based on powerful Zynq UltraScale FPGA from Xilinx
- Service functions, fast data transfer using MGBTs and potential data compression and preprocessing

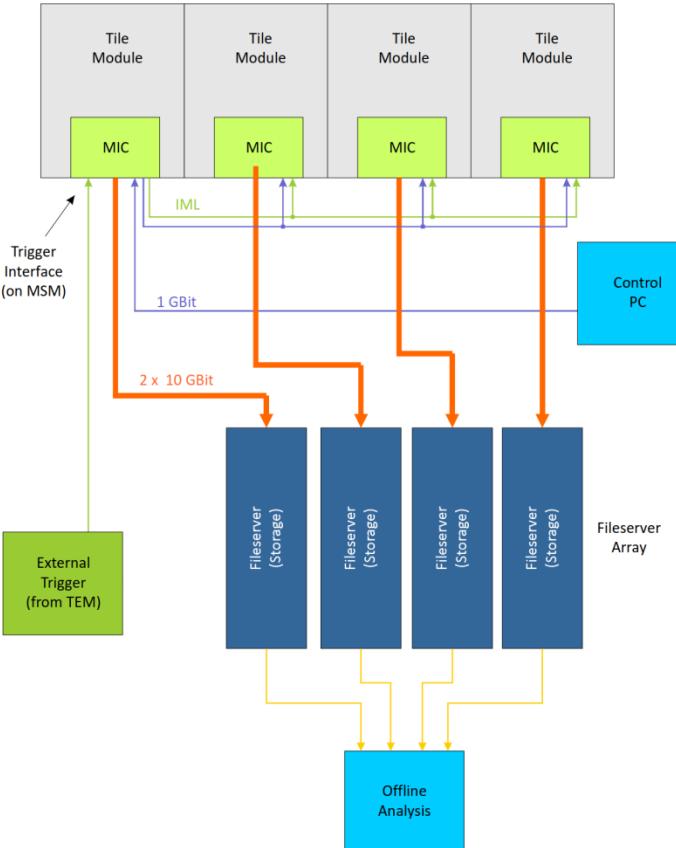


MBM module
(Enclustra Mercury + XU1)

System structure

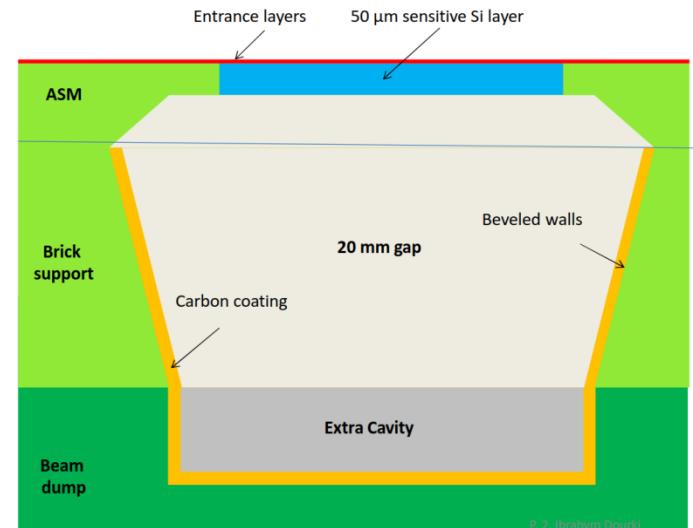
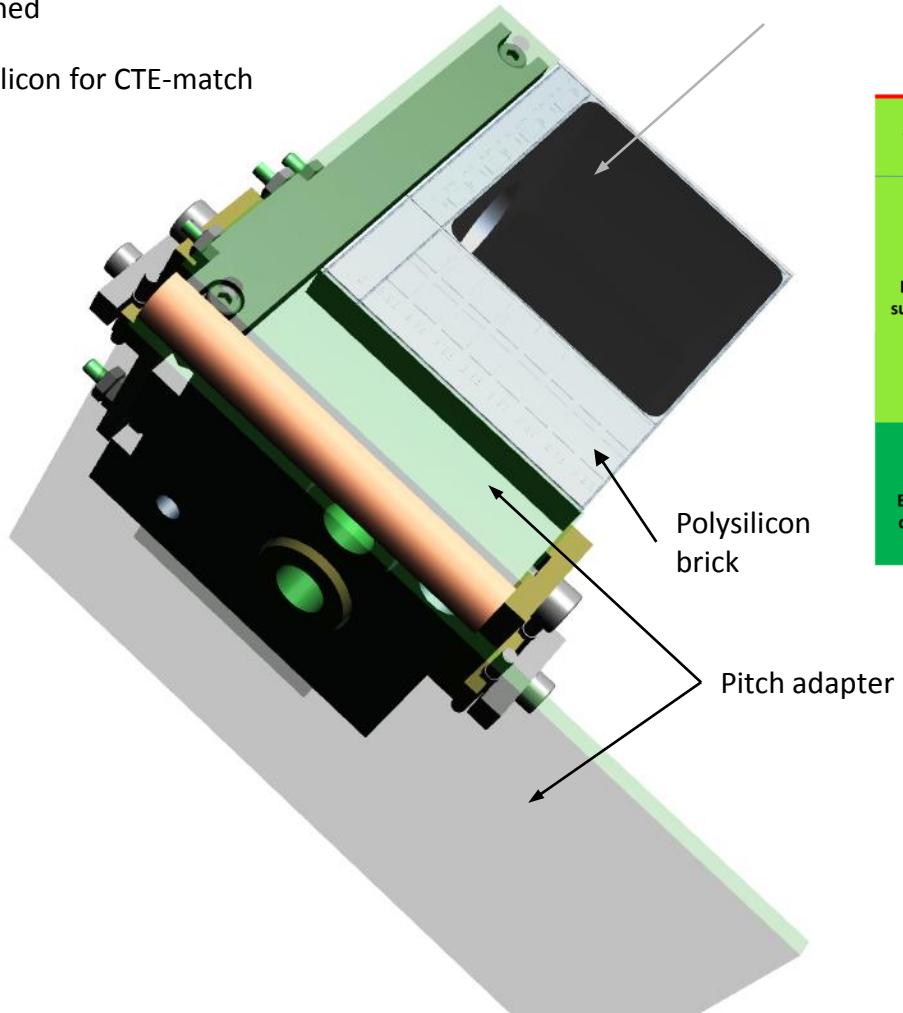
DAQ Concept:

- Complete system is formed by 4 identical, independent tile modules
- Configuration of modules via individual standard 1Gb Ethernet link
- Control PC does configuration, housekeeping and online Monitoring
- Trigger from TEM is applied to one ("master") module
- Master distributes the trigger to slave modules using proprietary Inter-Module link (IML)
- Fast data is transferred to module-individual Fileserver storage using 2 optical 10 Gbit Ethernet connections
- Fileserver array makes data available for offline analysis
- Possible replacement of module-individual configuration link by IML based master-slave architecture in a later stage



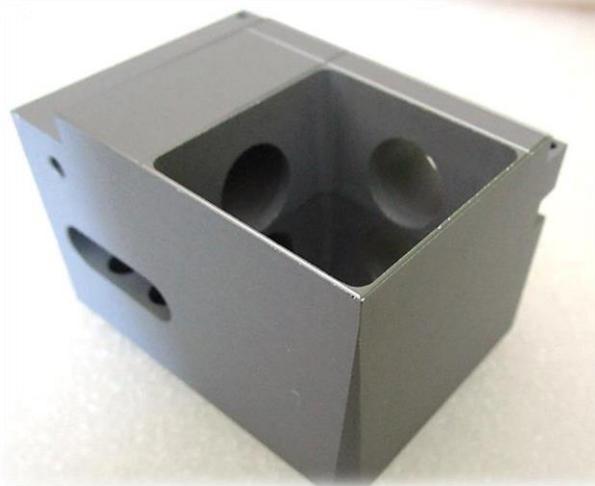
CAD impressions

- Brick support w/ patch panel attached
- Polysilicon for CTE-match

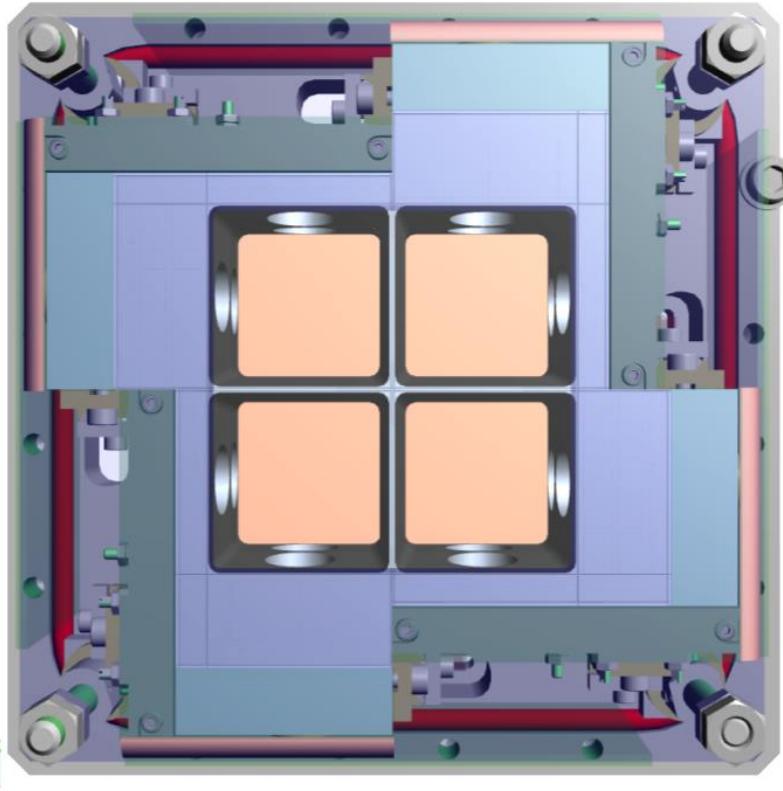


- Beam dump geometry for lowest backscattering

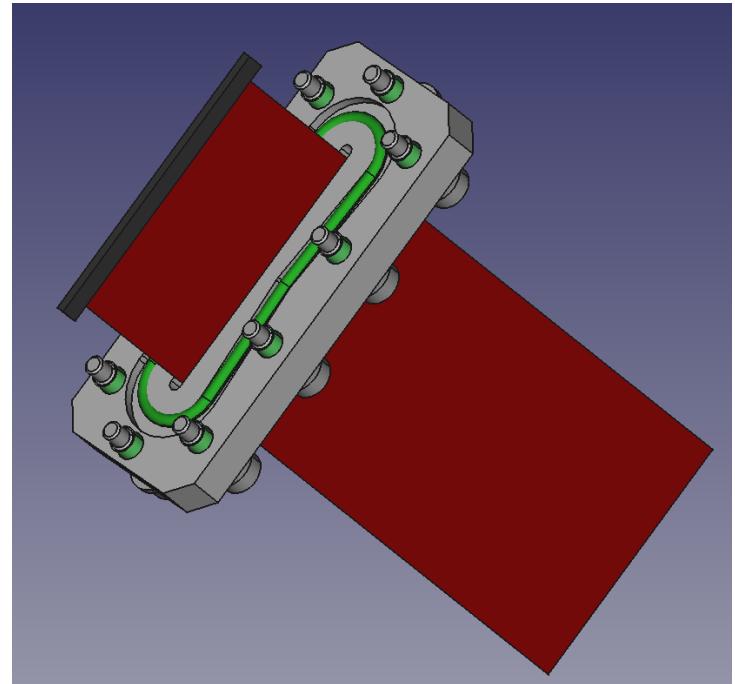
Hardware



CAD impressions



- Top view of FPA w/o ASMs attached

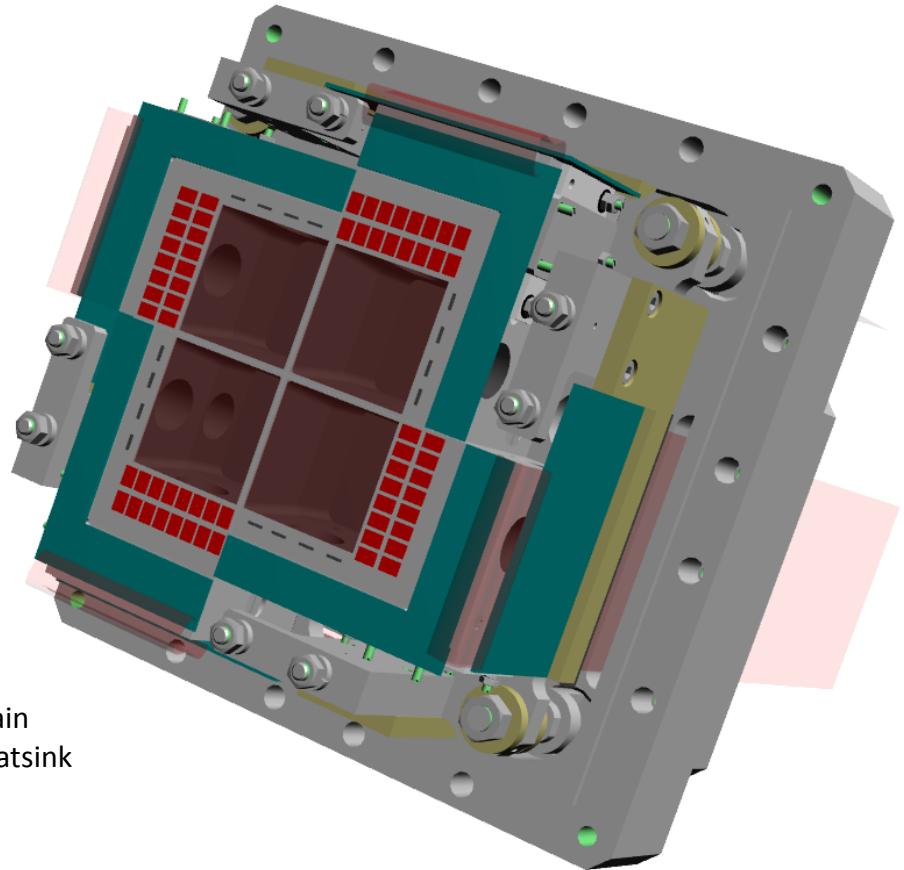
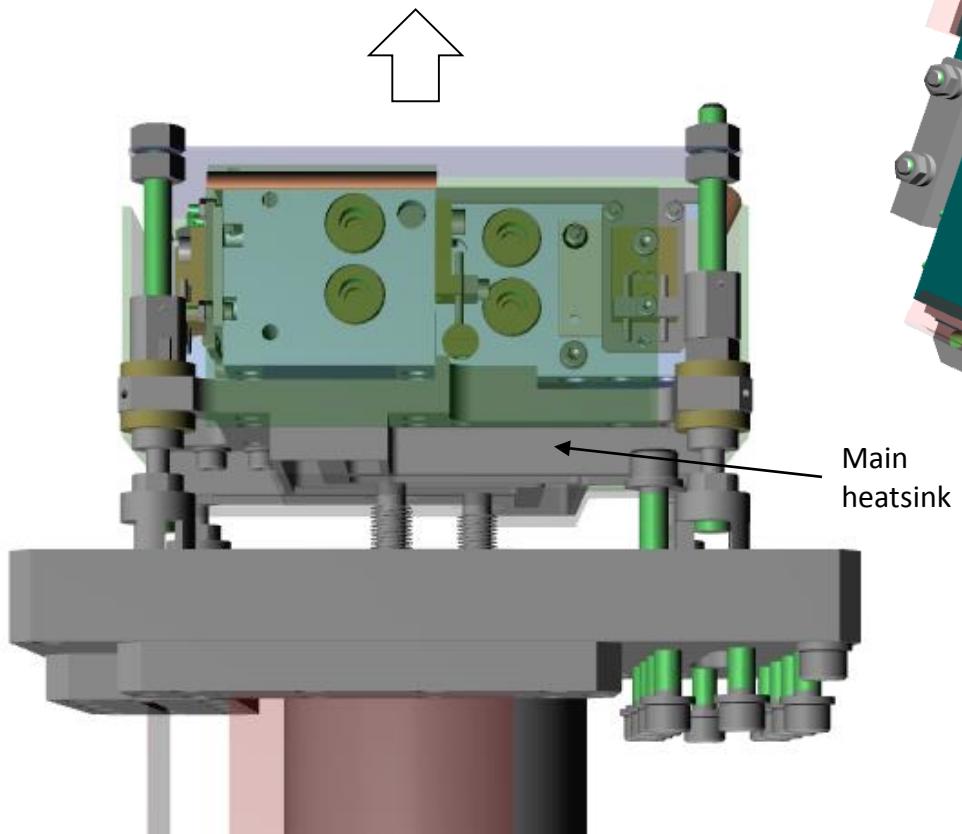


- Vacuum feedthrough flange

CAD impressions

Insertion:

- Insertion fo complete FPA stack from below
- No cable mounting from top required after insertion



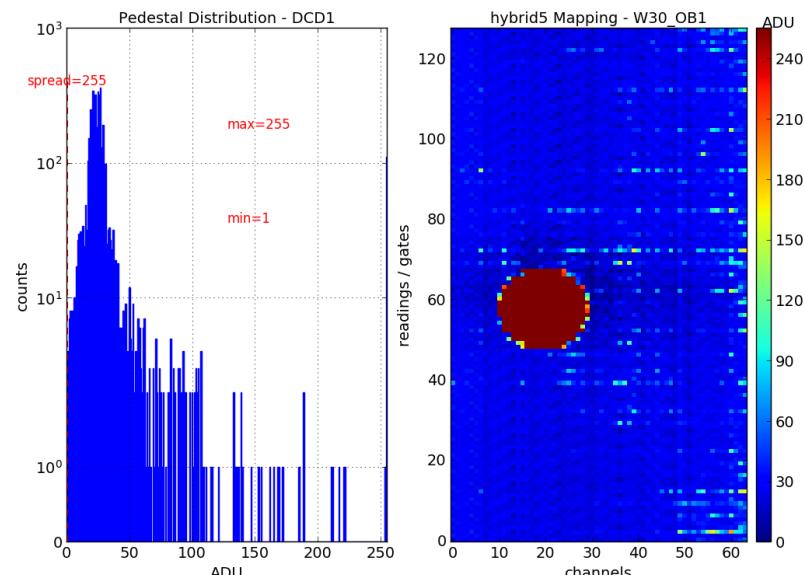
- Complete FPA (4 ASMs, FEE shield not shown)

Test program

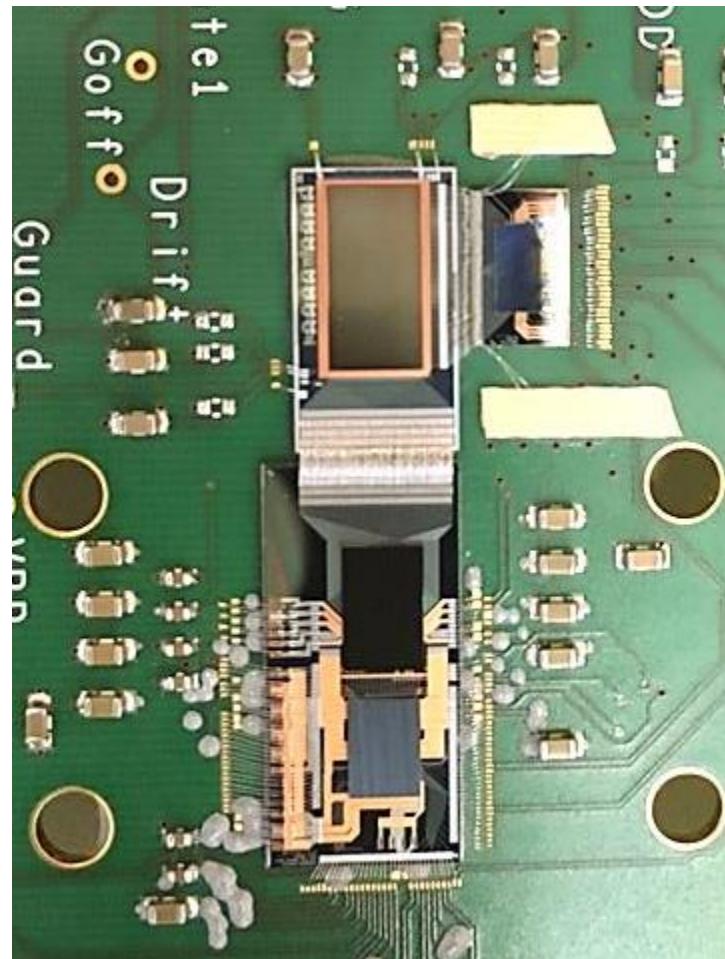
Prototypes:

- Matrix prototypes with 64×128 topological pixels used for detector and ASIC qualification, system development
- Current prototype assemblies use the BELLE DHPT IC
- Single pixel chips for detailed device response calibration and irradiation testing
- Tests in progress

- Test matrix assembly



- Laser beam spot

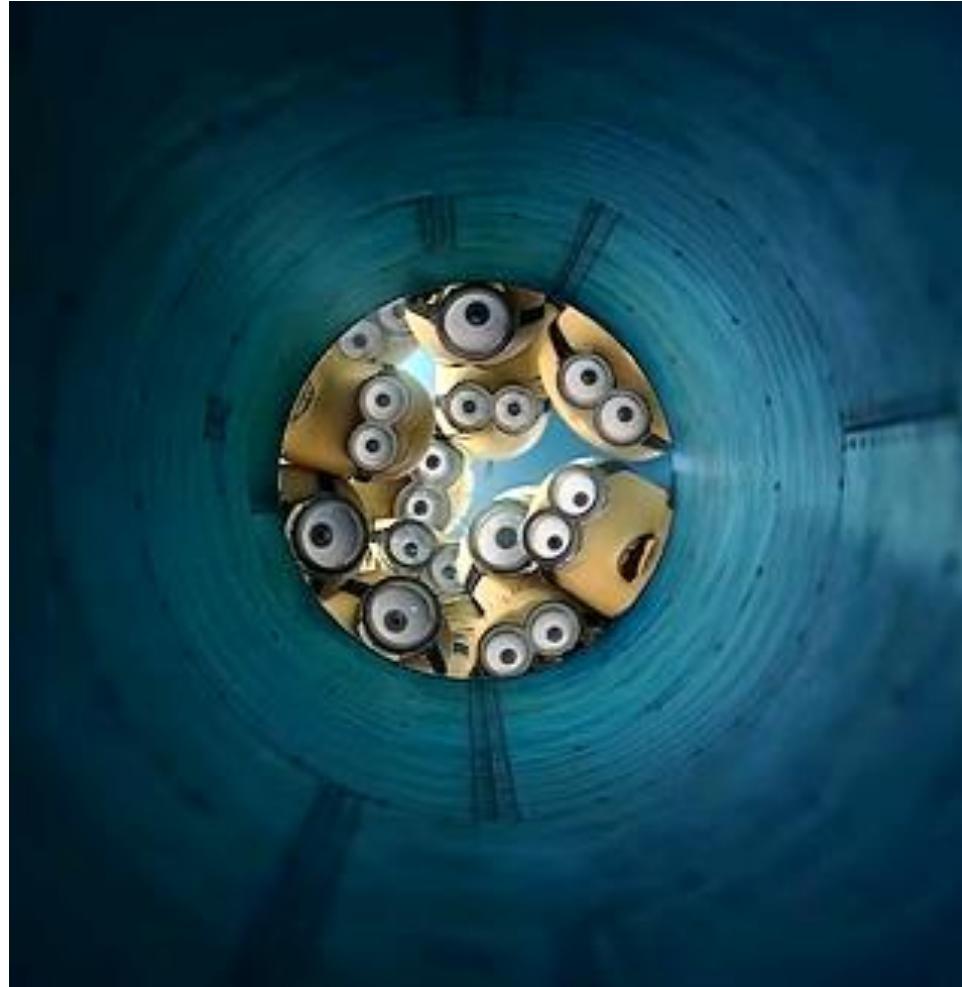


Summary & Outlook

Status:

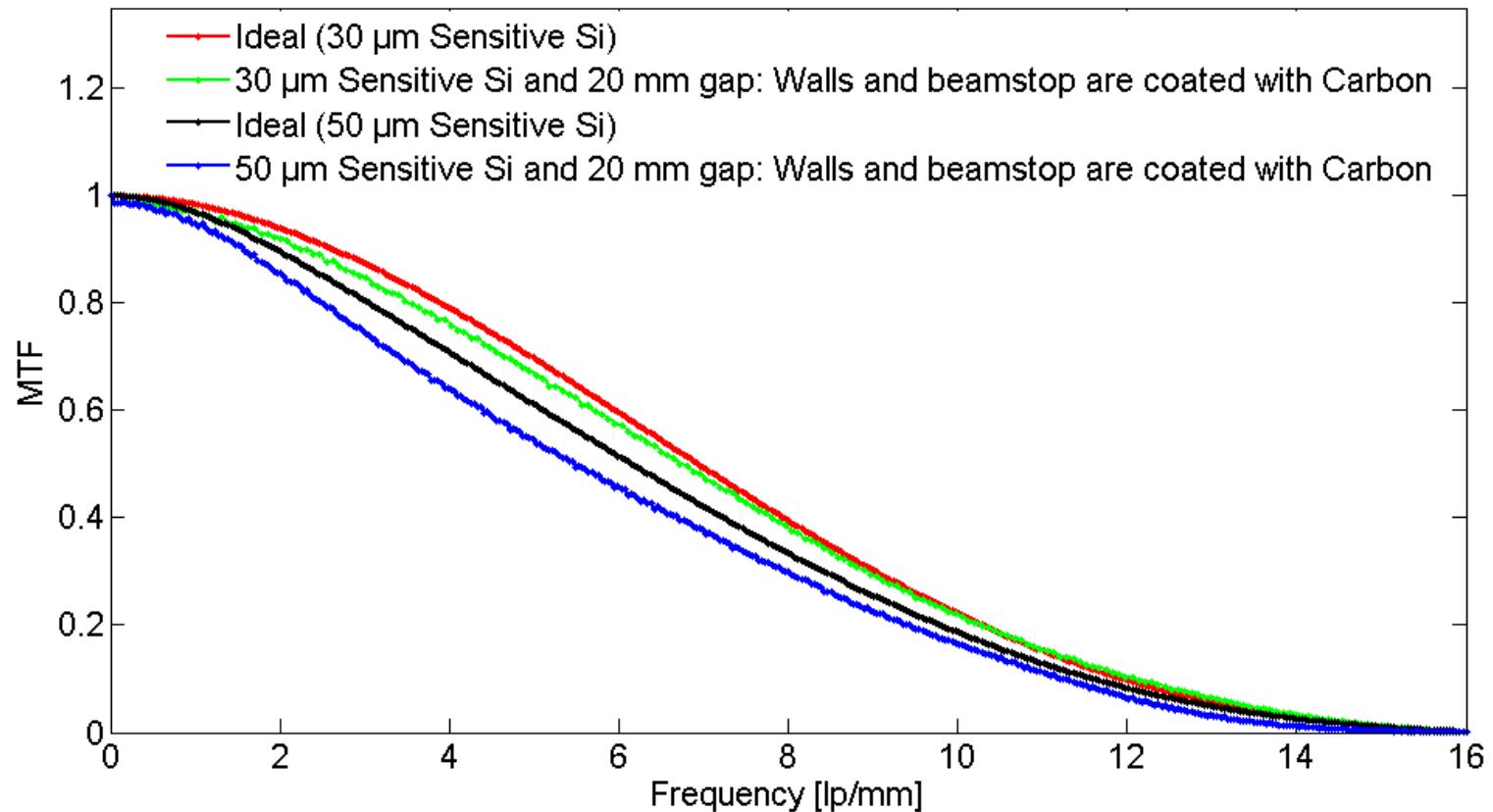
- ASM pilot production finished
- Detector measurements on small devices in progress / qualification of different designs
- DCD-E available and qualified
 - DMC submission 3/2018
 - DLSP prototyping successful
- Roadmap for DLSP / MIC development
- Full sized prototype module in Q3/2018
 - Using DHPT IC instead of DMC
 - Full-scale system ready Q1/2019

Backup slides

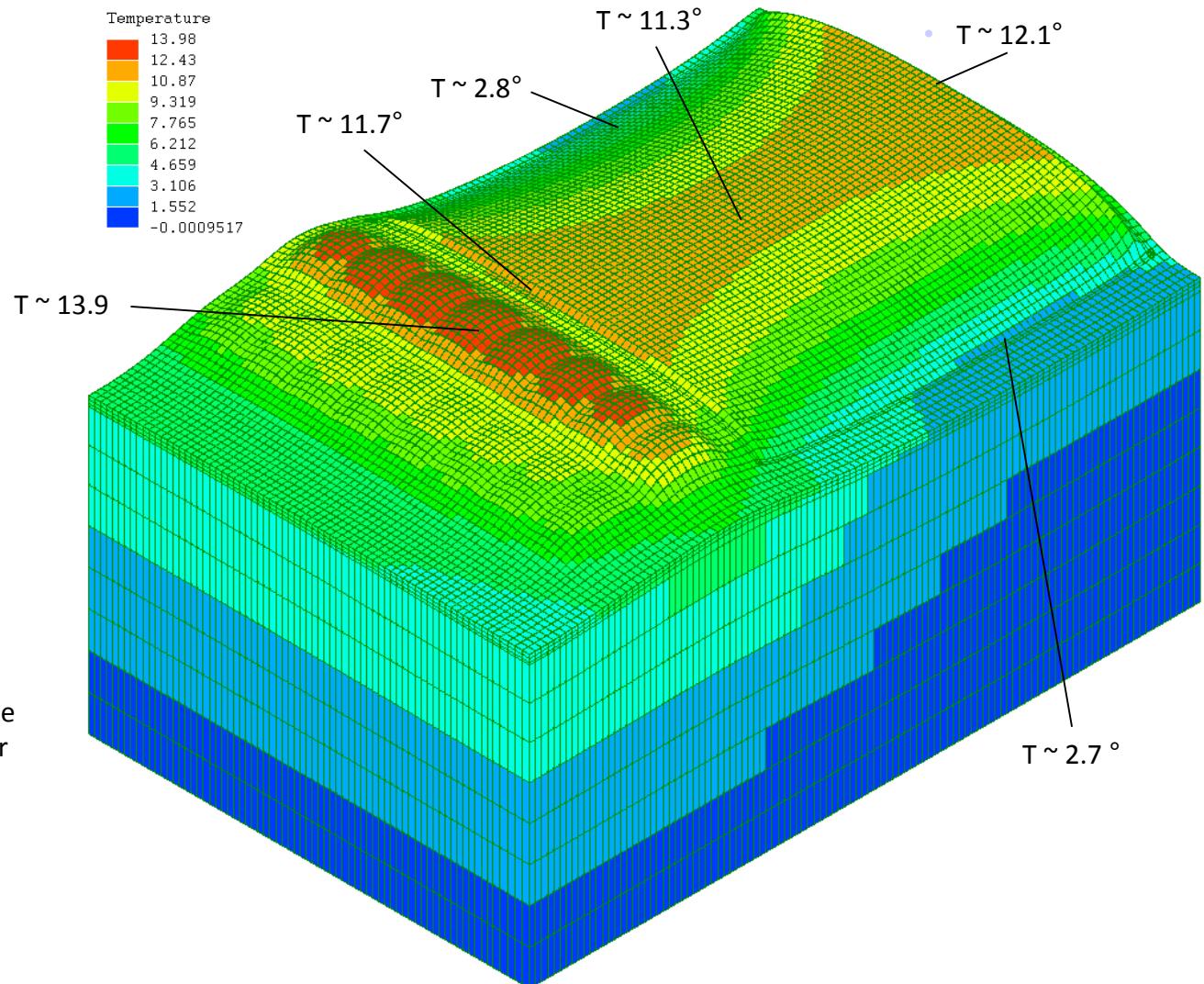


Modulation transfer function

Quantitative description for the contrast behavior



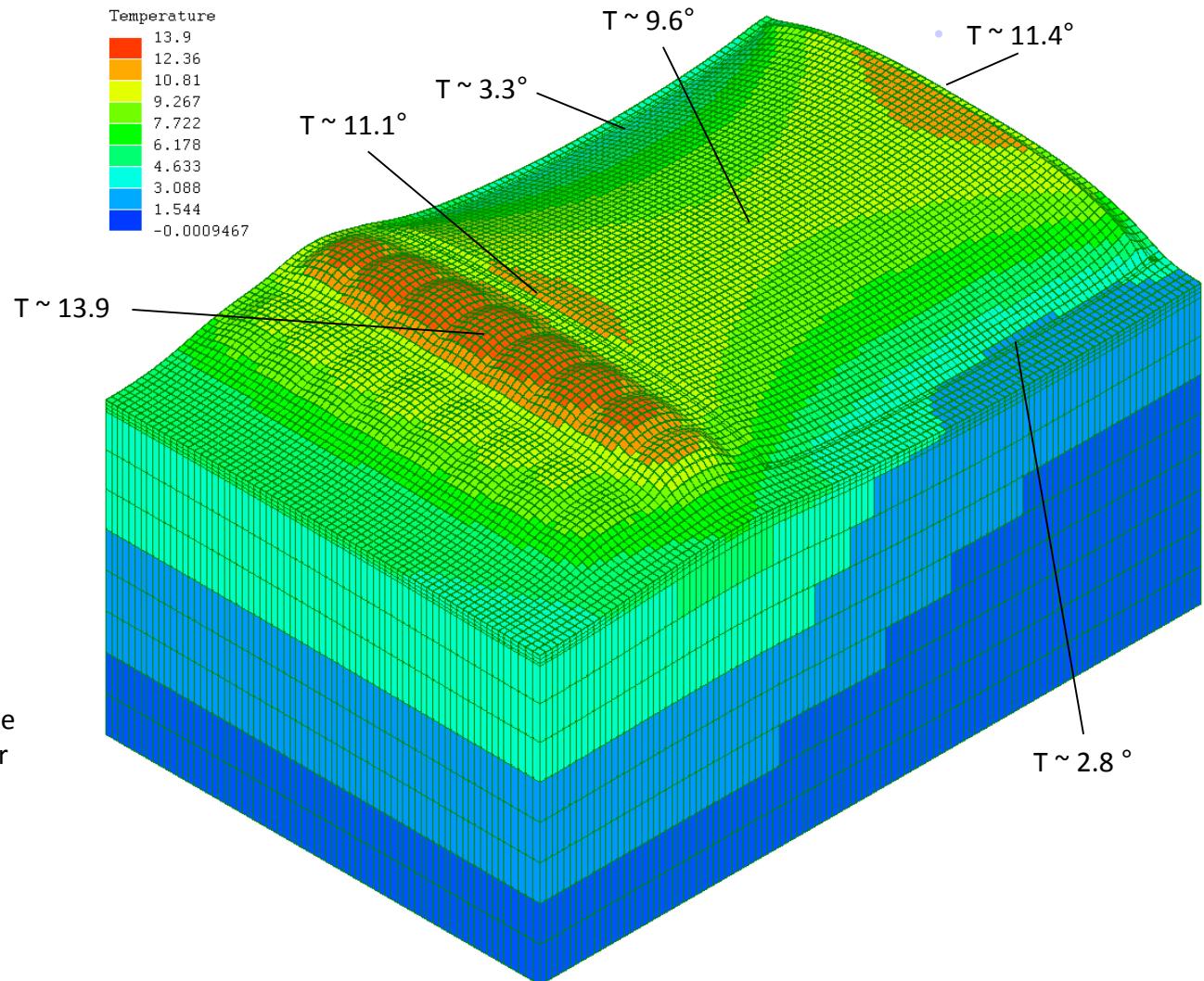
Thermal gradient 30 µm



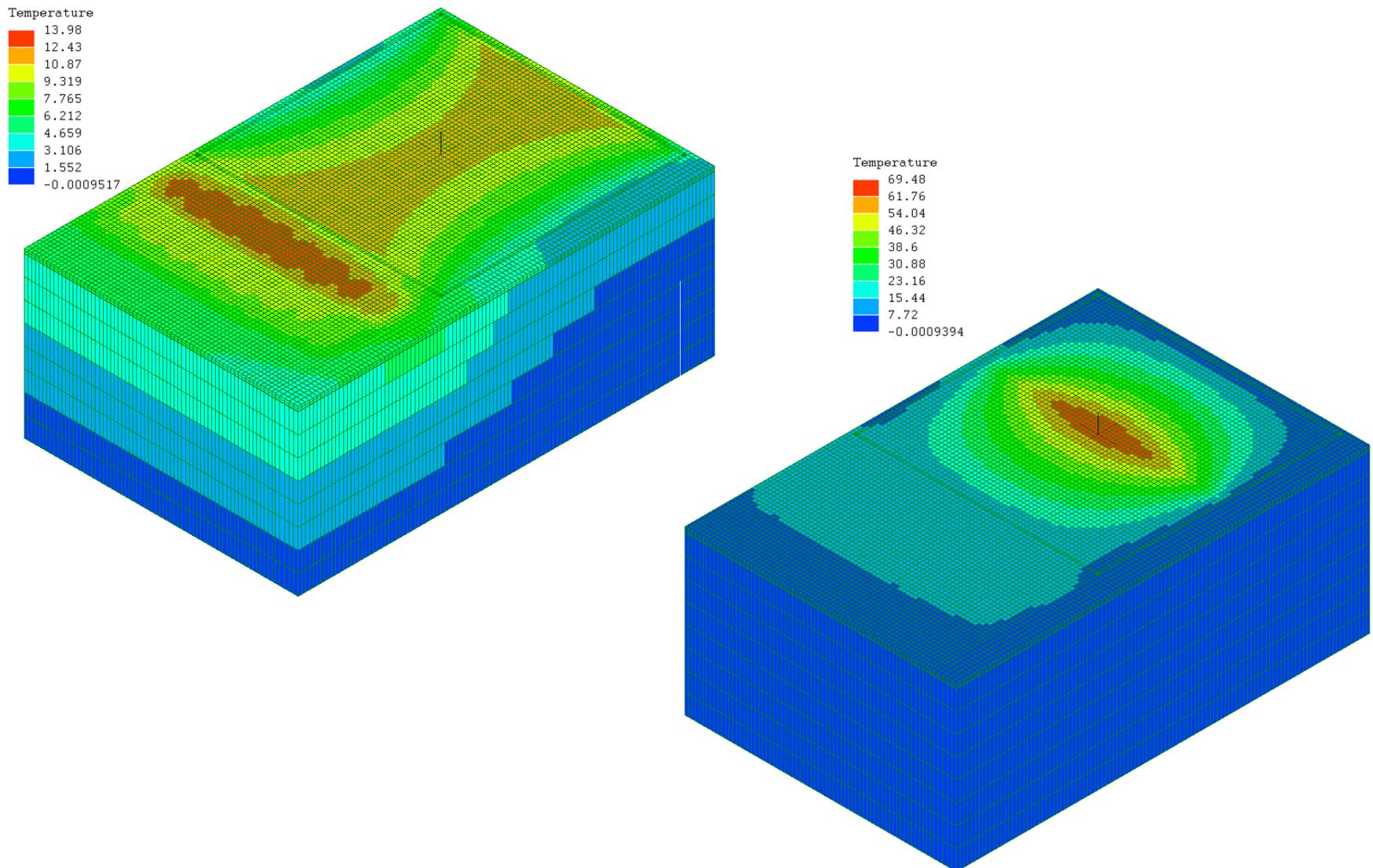
Detector temperature:

- Adaption of operation mode limits thermal gradient over matrix to 9°C (30 µm case)
- Duty cycle of ~ 10:1 mandatory to keep temperature gradient low

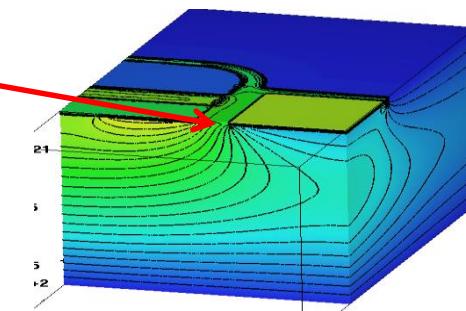
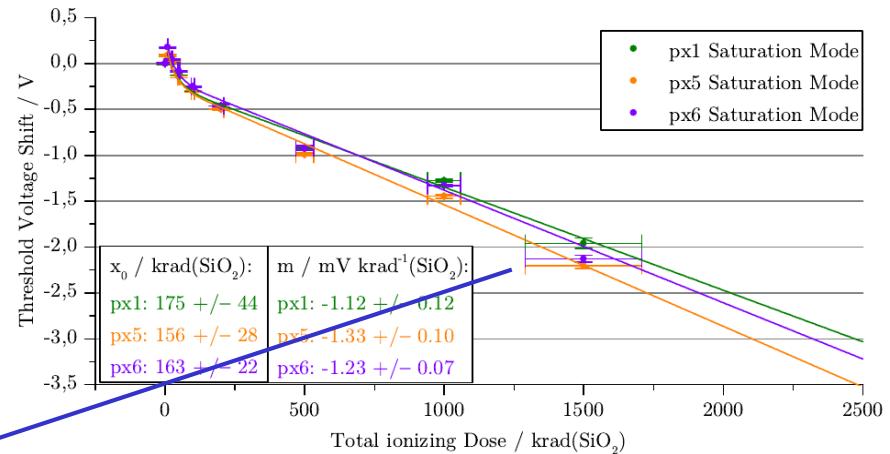
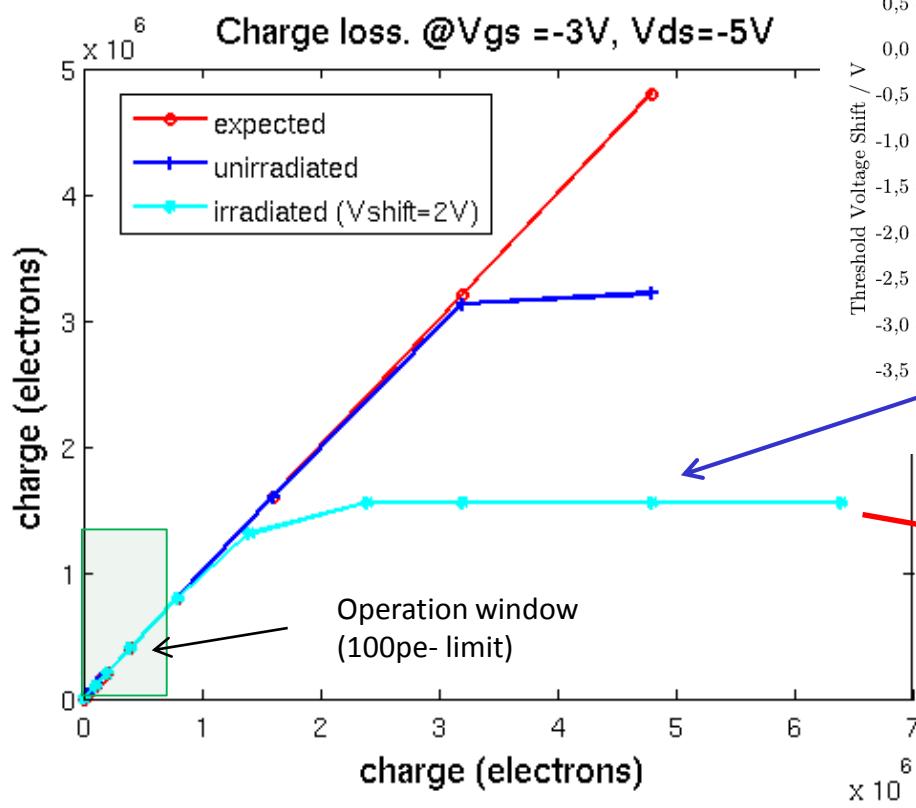
Thermal gradient 50 µm



Thermal budget



Radiation hardness



Real space detector sees a rather homogeneous radiation level

→ Oxide charge buildt up is homogeneous

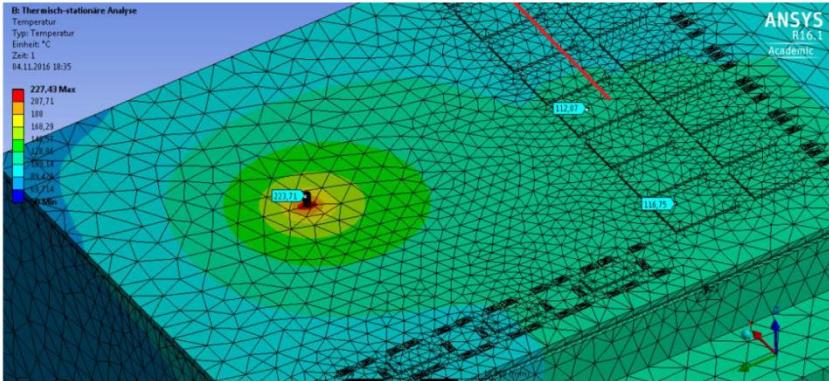
→ compensated by Gate voltages

Concern: inhomogeneous rad.

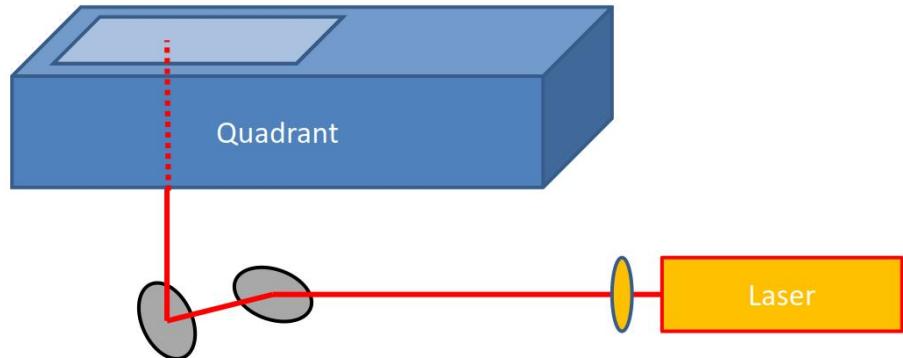
Scanning laser annealing

Laser: 500 µm, 5W

112°



- 5W: 225° around laser point



2 Mirror deflection unit:
To cover sensitive area
even with inclined walls

Laser: 810 nm
cw, 10-20 Watt

WHENEVER YOU
ASK THAT, MY
TAIL GETS ALL
BUSHY.
WHAT
COULD POSSIBLY
GO WRONG??

