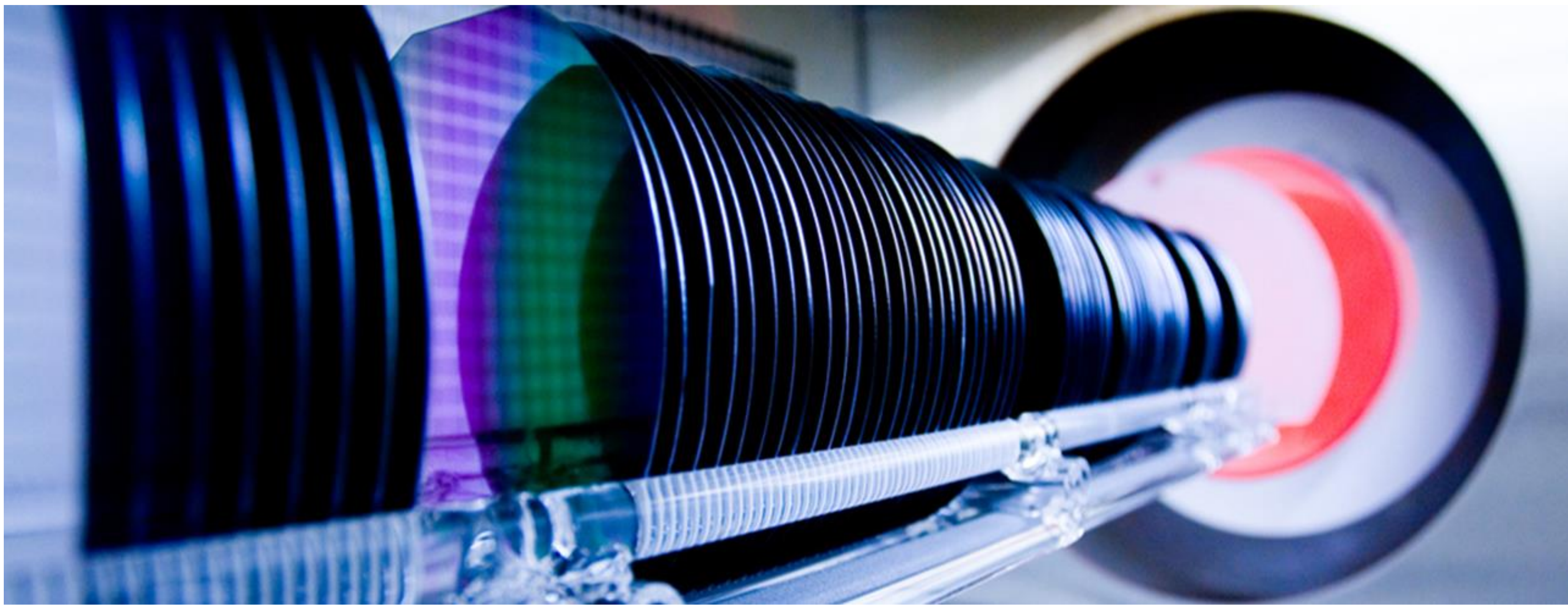


CiS Forschungsinstitut für Mikrosensorik GmbH

13th Trento Workshop on Advanced Silicon Radiation Detectors

New Approaches to HEP Sensors at CiS

Munich, 19.02. – 21.02.2018

Arno E. Kompatscher | Tobias Wittig | Alexander Lawerenz | Ralf Röder

February 20, 2018

Contents

1. Bias grid alternatives: fuses

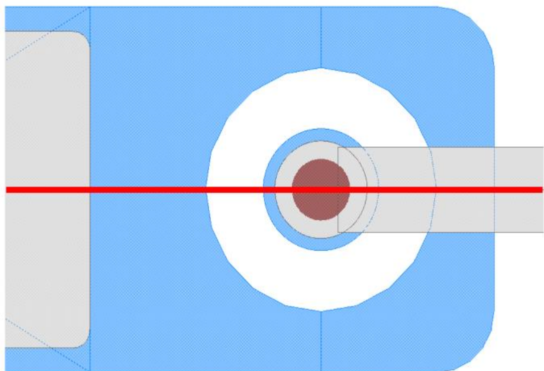
   first dummy wafer run, electrical fuse tests, etching tests, sensor waferrun completed this week, dummy flip chipping, testing with x-ray

2. Active edge sensors

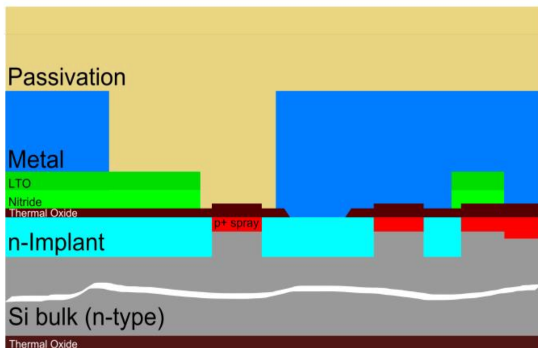
   Project completed, some results

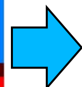
3. Trenches as pixel isolation, 3D-sensors

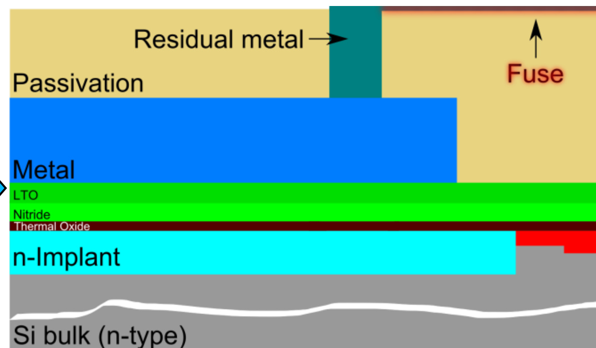
Bias rail alternatives
└ proposed solution



- idea: implementation of „fuses“
  - very thin metal traces on top of the final passivation
- sensor test with short-cutted pixel matrix





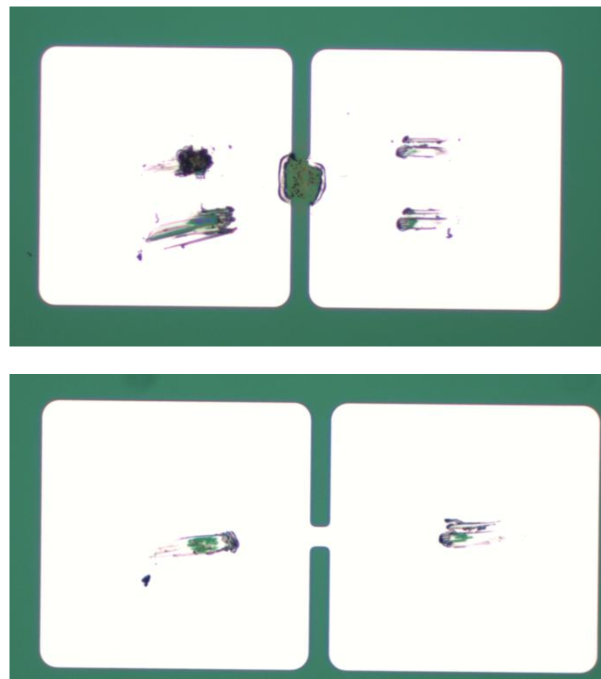


Removal of fuses afterwards:
- very short etching step
- laser
- melting by applying high currents

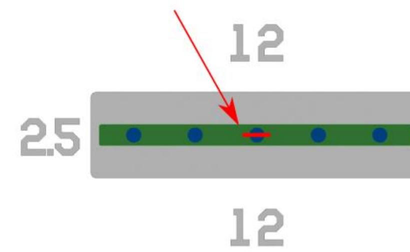
Bias rail alternatives
└ dummy fuse tests

- first tests of “burning” fuses successful
- but: problems with thickness of metal layer
  - 25, 50, 150, 300 nm thickness
  - too thin for needle: sometimes metal melted/scratched contact point
  - no issue though: pads were only for proof of principle

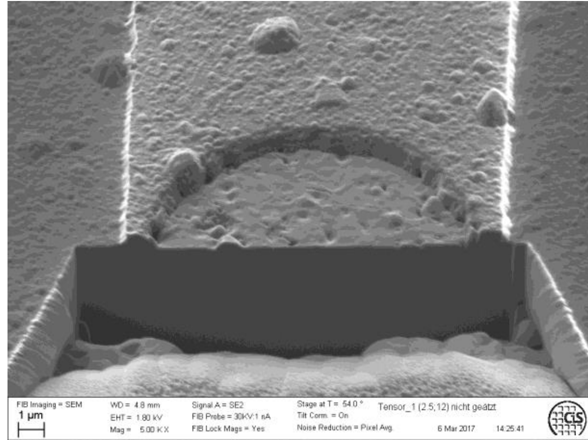
- additional test on prototype (2nd wafer run): wet etching!



Bias rail alternatives
└ etching tests: FIB analysis

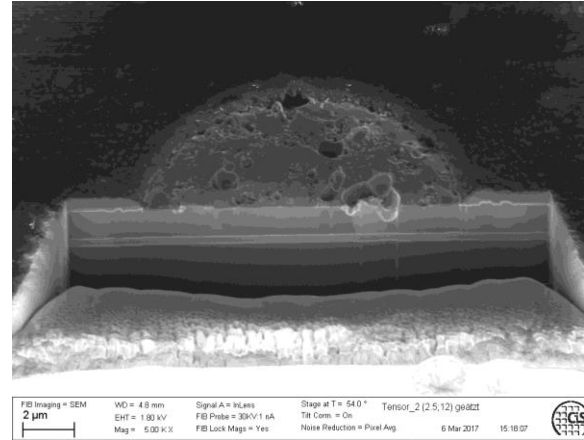


not etched



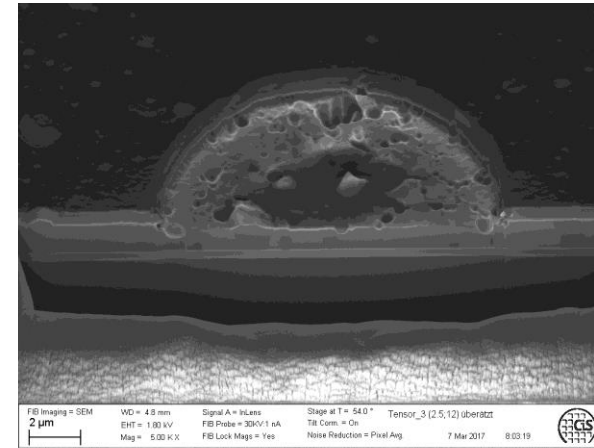
Metal rail (fuse) clearly visible

etched



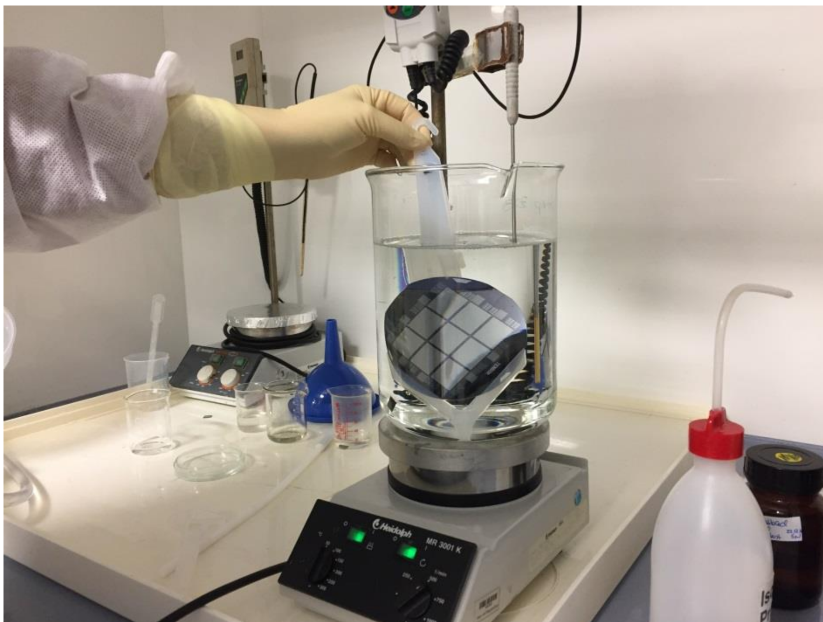
Fuse etched away

over-etched



Twice the etching time of „etched“

Bias rail alternatives
└ etching tests: results

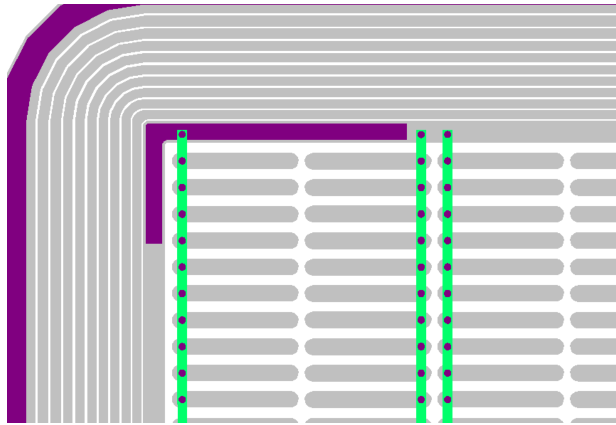


- Etching successful
- Very promising: even with significant over etching acceptable

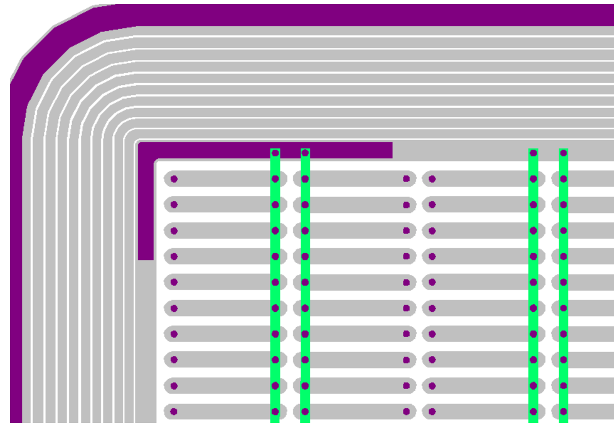
- With new layout promising cheap alternative
- More reproducible and cleaner than burning out (as expected)

Bias rail alternatives

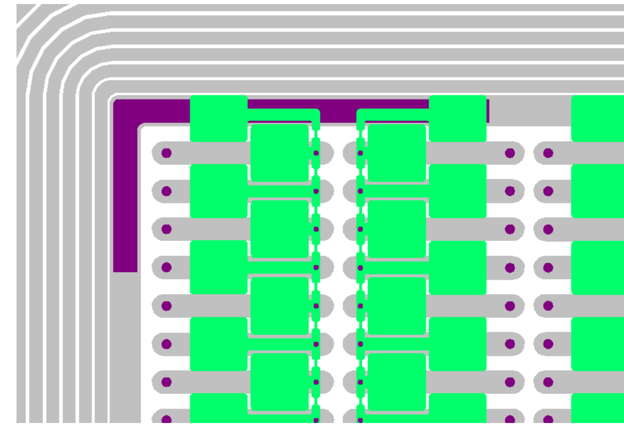
└ sensor wafer run: variants



Bias rail over bump openings



Bias rail oposite of bump openings (same position as punch through in conventional FE-I4)



With pads for needle prober access

Bias rail alternatives
└ summary

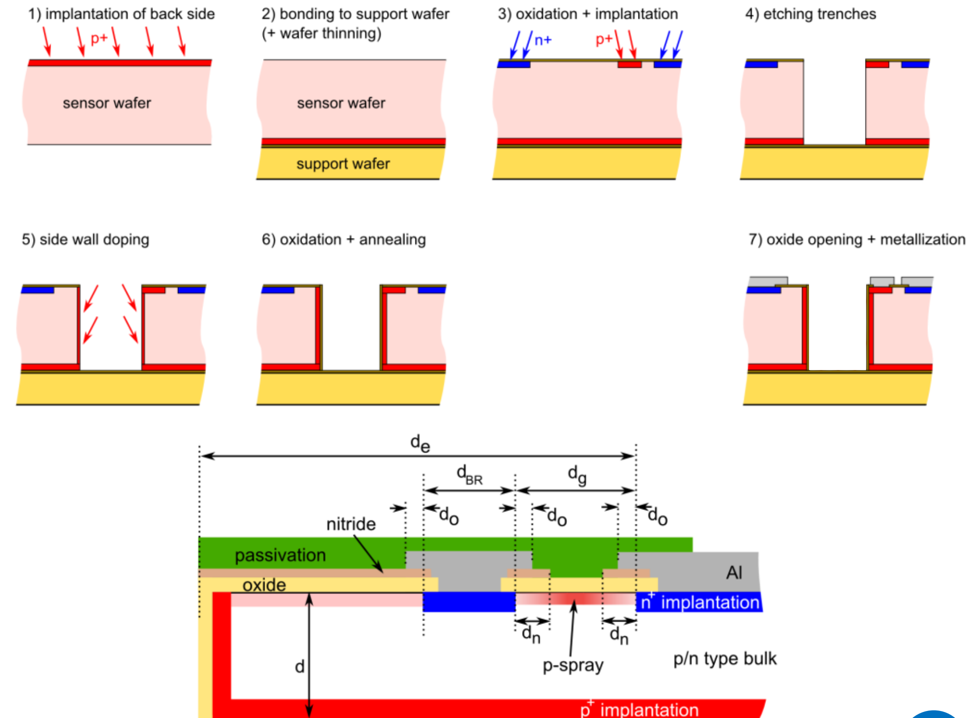
- Burning tests with dummy wafer run expectedly not very reliable
- Etching tests very promising: reproducible results with low risk of failure
- Sensor wafer run being finished this week

Outlook:

- Initial characterization: is temporary metal suitable for IV-measurements?
- Flip chipping with FEs and glass wafer dummies
- Tests with x-ray source

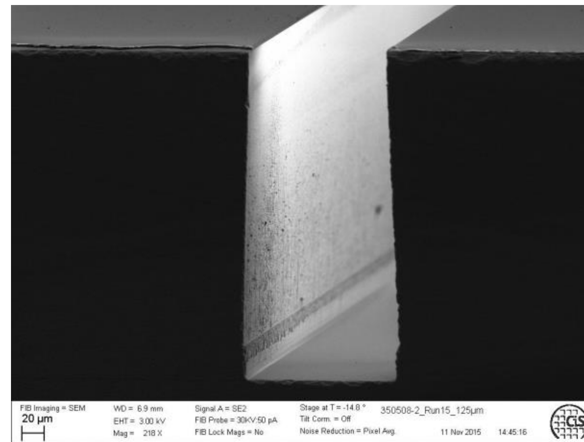
Active edges
└ wafer run

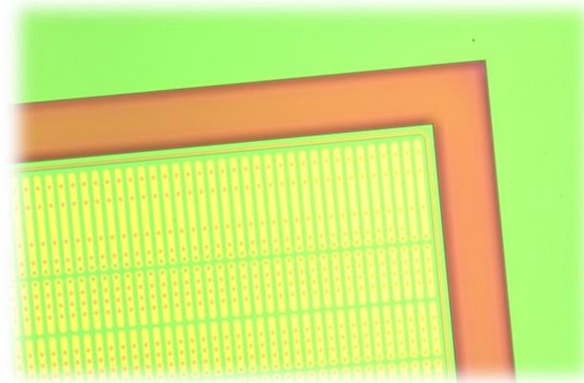
- reduction of inactive sensor edge by doping of side walls
- several parameters are varied
  - p- and n-type bulk
  - sensor thickness (300 & 100µm)
  - three side wall doping methods
  - trench widths
- numerous edge designs had been simulated
  - most promising ones were implemented in the layout



Active edges
└ wafer run

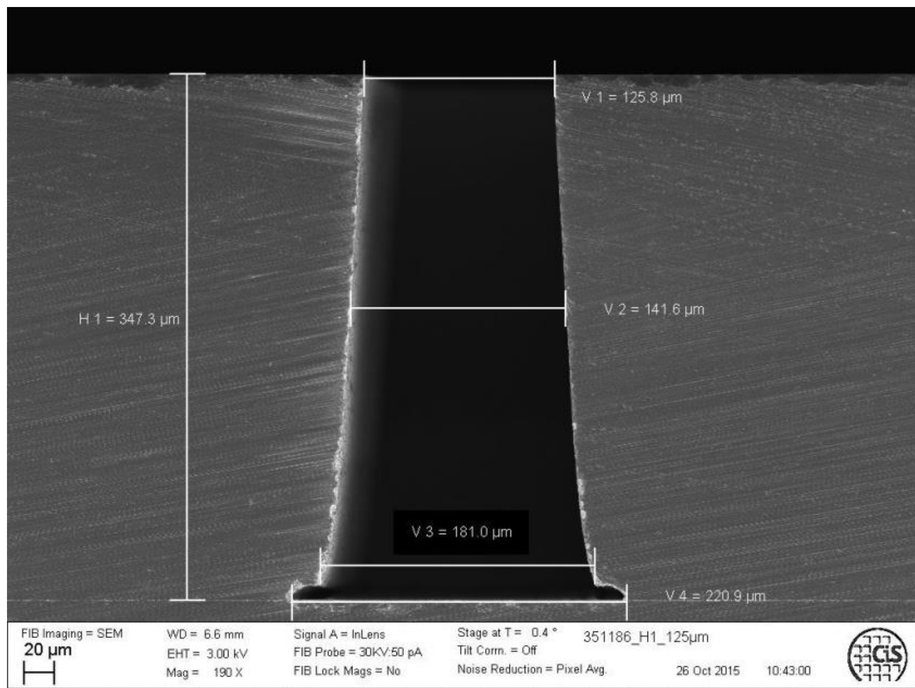
- ICP trench etching step was challenging
- didn‘t have much experience up to now
- dummy trials to adjust etching parameters
- optimized the etching homogeneity at the wafer edge
- most of the side walls look fine

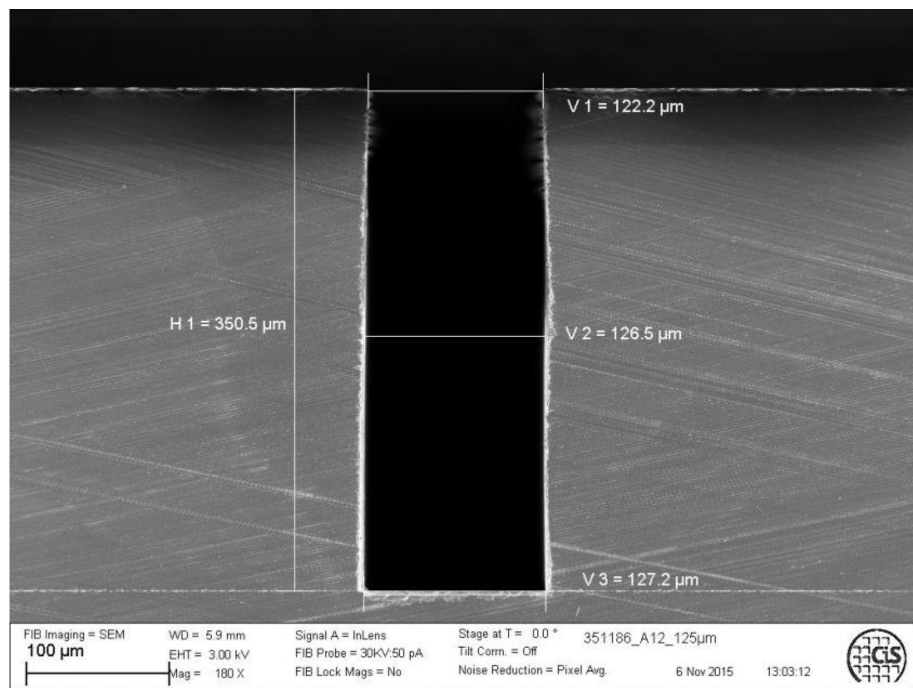




Active edges

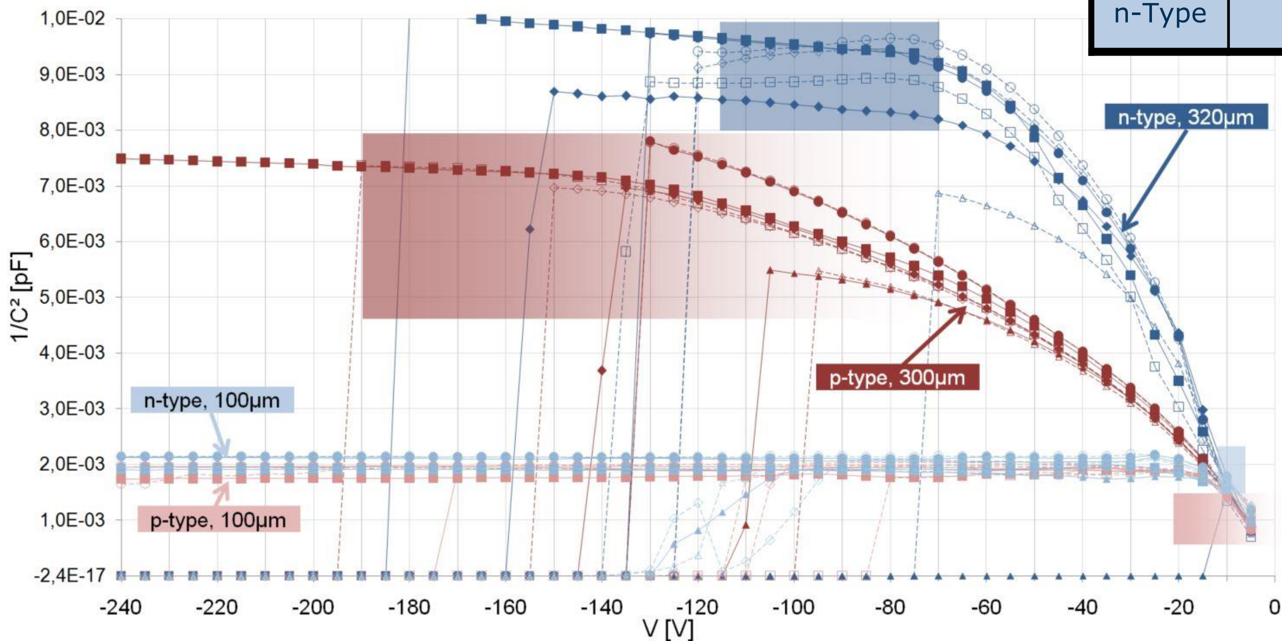
└ wafer run: optimization of trench geometry





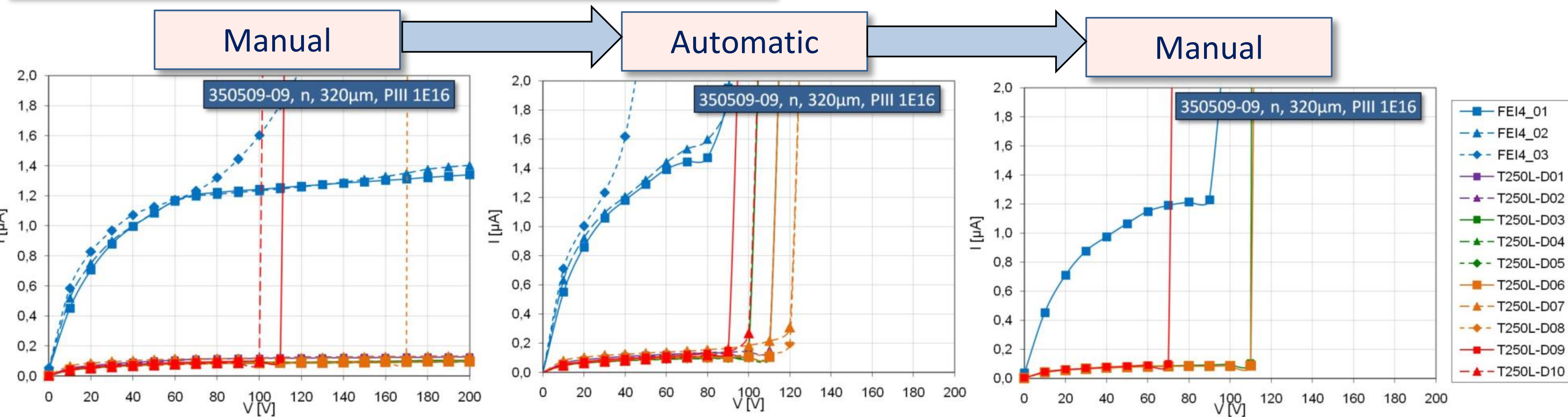
Active edges
└ wafer run: CV measurements

	Thickness [µm]	V_{depl} [V] Calcul.	V_{depl} [V] measured	V_{op} [V]
p-Type	300	<190	130	170
p-Type	100	<21	<20	50
n-Type	320	70...115	60	100
n-Type	100	7...11	<20	50



- Measured V_{dep} fit to calculated values
- Thick wafers V_{depl} up to 130V
- Thinned wafers V_{depl} as low as 20V

Active edges
└ wafer run: IV measurements

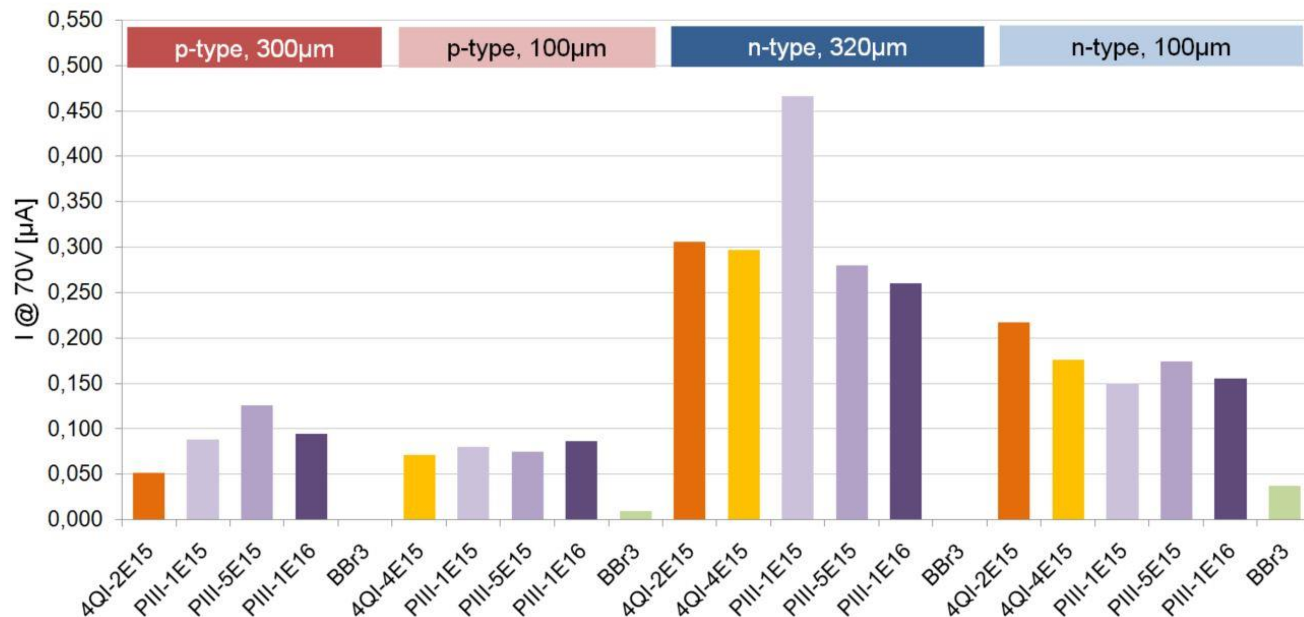


- Random selection, measured manually
- Excellent results
- No breaktroughs under 200V for most diodes

- Systematic automatic measurement
- Inconsistencies between curves
- Majority of sensors break through at ~80...120V

- Manual Cross-Check
- Early breakthroughs remain
- Assumption: sensors were affected/damaged irreversibly by automatic prober

Active edges
└ wafer run: implantation variants



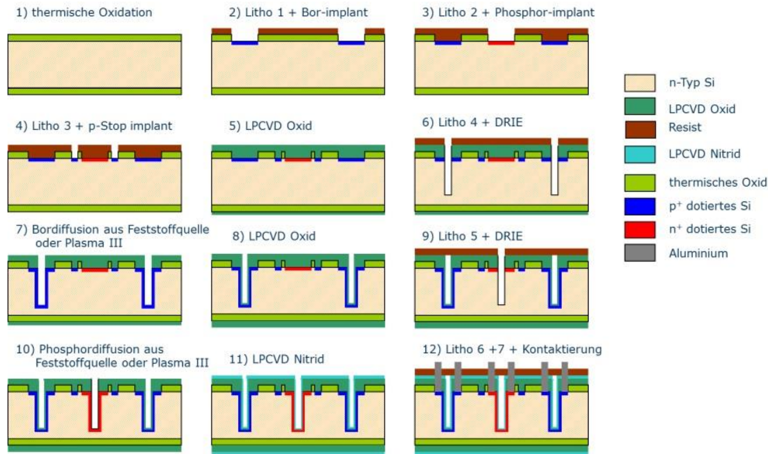
Leakage currents @ 70V

- No significant differences between 4QI and PIII
- BBr_3: Faktor 10 (p-type) ... 5 (n-type) smaller
- Matches doping profiles
- Otherwise substrate material more influence
- n-type material of inferior quality?

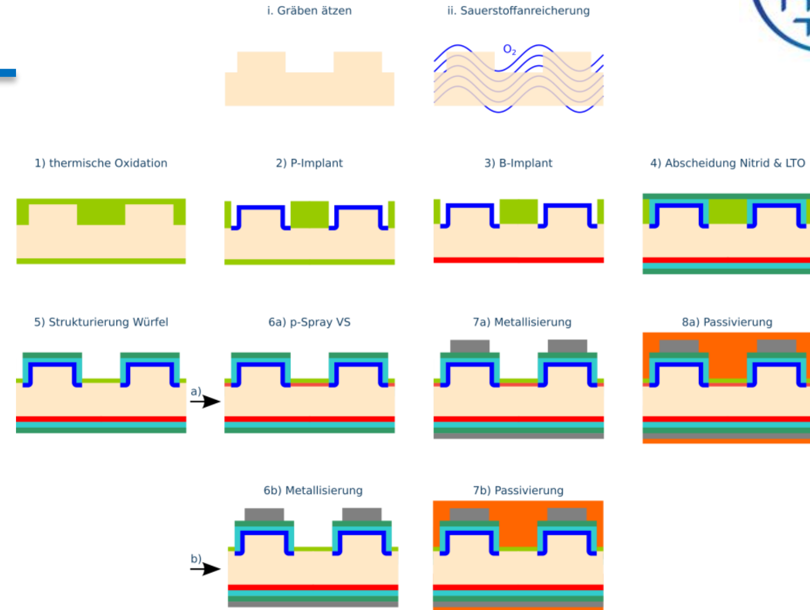
Active edges
└ summary

- Technological development & processing of active edge sensors successful
- Even after obviously damaged (by automatic prober), thinned sensors have excellent yield with up to 90 % for d_e=50µm
- Significant reduction in yield only for d_e=30µm
- No disadvantages with thinned sensors
- Implantation Variants:
  - **4QI:** Reliable and reproducible, no disadvantages with larger angles
  - **PIII:** IV results good, doubts concerning doping profiles (susceptible to mechanical defects?)
  - **BBr_3:** many advantages in principle (high and deep doping, lower leakage currents)

Trench detectors and 3D
└ new project sneak peak



3D-sensor process



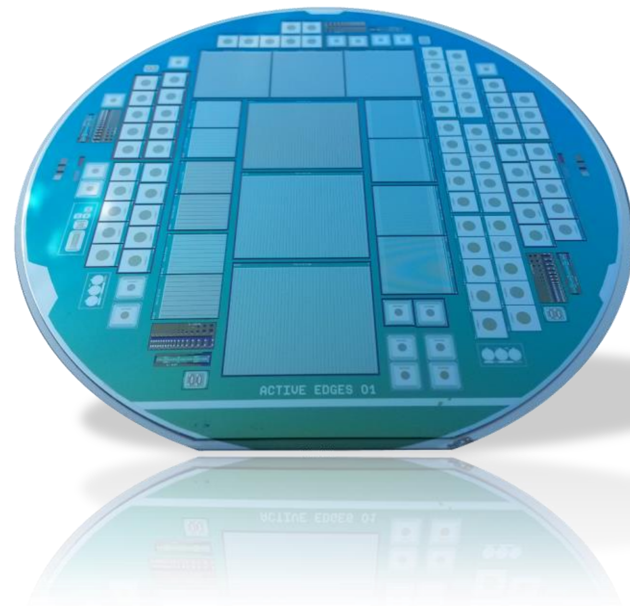
Planar „trench detector“ process

Aim: establish 3D-sensor processing at CiS while developing a versatile prototyping technique for variable geometries

Summary

CiS is developing several different technologies to be able to cope with future HL-LHC challenges

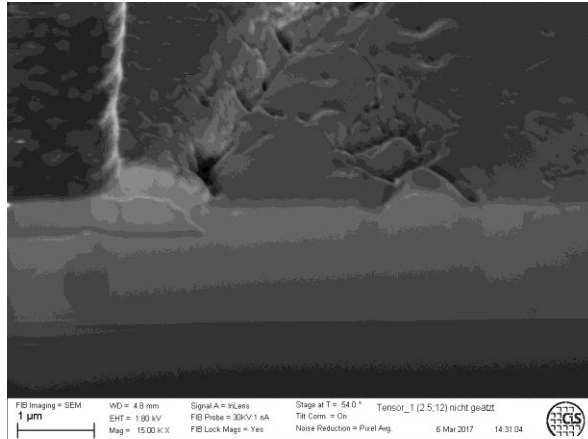
- Active Edge project completed
- Alternative biasing methods for pixels: sensor wafer run to be finished
- New project: 3D processing



Backup
└ etching tests

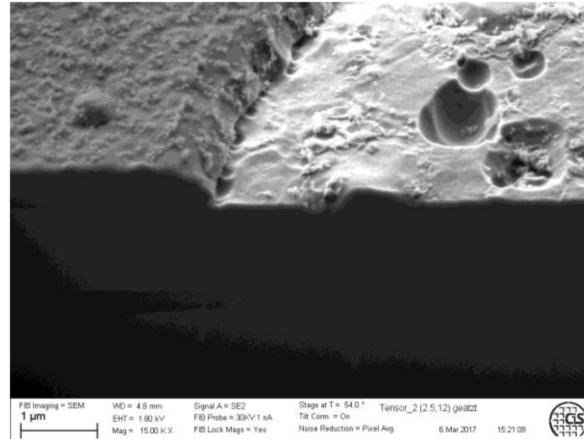
not etched	etched	over-etched

not etched



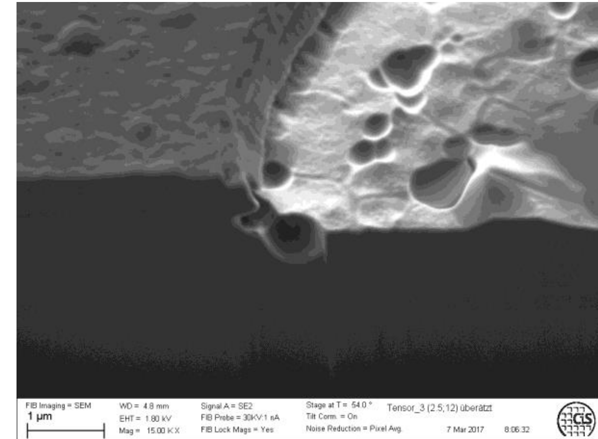
Metal rail (fuse) clearly visible

etched



Fuse etched away

over-etched



Twice the etching time of „etched“