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E-TCT characterisation of irradiated backside biased H35DEMO pixel demonstrators

A Phase II upgrade is proposed for ATLAS to take full advantage of the upcoming High Luminosity-LHC (HL-LHC). High Voltage-CMOS (HV-CMOS) pixel detectors are considered for the outer pixel layers of the Inner Tracker (ITk), where detectors will need to cover a large area and withstand irradiation to fluences of the order $10^{15} n_{eq} cm^{-2}$. Monolithic HV-CMOS detectors remove the need for the expensive assembly processes required by hybrids, as the front-end electronics can be directly embedded in the sensor chip. Sensing diodes can be biased at high voltages for fast charge collection by drift and high radiation tolerances. However, as recent measurements have demonstrated, the maximum achievable tolerance is about one order of magnitude lower than that of hybrids.

The H35DEMO is an HV-CMOS pixel demonstrator in the 0.35 μm process from ams AG and fabricated in different substrate resistivities between 20 $\Omega \cdot cm$ and 1 $k\Omega \cdot cm$. A 1 $k\Omega \cdot cm$ wafer of H35DEMOs was thinned to 100 μm and processed to allow backside biasing. This contribution presents results of edge-TCT measurements of the processed H35DEMO sensors before and after irradiation to fluences up to $2 \times 10^{15} n_{eq} cm^{-2}$. The measured results are in line with those obtained with TCAD simulations which indicate that backside biased H35DEMO sensors have a stronger more uniform electric field, giving faster charge collection times and therefore higher radiation tolerances than top biased counterparts. Further studies of backside processed H35DEMOs irradiated to fluences beyond those expected in the outer pixel layers of the ATLAS ITk are currently planned.

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