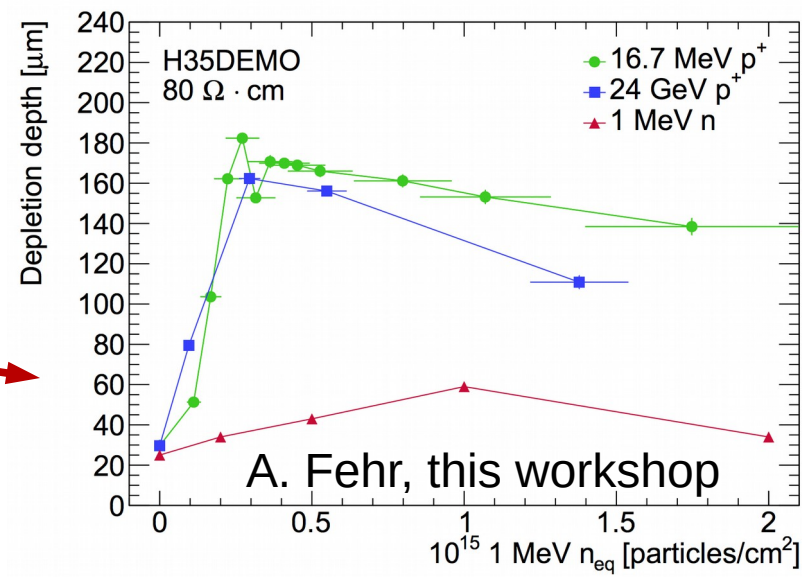


edge-TCT results from AMS H18 HV-CMOS
test chips irradiated with 800 MeV protons

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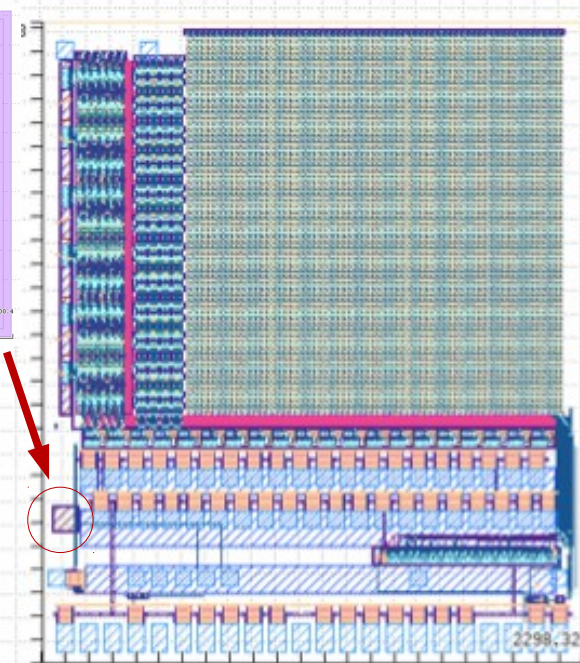
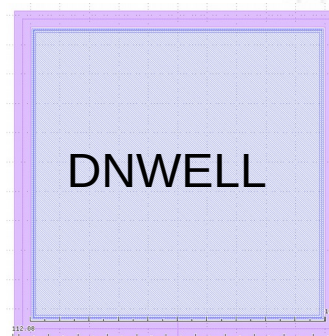
What is this presentation about?

- Irradiation “habits”: neutrons
 - In our community, we often irradiate with reactor neutrons as it is (thanks to our Ljubljana colleagues) convenient, fast and reliable
 - In the HL-LHC (pixel), however, we are expecting mainly charged hadrons of $o(100 \text{ MeV})$ – even at the outermost pixel layer they are still dominating ($>50\%$)
- CMOS foundry default substrates: $10\text{-}20 \text{ } \Omega\text{cm}$
 - In recent years, it has been shown with several foundries that CMOS processes can be used to create radiation-tolerant drift-based monolithic sensors (DMAPS/HV-MAPS)
 - The standard substrates, which are accessible for prototyping at a very affordable price ($\sim 10 \text{ kEUR}$) via Multi-Project Wafer submissions (MPWs), are often low(er) resistive than we are used to – typically $10\text{-}20 \text{ } \Omega\text{cm}$
 - These substrates have been found to behave different from the high-resistive FZ substrates we are used to – strong acceptor removal has been observed, leading to an increasing depletion depth
 - Neutrons and protons have quite different behaviour!



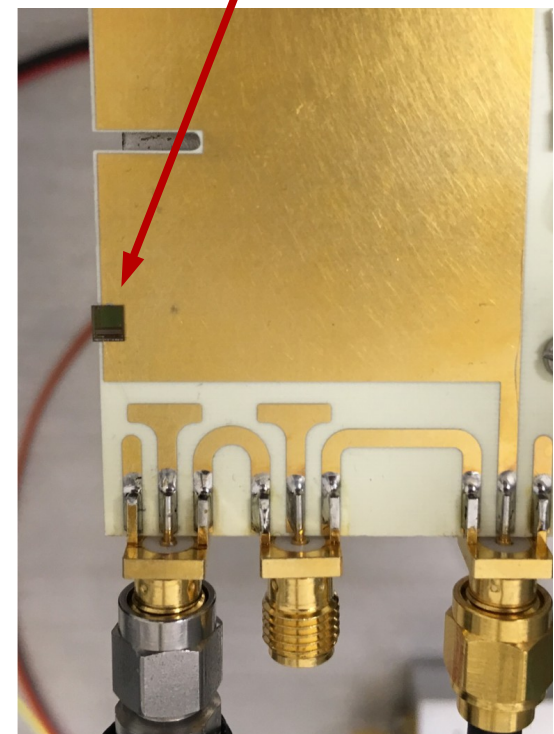
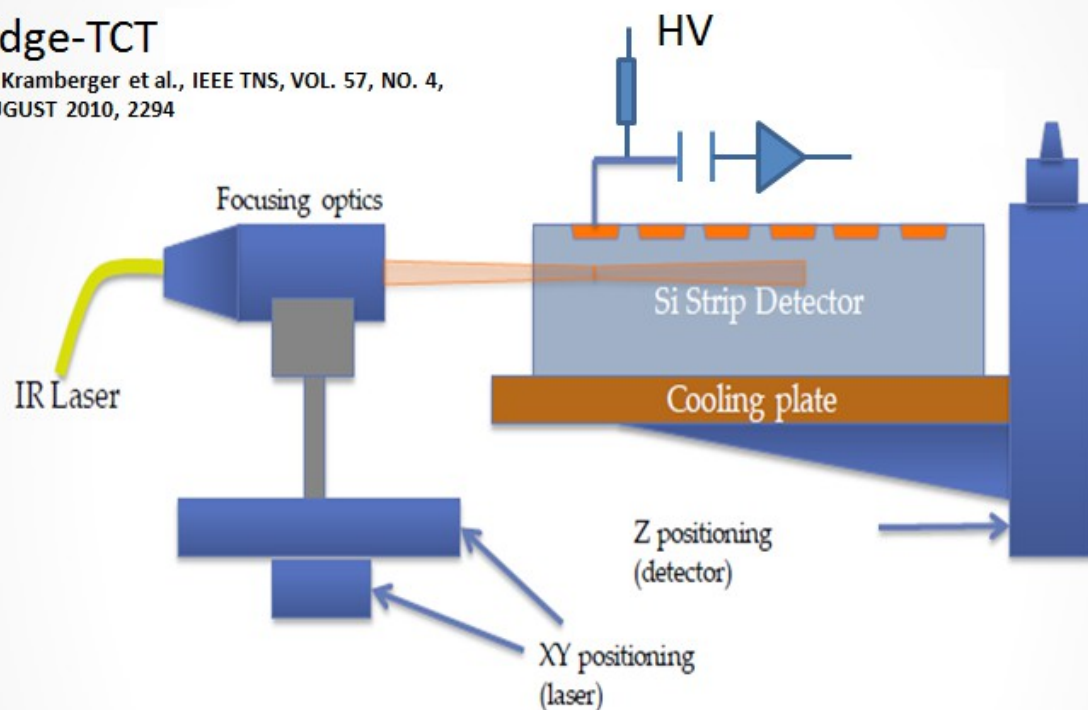
What did we do?

- Used ams H18 CCPDv3 HV-CMOS test chips from an MPW (I. Peric)
 - contains 100 μm x 100 μm passive diode, 10 Ωcm substrate
- Irradiated with 800 MeV protons at LANSCE (thanks to S. Seidel and M. Hoferkamp!)
- Performed edge-TCT measurements to characterise depletion depth and signal



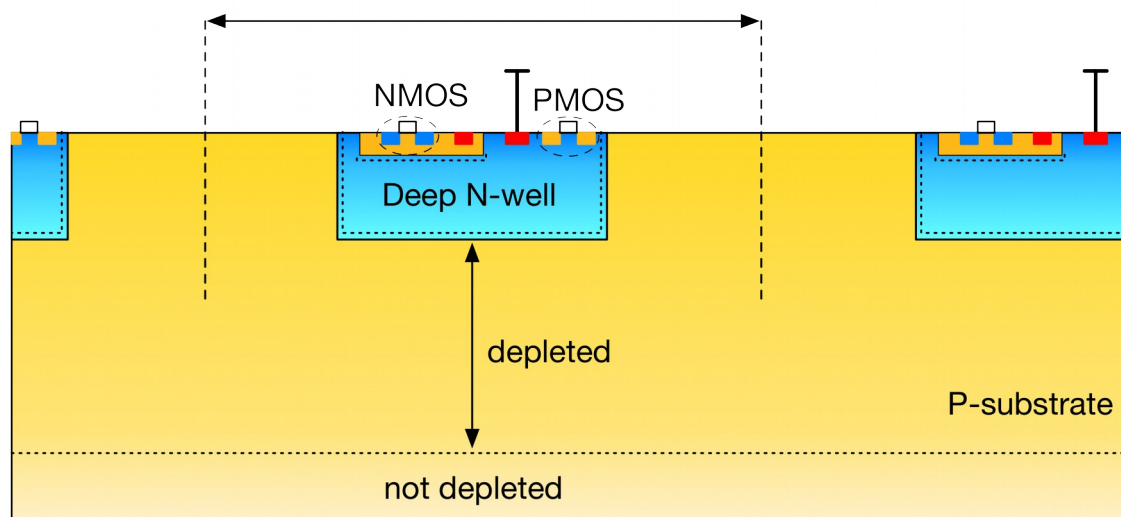
Edge-TCT

G. Kramberger et al., IEEE TNS, VOL. 57, NO. 4, AUGUST 2010, 2294



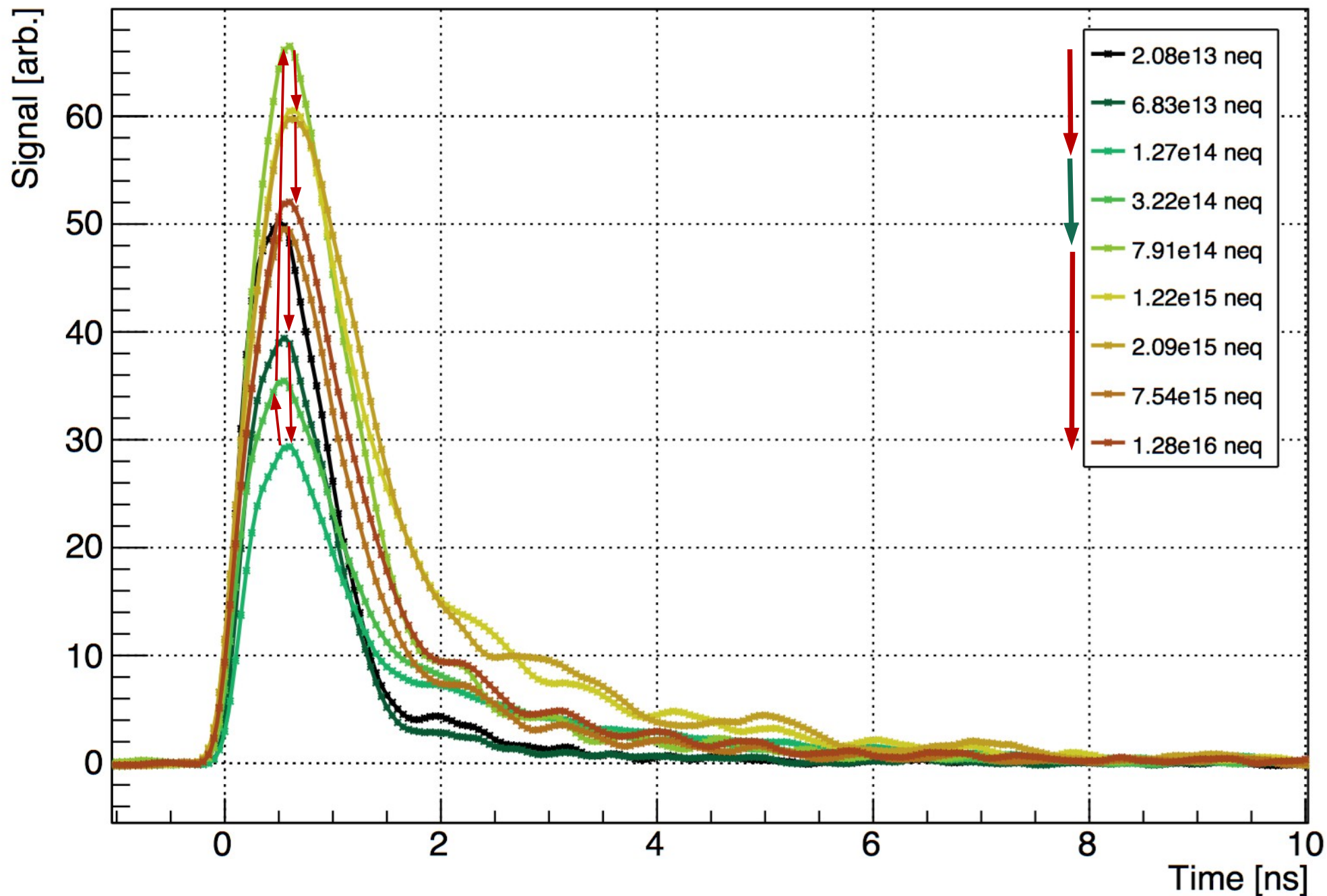
What did we do?

- Some more details:
 - the diode only utilises a deep N-well, but contains no logic
 - was placed close to the edge for eTCT and bulk characterisation



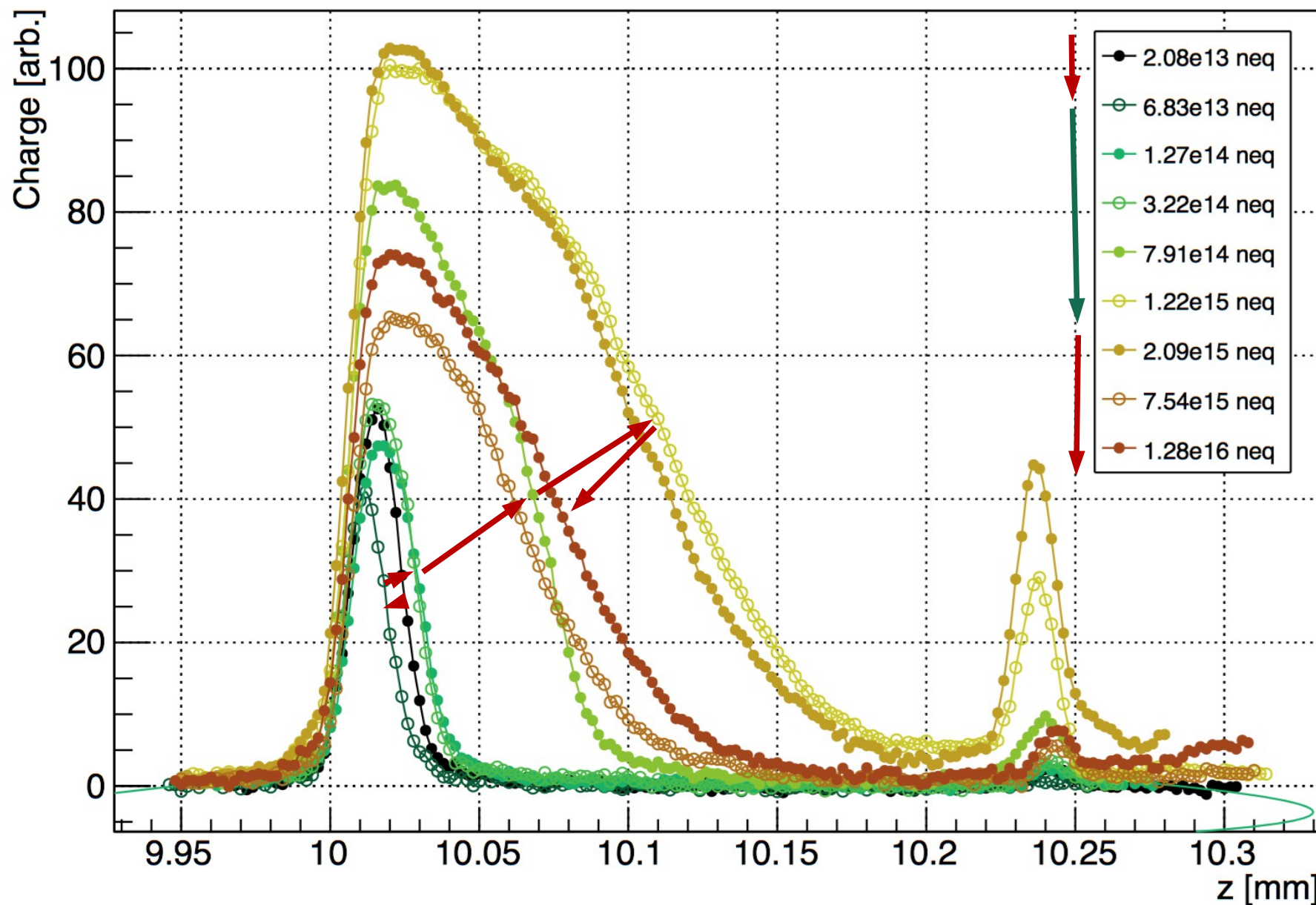
- 9 fluences from 2.1×10^{13} to $1.3 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^3$
- chip is thinned by the foundry to $\sim 250 \text{ }\mu\text{m}$, but not backside processed
- chip backside is connected to the HV plane using conductive glue
 - this indeed establishes a contact – in spite of no processing, implant or metal
 - but low-resistive silicon bulk!
 - minor differences with/without top side biasing
 - might be an option for contacting, but beware of issues when approaching “full depletion”!

Waveforms – sidewall not polished!

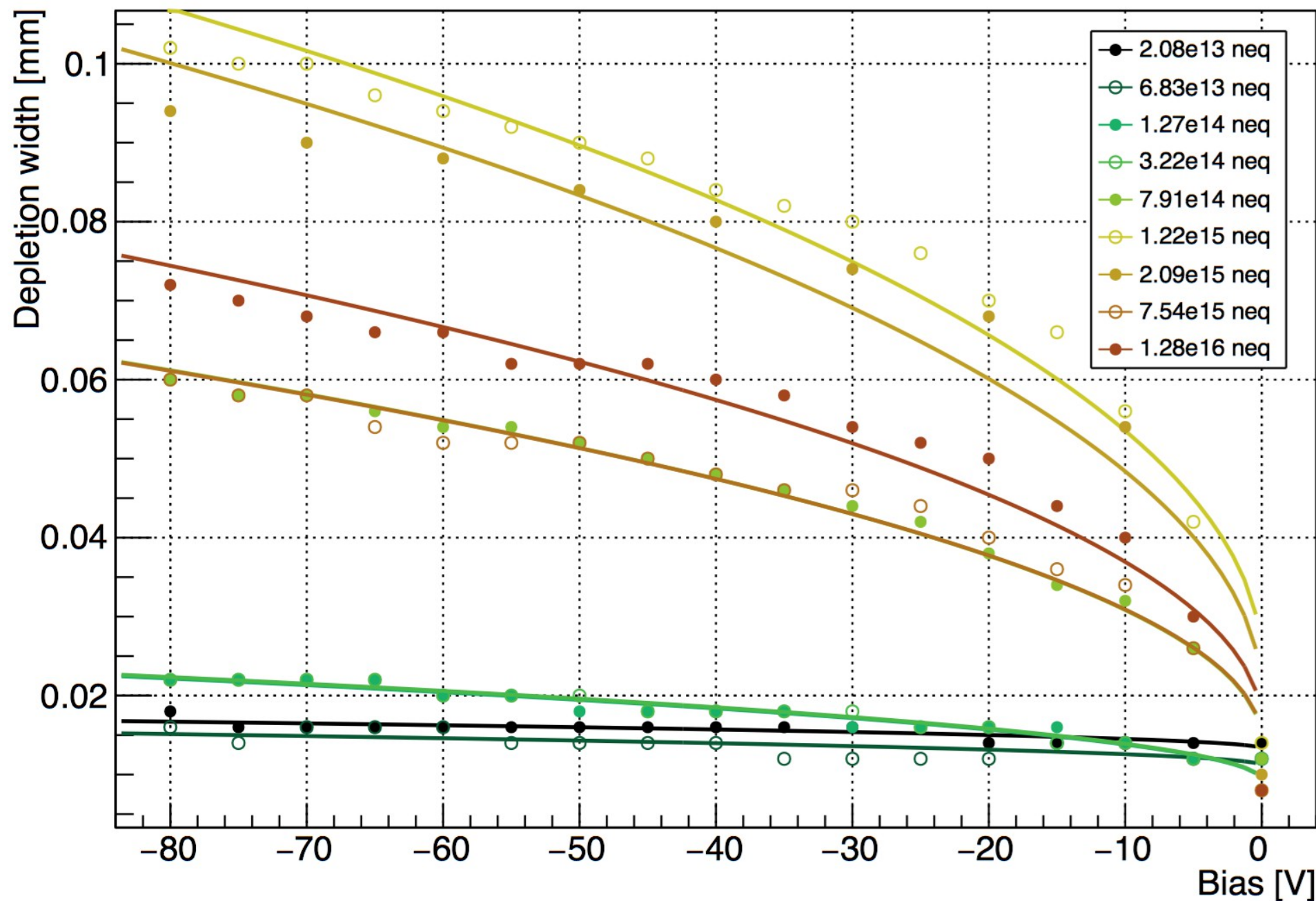


z-profiles

Charge collection in 8 ns in proton irradiated HV-CMOS at -80 V bias

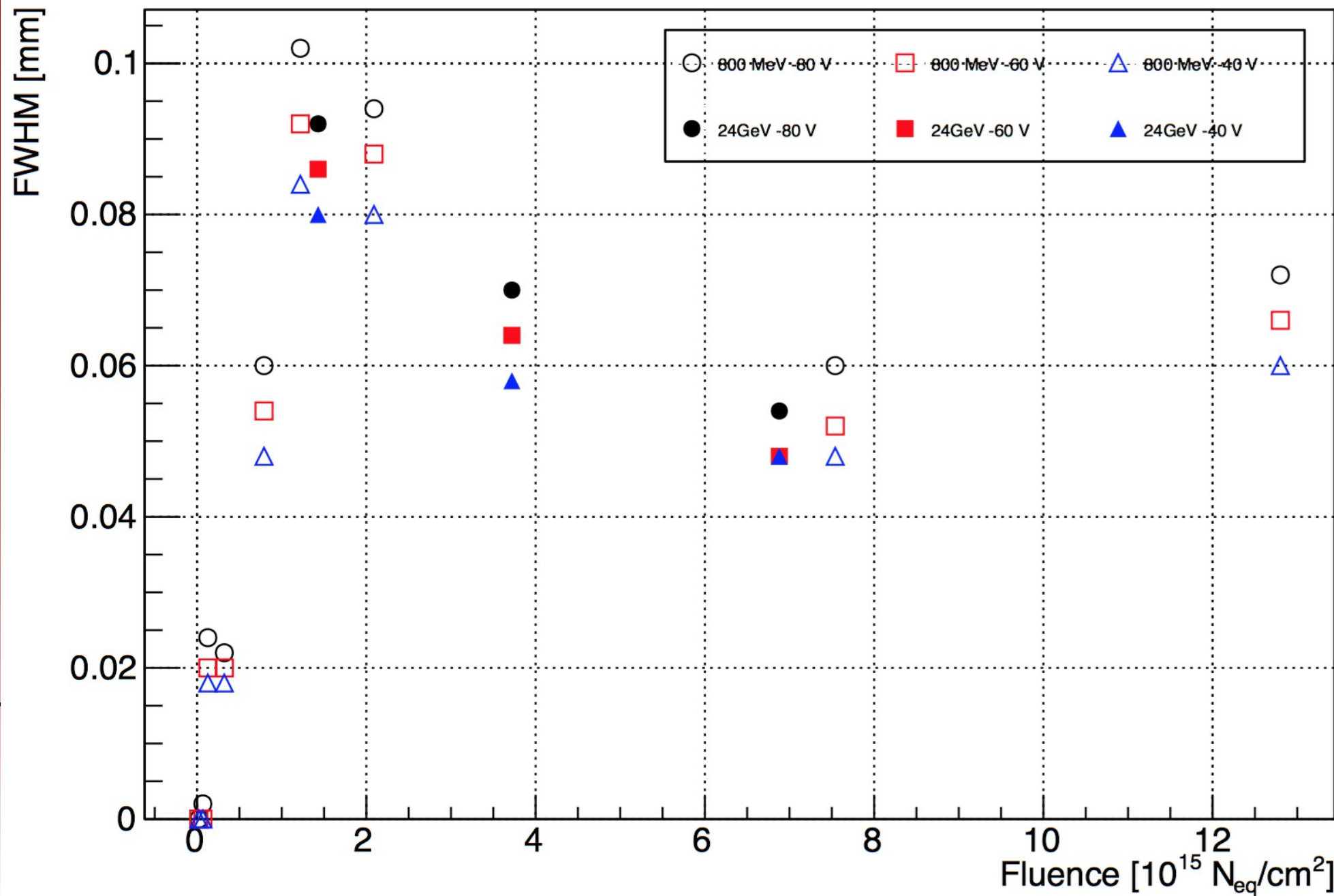


Depletion depth



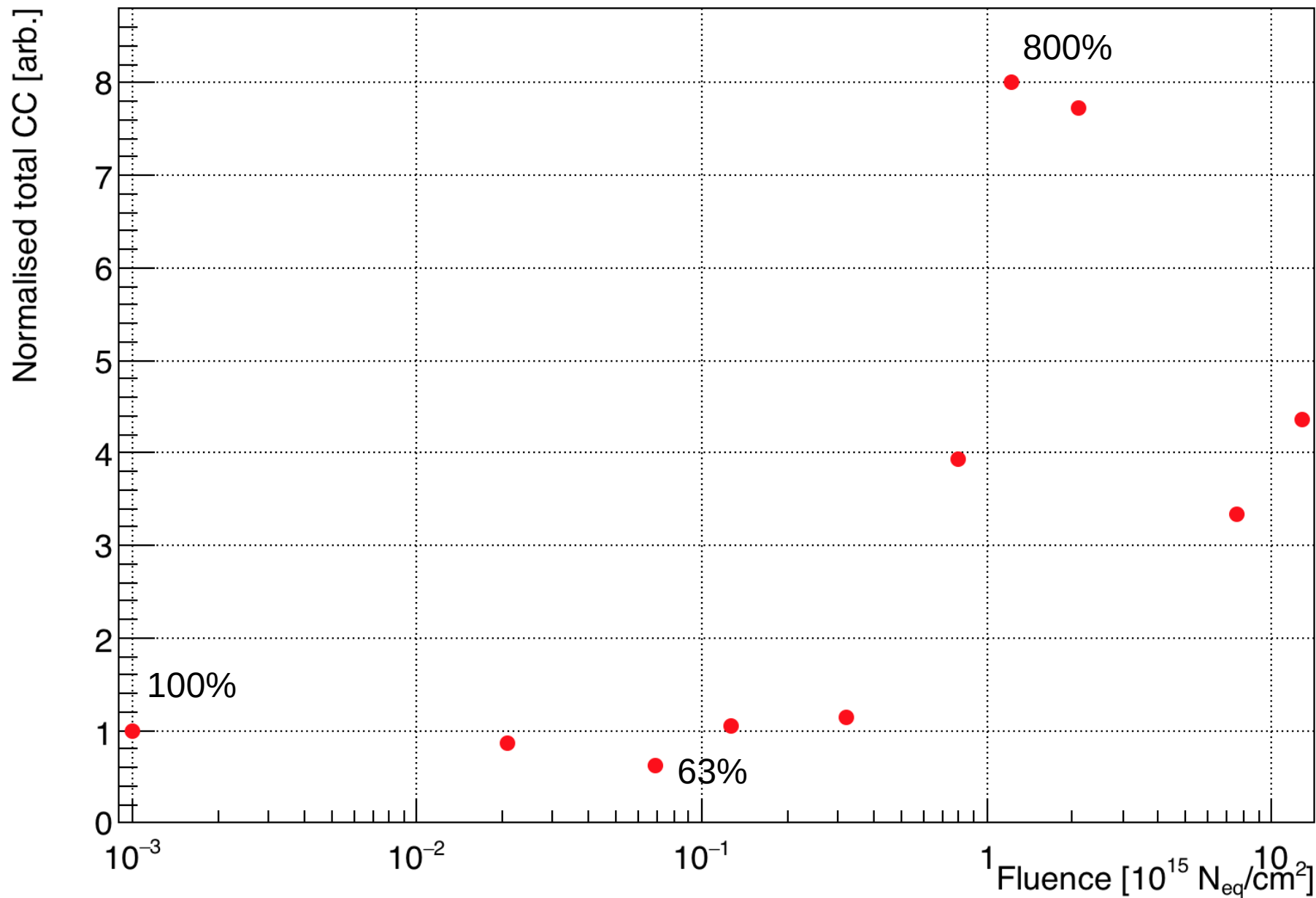


Depletion depth



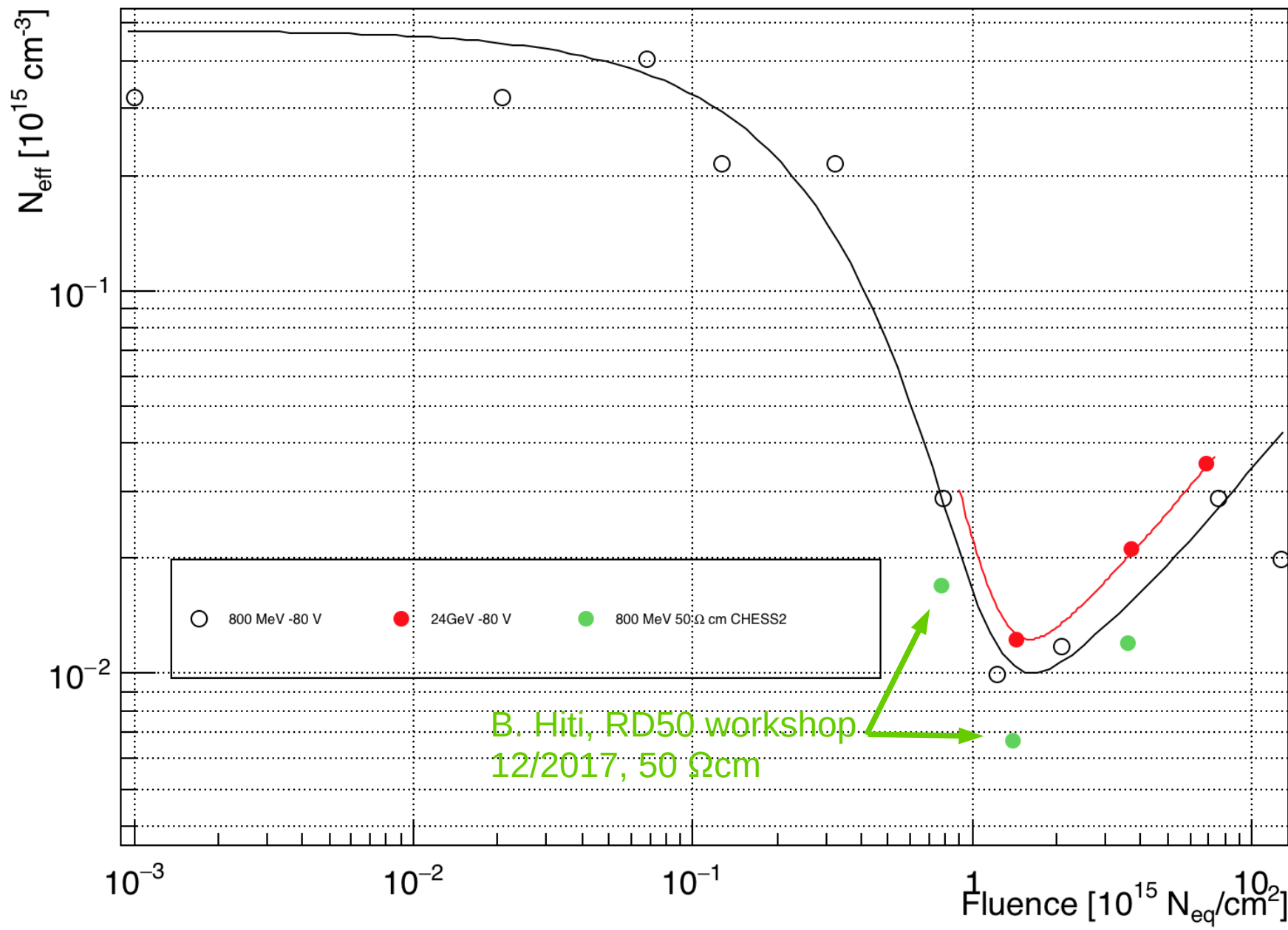
Total collected charge (integral over z) vs. fluence

Total charge collection in 8 ns, normalised to unirradiated value and excluding CC at back



N_{eff} evolution

Effective doping concentration calculated from CC in 8 ns



Conclusions and outlook

- Acceptor removal is much stronger with charged hadron irradiation
 - 800 MeV protons are closer to HL-LHC case than 24 GeV or 18 MeV, but results are (luckily!) similar
 - “valley of tears” around $\sim 7 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$ for 10 Ωcm substrate
 - if this can be survived with good efficiency, then collected charge should be much larger until $> 1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ (!)
- For default substrate resistivities of 10 Ωcm
 - depletion zone starts to grow after $\sim 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$
 - maximum reached at $1\text{--}2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
 - still $\sim 70 \mu\text{m}$ width after $1.3 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$
 - not really unsuitable for HL-LHC – if your sensor survives the “valley of tears”, it will survive until the end-of-life
- Samples without backside processing can be contacted via conductive glue, provided the depletion zone does not reach the surface
- Mixed irradiations to mimic realistic environment to follow

