A study of SEU-tolerant latches for the RD53A chip

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Outline

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
CPPM

- Introduction
- SEU test chip description
- Test Set-up description
- Flavor of latches
  - Hamming code version
  - Hamming code results
  - DICE latches versions
  - DICE latches results
  - TRL latches versions
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- Influence of the Deep NWell
- Proposal of SEU tolerant latches for the pixels of the RD53A chip
- Conclusion

introduction

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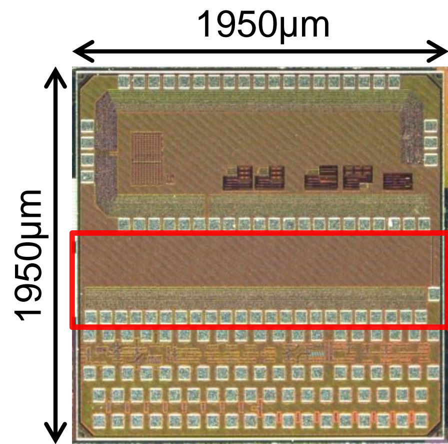
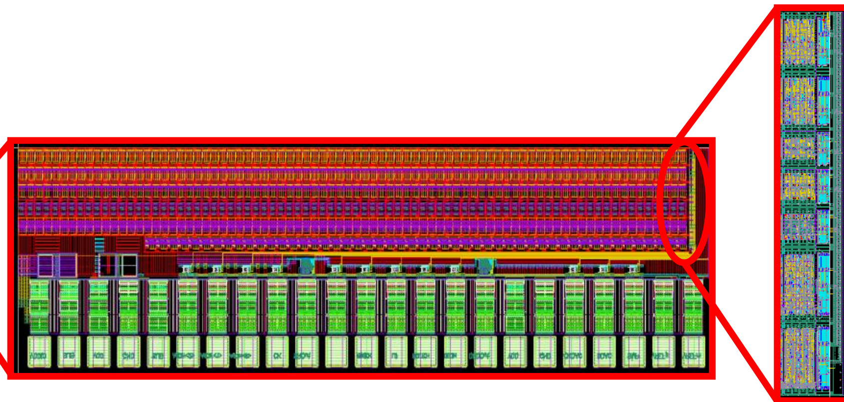
- RD53A main characteristics:
  - 160k pixels x 8 configuration bits=1.28M latches in totally
  - Technology: TSMC 65nm
  - TID 500 Mrad – 5 years (total fluency 10^{16} p/cm²)
  - Peak fluency ~ 0,5.10^9 particles/cm²/s for the layer 0 (3.7cm)
- The SEU immunity for this highly scaled process should be carefully considered because the device dimensions are small and the capacitance of the storage nodes becomes very low.
- Hardened By Design (HBD) approaches are used to reduce the effect of single bit upsets
- 3 flavors of structure have been designed and tested
  - Hamming code,
  - Triple Redundancy Latches (TRL) cell,
    - ✓ Particular attention to the global nodes
  - Dual Interlocked CEll (DICE).
    - ✓ Sensitive to the charge sharing
- The last SEU prototype chip allows to measure the influence of a deep N well on the digital part
- Experimental test set-up
  - Irradiation tests were carried out at CERN using the IRRAD proton facility is located on the T8 beam-line (PS East Hall bldg 157)

SEU test chip



65nm chip prototype

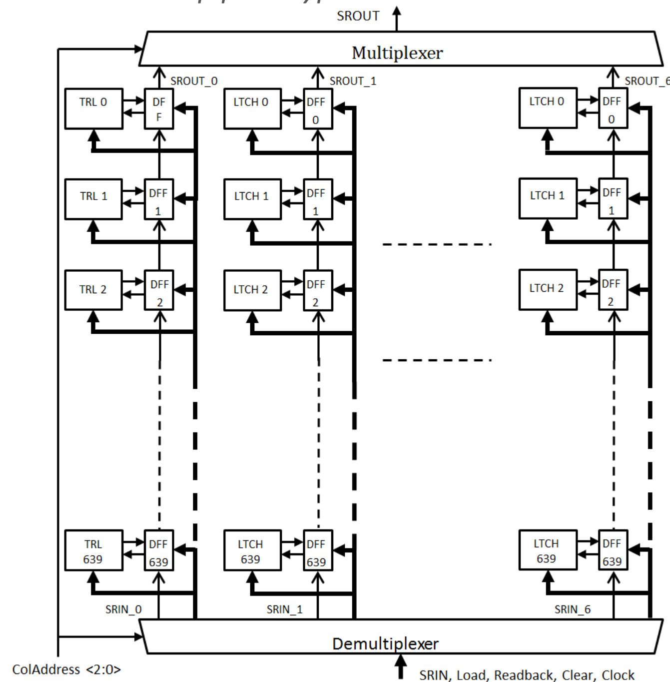


Example of a SEU layout

- ❑ Clmn1
- ❑ Clmn2
- ❑ Clmn3
- ❑ Clmn4
- ❑ Clmn5
- ❑ Clmn6
- ❑ Clmn7

PIN NAME	IN/OUT	Description	Comments
ClAdd<2:0>	IN	Column selection	1 column selected at the same time
LD	IN	Load	Data loading
CK	IN	Clock	
RDBCK	IN	ReadBack	Latches data loading in SR
CLR	IN	Clear	Reset
SRIN	IN	SR Input	
SROUT	OUT	SR Output	Buffered signal (C_{LOAD} = 10pF)

I/O pins of the SEU chips

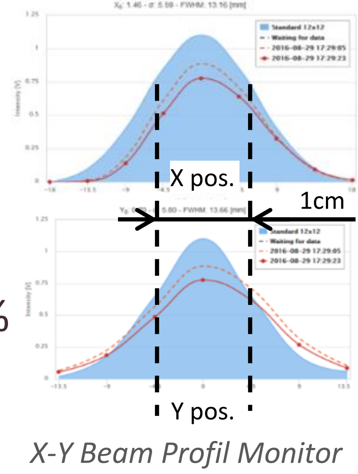


Synoptic of a SEU chip

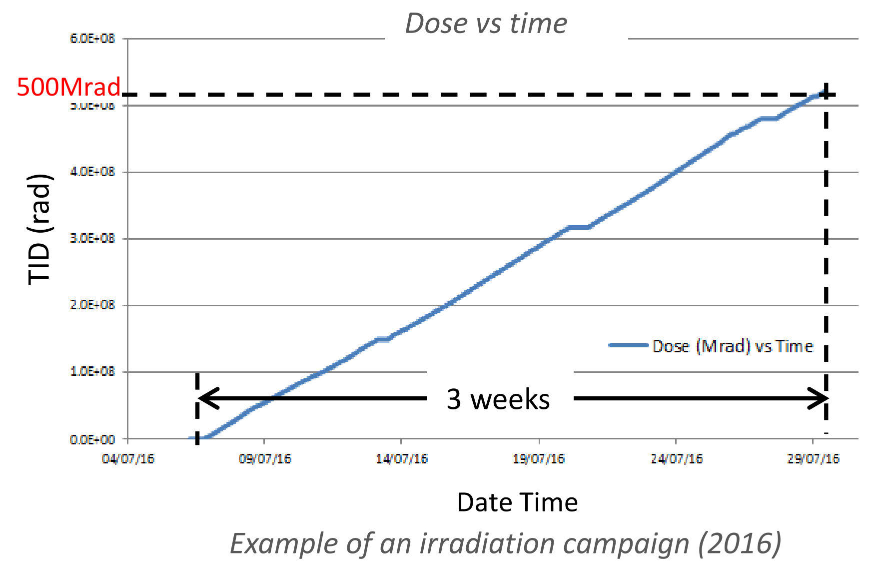
- ❑ 3 SEU chips have been designed and allow to collect all datas from latches and directly compare their behavior during irradiation tests.
- ❑ The SEU chip is sub-divided in several columns
  - ○ Typically 640 cells per kind of latches
  - ○ 8 Inputs, 1 output needed to monitor the chip (shown on the table above)
- ❑ Custom patterns are written and read through a shift register (cf.: synoptic) in synchronization with the beam.

Experimental test set-up

- 24 GeV protons beam line at CERN (east zone PS)
  - 12.10^{10} protons/cm²/spill
  - beam size 1cm²
  - mean dose rate
    - ✓ 950krad/h
  - TID: 500Mrad (10^{16}p/cm²) ± 7%
  - exposure time 3 weeks

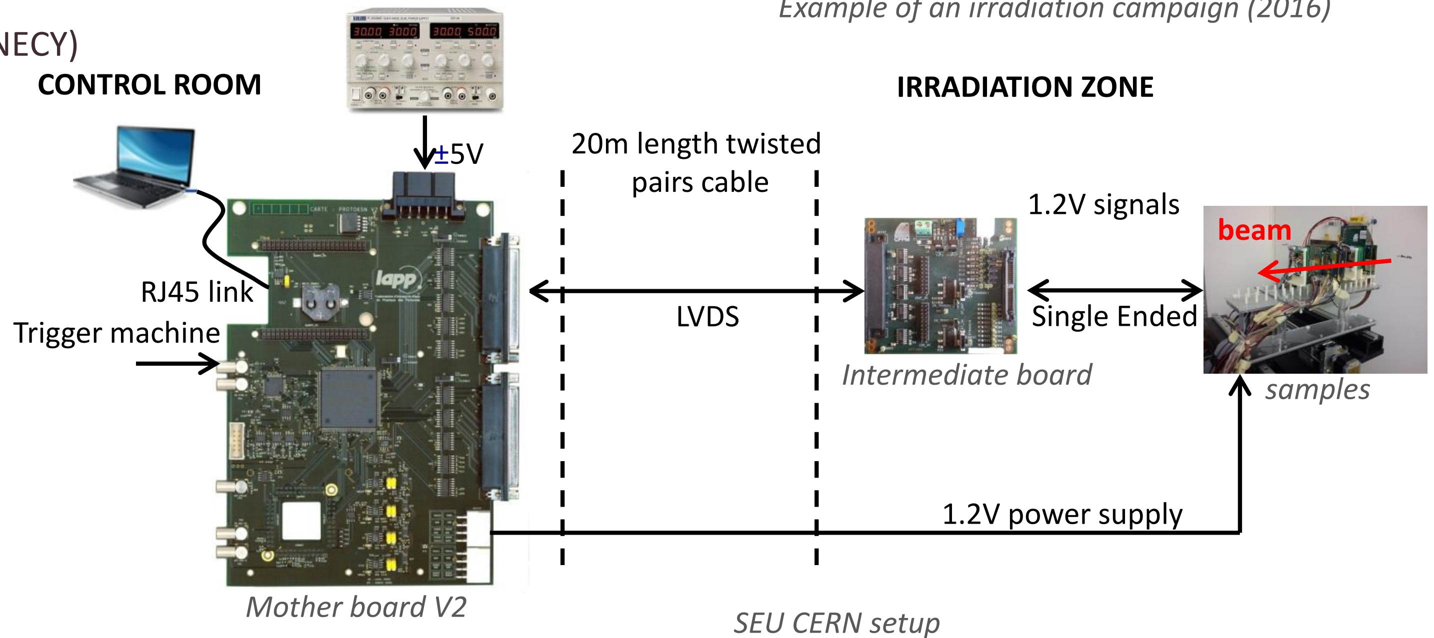


X-Y Beam Profil Monitor



Example of an irradiation campaign (2016)

- Mother board V2
  - Collaboration with LAPP (IN2P3 ANNECY)
  - nanoPC BeagleBone card + FPGA
    - ✓ Parallel bus GPMC
  - Flexible programing
  - 40 logic signals TTL + <u>30 LVDS</u>
  - Analog channels
    - ✓ 4 SAR ADC (16 bits)
    - ✓ 10 DAC (16 bits)
  - Monitoring (°C, current supply)
  - Lab tests + <u>irradiation tests</u>



Mother board V2

SEU CERN setup

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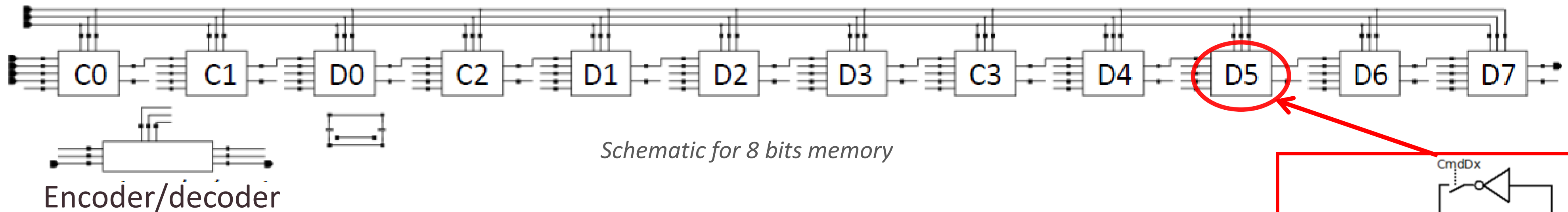
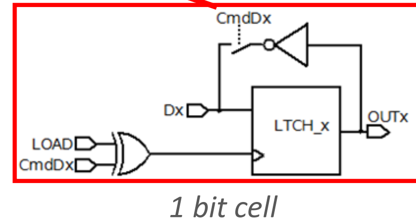
Hamming code version/results



Schematic for 8 bits memory



1 bit cell

- A 8 bits memory in a hamming code version has been designed with the ARTISAN library and tested during a irradiation campaign.
  - It needs 4 parity bits to detect and change 8 data bits. In totally, 12 bits are used for 8 configuration bits.
  - Main drawbacks:
    - ✓ A double error can't correct the data corrupted, only a detection is possible
    - ✓ The dedicated area for the logic isn't negligible but can be optimized by using the VCAD library
    - ✓ The results we obtained show a gain by 13 compared to a standard latch

Cell	Dedicated area	%
Latch	5µm x 8µm	7%
Logic	10µm x 20µm	35%
8 bits memory	18µm x 20µm	65%
Total	28µm x 20µm	100%

Example of an area cost for a 8 bits cell in a hamming code version

Cell	Error rate/spill			gain
	0 → 1	1 → 0	all	
Standard Latch	5.6	2.9	4.2	-
Hamming code 8d+4c	0.467	0.185	0.326	X 13

Obtained results compared with a single latch

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DICE versions

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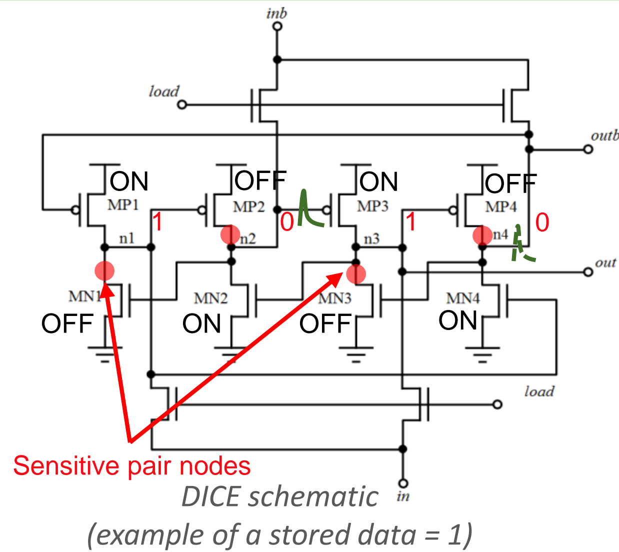
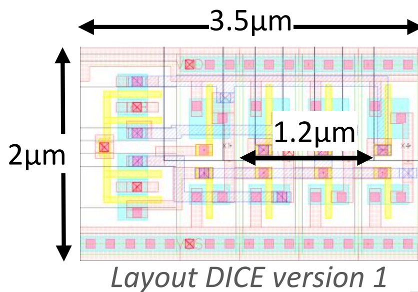


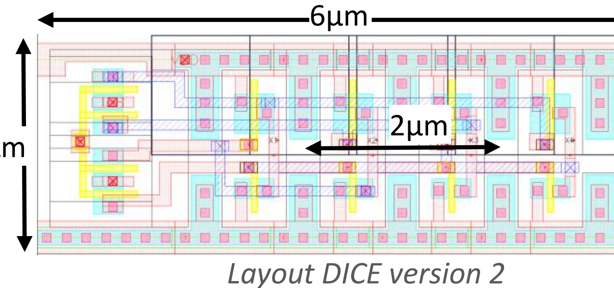
DICE schematic
(example of a stored data = 1)

- DICE latch structure is based on the conventional cross coupled inverters:
  - The charges deposited by a ionising particle strike one node can't be propagated due to the stability of this architecture.
  - If 2 sensitive nodes (corresponding to the OFF transistors drain area) are affected simultaneously, the immunity is lost and the DICE latch is upset
    - ✓ In this case, the equivalent critical charge becomes very low
    - ✓ Spatial distance between 2 sensitive pair nodes (D_{2N}) must be increased
- 4 versions have been submitted:



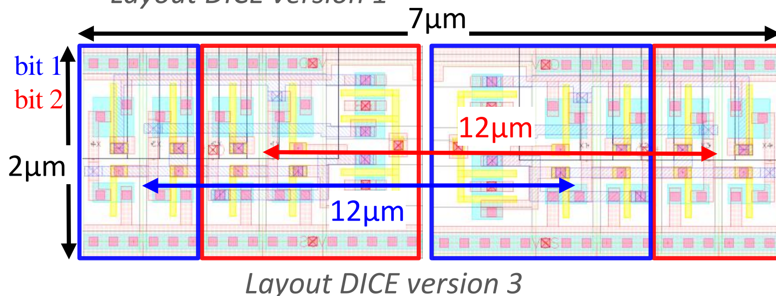
Layout DICE version 1

- Version 1
  - DICE structure
  - W_{PMOS}/L_{PMOS}=400nm/60nm
  - W_{NMOS}/L_{NMOS}=200nm/60nm
  - D_{2N} = 1.2µm



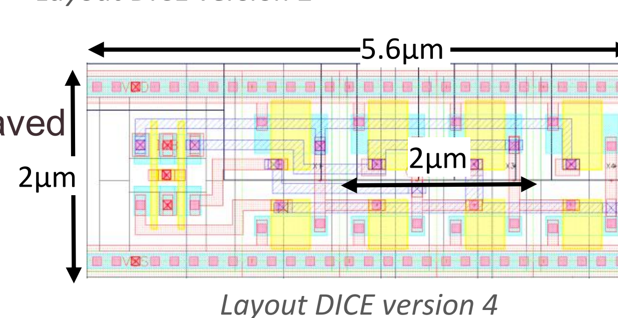
Layout DICE version 2

- Version 2
  - Version 1 + guard rings
  - D_{2N} = 2µm



Layout DICE version 3

- Version 3
  - Version 1 interleaved
  - D_{2N} ↑ up to 12µm



Layout DICE version 4

- Version 4
  - ↑ the size of transistors
  - ↑ the node capacitance
  - W_{PMOS}/L_{PMOS}=400/400nm
  - W_{NMOS}/L_{NMOS}=200/400nm
  - D_{2N} = 2µm
  - Interleaved version has been tested

DICE latches results

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version 2	DICE with guard rings
version 3	DICE interleaved
version 4	DICE with large size of transistors
version 4bis	version 4 interleaved

reminder of DICE version

Cell	Area ratio: $\frac{\text{memory (8 bits)}}{\text{pixel }(50\times50\mu m^2)}$	Error rate/spill			Gain
		0 → 1	1 → 0	all	
Standard latch W_{pmin} = 300nm	2%	2.58	2.29	2.43	-
DICE (version 1)	2.2%	0.46	0.63	0.54	X 4.5
DICE (version 2)	3.8%	0.36	0.51	0.43	X 5.6
DICE (version 3)	2.2%	0.26	0.29	0.27	X 9
DICE (version 4)	3.6%	0.12	0.18	0.15	X 16
DICE (version 4bis)	**3.6%**	0.07	0.12	0.095	**X 26**

Synthesis of DICE results

- We stored enough data to extract an acceptable statistic for SEU
  - 640 cells per type of latch and we reached a spill number > 20000
- Cross section of the standard latch ~ $2.8E^{-14}$ cm²
- Dice latch is ~ 5 x immune to SEU than standard latch
- With interleaved layout, improvement of the SEU tolerance : 9 x more tolerant than the standard latch -> cross section = $3.1E^{-15}$ cm²
- By increasing the size of transistors (L x 7), we win a gain value significantly (~30) while keeping an area budget compatible with the pixel size (50x50um).

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TRL versions

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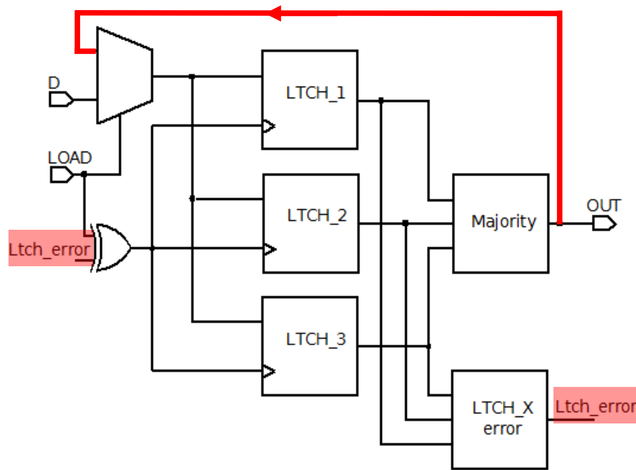
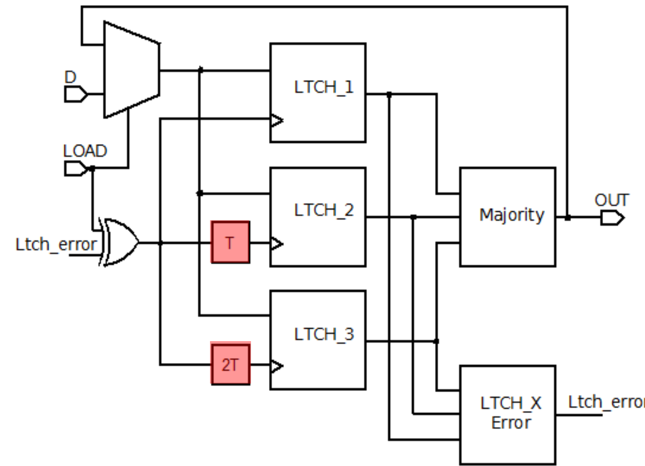
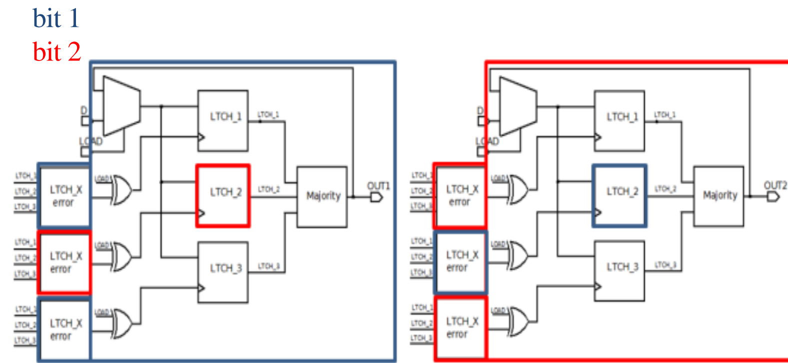


reference TRL version

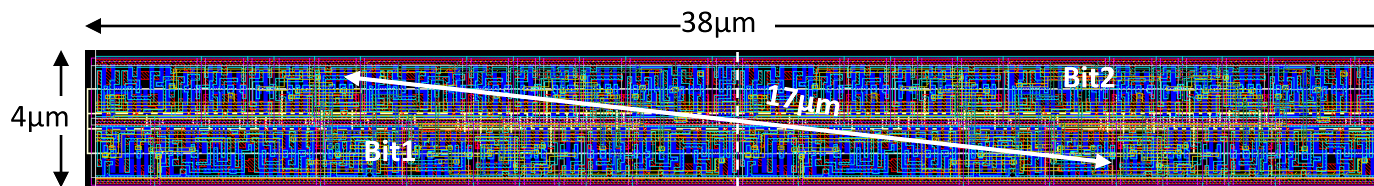


2nd TRL version



3rd TRL version

- 3 TRL versions have been designed and tested at CERN
  - Reference version with a feedback correction commanded by a latch error detection
  - 2nd version with an insertion of a delay cell (5ns ± 1ns) on the LOAD common node
  - 3rd version: triplication of the LOAD function with a special attention of the associated layout and a respect of a minimum distance between 2 bits (~17µm)



Layout of the 3rd TRL version (2 bits)

TRL latches results

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version 1	Reference TRL
version 2	TRL +3 X LOAD
version 3	TRL + 3 X LOAD interleaved

reminder of TRL version

Cell	Area ratio: $\frac{\text{memory (8 bits)}}{\text{pixel (50x50}\mu\text{m}^2)}$	Error rate/spill			Gain
		0 → 1	1 → 0	all	
Standard latch W_{pmin} = 300nm	2%	2.58	2.29	2.43	-
TRL (version 1)	18%	20E-3	1.8E-3	11E-3	X 220
TRL (version 2)	24%	4E-3	1.9E-4	2.1E-3	X 1160
TRL (version 3)	**24%**	1.2E-3	4.6E-5	6.2E-4	**X 3920**

Synthesis of TRL results

- Enough statistics for SEU (640 cells per flavor of cell and > 20 000 spills)
  - Cross section standard latch ~ $2.8E^{-14}$ cm²
- TRL latch is ~200 x immune to SEU than standard latch (same result as for the PROTO65_V1)
- Triplication of the “load path” improves the SEU tolerance by a factor 5 (~1000 x times immune than a standard latch)
  - Cross section ~ $2.3\ E^{-17}$ cm²
- With interleaved layout added the load signal triplication, SEU tolerance improved by a factor 18 regarding the reference TRL design (version 1). It represents an immunity 4E3 better than the standard latch
  - Cross section ~ $6.8\ E^{-18}$ cm²

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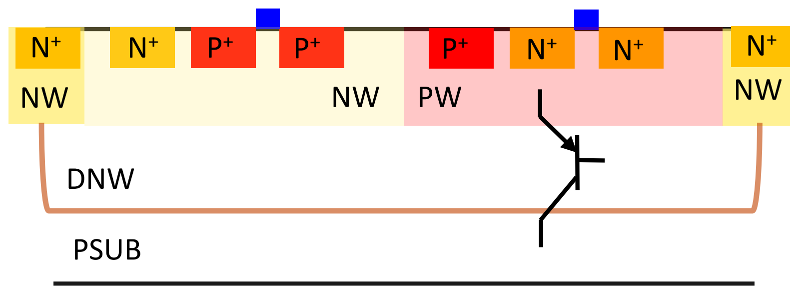
Influence of the DNW

- DNW is used to optimize an isolation between a sensitive part and the digital functions associated. This option is implemented in the RD53A chip.
- Some perturbations in term of SEU rate due to the presence of parasitic bipolar transistors.
- Direct comparison between 2 cells with and without DNW is possible with our last SEU prototype.

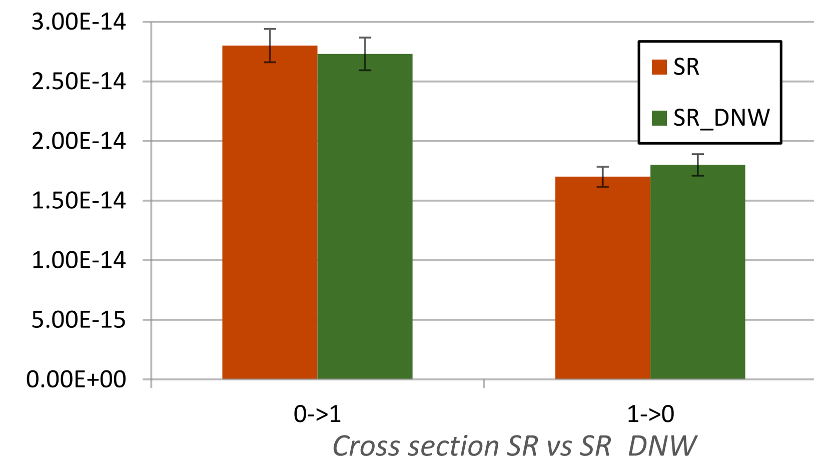
Layout of 2 cells with (left) and without (right) DNW

Cell	Error rate/spill	
	0 → 1	1 → 0
SR	2.34	1.94
SR_DNW	2.42	2
TRL	1.5E-2	2.05E-3
TRL_DNW	2.3E-2	1.1E-3

Synthesis error rate/spill



CMOS with a Deep N Well



Cross section SR vs SR_DNW

- No real difference measured between these 2 cells
- A DNW in this technology doesn't affect the SEU tolerance

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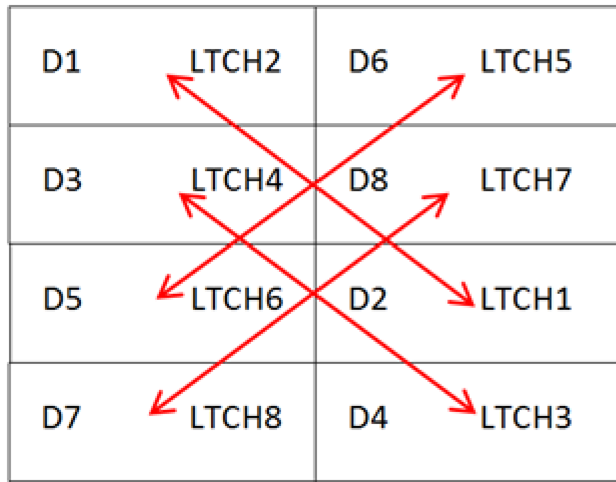
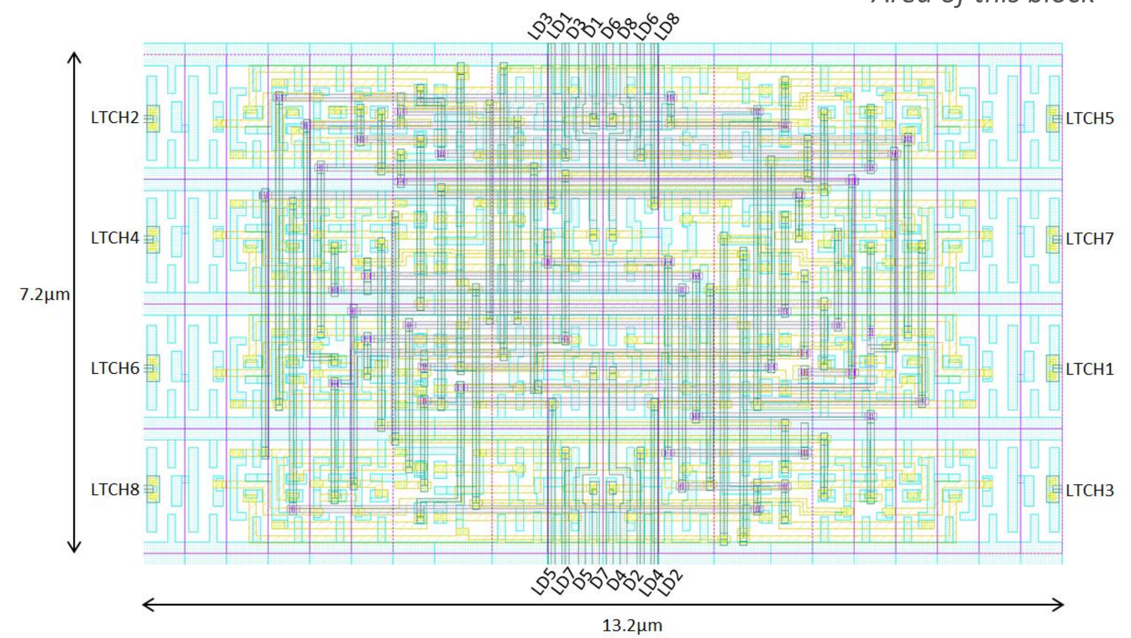
Proposal of SEU latches for RD53A

- A configuration memory pixel has been designed and implemented in few columns in the RD53A chip submitted at the end of august.
- It is equivalent to the DICE version 3 cell:
  - Interleaved version
  - Transistors size PMOS: 400nm/60nm, NMOS: 200nm/60nm
  - Distance between 2 DICE's (D_{2N}) ~10µm

S= 7.2x13.2=95µm²
(3.8%)
Area of this block



Synoptic of the block memory



Layout of the block memory

conclusion

- Several flavor of latches have been tested to evaluate their tolerance against the SEU effect
- Triple Redundancy Latches versus DICE retain our attention during this study
  - TRL:
    - ✓ very tolerant to the SEU (Cross section ~ 6.8 E^{-18} cm^2)
    - ✓ Compatible in a periphery of a full scale chip (global memory)
  - DICE:
    - ✓ Dedicated area compatible implementation in a pixel but sensitive to the charge sharing
    - ✓ Optimization of the size transistors is a good issue without affecting a lot the cost of area

	Mean time between 2 errors	
	Pixel config.	Global config.
Memory size	1.28Mbits/chip	1kbits/chip
Standard latch	55ms	71s
TRL (version 3)	209s	74 hours
DICE (version 4)	1.5s	2500s

Mean time errors estimation relative to cross section measured

- The hamming code version could be improve:
  - Only a factor 13 comparing with a standard latch
  - Parity bit architecture more tolerant, optimization of the area ratio logic/latches, …
- The implementation of a Deep Nwell to isolate the digital part doesn't show a degradation of the SEU cross section
  - The parasitic bipolar presents with the DNW layer doesn't affect the cross section of the memory
- RD53A side:
  - A pixel configuration 8 bits memory has been designed and implemented in the chip
  - A TRL architecture has been synthetized and implemented in the periphery

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THANKS FOR YOUR ATTENTION