FPGA as a Service in the Cloud

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Huawei FPGA Accelerated Cloud Server (FACS)

- Beta program launched in China, September 30
- Access available now
- Part of the HPC Cloud Scenario: Includes GPU & High Performance CPU instances

Existing Cloud Provider to Helix Nebula Science Cloud

Open Telekom Cloud FPGA instances coming 2018
FACS: Complete IaaS for FPGA Accelerated Computing

Hardware & Software Development Kit

Custom Logic

Huawei FPGA Image

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01110010011010010110
01000110011101100101

Huawei Cloud Marketplace

Publish

FP1 Instance (Hardware)

Provision

Develop

Deploy
Key Benefits to FPGA Cloud Computing

Balances Programmability and High Performance for Key Workloads
Utility Model that Disrupts traditional Price:Performance

<table>
<thead>
<tr>
<th>Performance Relative to CPU</th>
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<tbody>
<tr>
<td><strong>13x</strong></td>
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<tr>
<td>Machine Learning</td>
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<tr>
<td>Inference</td>
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<tr>
<td>CNN: Image</td>
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<tr>
<td>Xilinx Stack Benchmark</td>
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<tr>
<td><strong>43x</strong></td>
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<td>LSTM: Speech</td>
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<td>Data Analytics</td>
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<td>SQL Query</td>
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<td>Xilinx Stack Benchmark</td>
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<td><strong>29x</strong></td>
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<td>Networking vSwitch</td>
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<td>Xilinx Customer Deployment</td>
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<tr>
<td><strong>100x</strong></td>
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<tr>
<td>Genomics Sequencing</td>
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<td>Edico Genome</td>
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<tr>
<td><strong>90x</strong></td>
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<tr>
<td>Big Data Analytics</td>
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<td>Ryft</td>
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Cloud enables a new capability of utilizing FPGA technology as a utility, resulting in faster access to the newest technology with less cost.

Source: Xilinx Technical Marketing
Why Choose Huawei FACS IaaS?

Huawei is the global leader in the enablement of FPGA system solutions:

✓ Industry leading provider of FPGA accelerated system solutions for the Telecom and Enterprise
✓ The largest global employer of FPGA engineering resources
# Huawei FACS Specification

## Xilinx VU9P FPGA CARD

- Xilinx Ultrascale+ 16nm VU9P
- 2.58 Million System Logic, 6800 DSP
- PCIe3.0 x16
- 64GB DDR4 2133MHz SDRAM ECC
- 3*100G High-Speed Serial Links

<table>
<thead>
<tr>
<th>Name</th>
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<th>FPGA</th>
<th>Memory</th>
<th>NVMe</th>
<th>InterLink</th>
<th>Network</th>
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<td>116G</td>
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<td>300G Links/FPGA</td>
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</tr>
</tbody>
</table>

## Example Diagrams

**8xlarge**

- 300G Mesh

**16xlarge**

- 300G Interconnect
FACS Development Tools & Kits

High Bandwidth:
PCle x16
@12GB/s
Low latency:
<5us @ 512Byte

Language Support:
C, UVM, SystemVerilog-2012

Interface Support:
axi4/axi4-lite/axi4-stream BFM

30+ IP Reference Library:
AI, security, multi-media, etc.

20+ reference designs:
Network interface, RAM and inter-connects, FIFO

Static Region < 20%

Industry Standard Framework
DPDK APIs
OpenCL APIs
DPDK Runtime
OpenCL Runtime
SRIOV
OS

APP

HDK

Simulation Platform
Reference design and IP

Tool Kit

FPGA

SDK

HP Shell

Static Region – DPDK/OCL based Shell

Memory Controller

IP
(AI,H.265, ....)

Develop
FPGA Shell Options

**Huawei DPDK Based Shell**

- **PCIe**
- **HPI**
- **MgmtPF**
- **User VF**
- **HW icap**
- **PR iso**
- **flash_ctrl**
- **SEU**
- **XVC**

**DMA**

- **IP**
- **DDR0**
- **DDR1**
- **DDR2**
- **DDR3**

**Dynamic**

- **NIC**
- **ETH**

**Scenario**: High performance, stream computing

- User logic: HLS and RTL supported
- High performance IO bandwidth, low latency framework

**Shell feature**:

- Queue based ring buffer DMA optimized for transfer latency
- Poll mode multi-message notification
- Offload acceleration, inline acceleration (future)

**Xilinx SDAccel Based Shell**

- **PCIe**
- **MgmtPF**
- **User PF**
- **HW icap**
- **PR iso**
- **flash_ctrl**
- **SEU**
- **Clk_wiz**
- **AXI_BAR**
- **Feature ROM**

**Dynamic**

- **APM**
- **DDR0**
- **DDR1**
- **DDR2**
- **DDR3**

**Scenario**: Rapid development, block computing

- User logic: OpenCL C, HLS C and RTL supported
- Suited for quick evaluation/porting of existing customer code

**Shell feature**:

- Xilinx scatter-gather XDMA optimized for big block data transfer
- Serial message notification
- Offload acceleration
FACS FP1 Use Case Scenarios

Genomic Sequencing Acceleration

Falcon Computing Partner Solution:
- Genomic Accelerator-as-a-Service
- Accelerated GATK Best Practices Pipeline IPs (RTL & Merlin C generated)
- Huawei FP1 Instance
- Customer Genome App

CTAccel Computing Partner Solution:
- CTAccel designed CIP (Image Processing IP)
- Huawei FP1 Instance
- Xilinx SDAccel shell
- Cloud Media Storage App

Web Media Transcoding Acceleration
The Huawei FaaS Ecosystem

Partners & End Users

- Domain partners
- Solution providers
- Acceleration IP providers
- Design service providers
- End Users

HUAWEI CLOUD

- Server
- Accelerator
- Develop Kit
- 3rd Part Tool

GitHub

- Development tools
- HDK/SDK

Open Source
Education & training
University Program

Marketplace

- IP core
- AII
- Accelerator as a service
- Image

3rd Party Cloud Platform

- Server
- Accelerator

Private DC

- Accelerator
What About FPGAs for High Energy Physics?

**Workloads:**
- Data Acquisition (established)
  - Signal processing, filtering
- Simulation & Modelling
- CERN openlab 6th Phase Aligned Targets:
  - Machine Learning (Deep Learning)
  - Data Analytics

**Development & Productivity:**
- FPGA historically dominated by hardware design practice (RTL)
- Now, several high-level languages exist
  - Vivado HLS, OpenCL, Merlin-C, Reconfigure.io (GO based FPGA programming), etc.
- Improved high-level tools for software development productivity
  - C model simulations, integrated IDEs, frameworks and libraries, etc.
Ecosystem Examples:
FPGA Cloud Native Solutions
Xilinx Machine Learning Technology Stack

Source: Xilinx Developer Forum, Xilinx, Frankfurt, January 2018
Standard Application Stacks Leverage Ryft to Gain the Advantages of FPGA Technology with Zero Learning Curve

Ryft makes FPGAs easy-to-use by tightly coupling industry standard software interfaces/APIs with fast FPGA-accelerated primitives for: **Real-time performance:** Eliminate data preparation bottlenecks, **Low Latency Operations:** Swap Ryft Analytics Primitives in-and-out, **Purpose-built heterogeneous compute:** Ensure the right compute architecture—CPU and/or Xilinx FPGA

Source: Ryft Cloud Brochure, Ryft
Ryft Supercharges Analysis by 91X to Render Big Data Relevant Now

Benchmark comparison of Elasticsearch on Ryft Cloud with FPGA-acceleration vs. on CPU
Enable existing software teams to develop FPGA accelerated solutions.

**Reconfigure.io** provides a modern cloud-native devops environment that brings acceleration capability to the whole organisation.

- High level languages and tooling
- Visualisation
- Integration into SDLC
- Continuous Integration and Continuous Deployment
Thank You.