

International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2018)

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Book of Abstracts

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Opening

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opening materials

Pixel system performance / 1

Operational Experience and Performance with the ATLAS Pixel detector at the Large Hadron Collider

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The tracking performance of the ATLAS detector relies critically on its 4-layer Pixel Detector, that has undergone significant hardware and readout upgrades to meet the challenges imposed by the higher collision energy, pileup and luminosity that are being delivered by the Large Hadron Collider (LHC), with record breaking instantaneous luminosities of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ recently surpassed. The key status and performance metrics of the ATLAS Pixel Detector are summarised, and the operational experience and requirements to ensure optimum data quality and data taking efficiency will be described, with special emphasis to radiation damage experience

Pixel system performance / 79

The Belle II Pixel Detector - Status and Performance

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The Japanese Super flavor factory, SuperKEKB, is in its final commissioning phase and will start operating in 2019. This new e^+/e^- machine will deliver an instantaneous luminosity of $8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$, 40 times higher than the current world record. A new detector, Belle II, is needed to exploit the high event rate and provide high precision measurements of the B meson system while coping with increased backgrounds. It features a silicon pixel detector consisting of two layers of DEPFET active pixel sensors close to the interaction point for vertexing.

The DEPFET technology combines detection together with in-pixel amplification by integrating a field effect transistor into a fully depleted bulk for every pixel. This combines low power consumption in the active pixel area with low intrinsic noise, allowing Belle II pixel modules to be thinned to $75 \mu\text{m}$ without the need of additional cooling structures.

To commission the accelerator and ensure a safe radiation environment for the final vertex detector, a pre-experiment called BEAST was performed this year which featured a slice of the Belle II pixel detector mounted at its final position. In this talk the performance of Belle II pixel modules during

this commissioning phase will be presented and the current status of the final detector integration in Belle II will be discussed.

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The CMS phase-1 pixel detector - experience and lessons learned from 2 years of operation

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In 2017, CMS has installed a new pixel detector with 124M channels that features full 4-hit coverage in the tracking volume and is capable to withstand instantaneous luminosities of $2 \cdot 10^{34} \text{cm}^{-2} \text{s}^{-1}$ and beyond. By now the detector has been successfully operated for two years in p-p and heavy ion collisions. Besides many improvements of the DAQ system, the detector monitoring capabilities, and silicon property prediction, very valuable experience has been collected in running a detector with DCDC powering and CO₂ cooling, which are both new core technologies for most of the upcoming detector upgrades at LHC experiments. During the long shut down of LHC from 2019 to 2021 the CMS pixel detector will be extracted and the modules of the inner most layer that suffered the most from radiation damage will be replaced. At that occasion a better read out chip as well as a new token bit manager chip will be used for these modules that fixes problems observed during operation. This talk will give an overview of the different improvements that have been made and the challenges that have been faced in the last two years. A special focus will be put on the lessons learned in the light of the design of future detectors. Finally, the planned work on the CMS pixel detector during the LHC shutdown will be outlined.

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Development of the CMS Phase-1 Pixel Online Monitoring System and the Evolution of Pixel Leakage Current

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A new pixel online monitoring system has been developed to give a fast and intuitive view of the detector performance both offline and online. The source script was written modularly in Python programming language in association with the SQLite and Java languages. It establishes a connection with the CMS detector monitoring database, and extracts and stores detector information into a local database. Among all of the monitored detector parameters, the pixel leakage current is one of the most interesting, as it reflects the accumulated radiation damage of the silicon sensors. The leakage currents obtained from different module positions in the pixel detector are highly correlated with the distance from the beam pipe. Based on the new monitoring system, we have analyzed the pixel detector leakage current evolution since the recent Phase-I upgrade of the pixel detector and its dependence on the environmental temperature influenced by the cooling loop arrangement inside the pixel detector. The results provide a crucial reference on the detector performance for the re-design of the detector in the Phase-2 upgrade.

Pixel sensor monolithic / 87

Monolithic Deep Depletion CMOS Pixel Sensor for Detection of Minimum Ionizing Particles and X Rays

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High energy radiation like X rays and Minimum Ionizing Particles (MIPs) have a radiation length of several tens of microns in silicon. When using standard CMOS processes with low-resistivity silicon substrates or thin high-resistivity EPI layers, the achievable signal amplitude is too small to provide competitive performance for applications in particle tracking or low energy X-ray detection. For those applications a deep depletion silicon detector is necessary which cannot be built using standard CMOS processes.

We modified a standard 180nm CMOS process using high resistivity silicon substrate to create a thick depletion layer in which a strong drift field is created when a high voltage is applied to the backside. High charge collection efficiency is expected to be maintained up to neutron irradiation of to 1016 neq/cm² by increasing the depletion voltage on the backside, without constraints by the CMOS circuitry on the front side. We have demonstrated complete and accurate charge collection for detector thicknesses from 50 to 400 microns. In the past two years we have designed and fabricated the following devices that have applicability to X-ray and MIP detection in high energy physics:

- (1) 640 x 512, 15 μ m pitch, low-noise imaging sensor
- (2) 1K x 1K, 20 μ m pitch, digital-output OrthoPix sensor that detects and reports locations of MIP events at high brilliance (>100M hits/cm²/sec)
- (3) 36 x 36, 50 μ m pitch demonstration device for X-ray tracking

We present measurement results from the latest developments of our deep depletion sensors for these applications. In particular, we successfully demonstrated imaging with high MTF on our 640 x 512 sensor with 400 μ m thickness, which is the thickest fully depleted silicon sensor reported in the literature, to our knowledge. Our recently developed megapixel OrthoPix detector supporting a frame rate of 50 MHz at 200 mW/cm² power dissipation is suited for large-area particle trackers at low sensor cost.

Pixel sensor monolithic / 82

Development of fast, monolithic silicon pixel sensors in a SiGe Bi-CMOS process.

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An ultra-fast, low-noise and low-power SiGe Bi-CMOS electronics was developed and implemented in a monolithic silicon pixel sensors, with the aim to achieve 100ps time resolution for minimum ionising particles with 500x500 micron² pixels, corresponding to ~750fF capacity. The performance of a prototype chip, comprising a 3x10 pixel matrix and a 50ps binning TDC will be shown, together with the technique proposed to synchronise a large number of sensors at picosecond level.

Pixel sensor monolithic / 54

Electrical characterization of AMS aH18 HV-CMOS after neutrons and protons irradiations

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In view of applications in the tracking detectors of the ATLAS High Luminosity LHC (HL-LHC) upgrade, we have developed a new generation of High Voltage CMOS (HV-CMOS) monolithic pixel-sensor prototypes featuring the AMS aH18 (180 nm) commercial CMOS technology. By fully integrating both analog and digital readout-circuitry on the same particle-detecting substrate, current challenges of hybrid sensor technologies: larger readout input-capacitance, lower production-yield, and higher production and integration cost can be downscaled. The large fill factor design using high resistivity substrates strongly helps to mitigate the charge-trapping effects, making these chips radiation hard. The surface and bulk damage induced at the highly irradiative environment change the effective doping concentration of the device that modulates the high electric fields as the substrate-bias voltage is increased can cause an increased leakage current and premature electrical breakdown due to impact ionization. In order to assess the characteristics of heavily irradiated samples, using ATLASPix1 HV-CMOS chip as test vehicles, we have carried out a dedicated campaign that included irradiations of neutrons and protons, made at different facilities. Here, we report on the electrical characterization of the irradiated samples at different ambient conditions, also in comparison to their pre-irradiation properties. Results demonstrate that hadron irradiated devices can be safely operated at a voltage high enough to allow for high efficiency, up to the fluence of 2×10^{15} neq/cm², beyond the radiation levels (TID and NIEL) expected in the outer barrel region of Inner Tracker (ITk).

Pixel sensor monolithic / 53

Simulations of CMOS sensors with a small collection electrode improved for a faster charge-collection and increased radiation tolerance

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CMOS sensors with a small collection electrode are attractive for a wide range of applications due to the very low sensor capacitance allowing for a very low noise and analogue power consumption. Such sensors have been studied and developed for the ALICE ITS upgrade, where they have been

selected as the technology of choice. To achieve a full lateral depletion in the sensor, a process modification has been performed, making this technology also attractive for detectors in harsh radiation environments, such as for the ATLAS ITk upgrade, and for detectors with time resolution requirements in the order of a few nanoseconds, such as the CLIC tracking system. However, the electric field in the sensor reaches a minimum in the pixel corners, more pronounced for larger pixel sizes, increasing the charge-collection time. This can result in a degraded timing resolution and loss of efficiency after irradiation. Recent studies of this technology have shown the challenge to achieve a fully efficient operation after irradiation and a timing resolution in the order of a few nanoseconds precision for pixel sizes of larger than approximately 40 micrometres. This paper presents three-dimensional self-consistent Technology Computer Aided Design Simulations for two concepts to improve the timing resolution and radiation hardness for a given pixel size: a mask change and an additional implant. The transient simulation has been performed for several variations of the proposed designs and of the operation conditions for non-irradiated and irradiated sensors. The simulation results indicate a significant improvement of the charge-collection time before and after irradiation and of the collected charge after irradiation. The new designs are now implemented in a next submission of the ATLAS prototype chips in this technology.

Pixel system upgrade / 47

The LHCb VELO Upgrade

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The LHCb experiment at the LHC is designed to capture decays of b- and c-hadrons for the study of CP violation and rare decays. It has already had a transformative impact in the field of flavour physics as well as making many general purpose physics measurements in the forward region. At the end of Run-II, many of the LHCb measurements will remain statistically dominated. For this reason the experiment is being upgraded to run at higher luminosity after 2020. The trigger scheme, which currently has a 1 MHz lowest level hardware rate, will be transformed to a strategy whereby the entire experiment is read out at 40 MHz to a flexible software trigger. The increased luminosity and trigger efficiency anticipated at the upgrade will allow significant improvements in measurements across the flavour sector and beyond. In order to allow the triggerless readout the front end electronics of all subdetectors will be changed, and many subdetectors will be upgraded to cope with the increased occupancy and radiation levels anticipated at the upgrade.

The Vertex Locator (VELO) surrounding the interaction region, whose role is to reconstruct and trigger on the primary and secondary vertices of the events, is an example of a subdetector which will be completely changed. The current strip detector will be replaced by a hybrid pixel detector read out with the VeloPix ASIC. The detector operates just 5 mm away from the collision region, and will give optimum track reconstruction efficiency and projected precision at the vertex region.

The upgraded VELO is composed of 52 modules placed along the beam axis. The 26 modules in each half can be retracted during LHC filling and only close to the nominal position after stable beams have been declared. Each module is equipped with 4 silicon hybrid pixel tiles, each read out with by 3 VeloPix ASICs. The pixels have a pitch of $55 \mu\text{m} \times 55 \mu\text{m}$ and the sensors are produced in $200 \mu\text{m}$ thick p-in-n type silicon. The sensors must withstand an integrated fluence of up to $8 \times 10^{15} 1\text{-MeV } n_{eq}/\text{cm}^2$, a roughly equivalent dose of 400 MRad, and it is anticipated that the bias voltage must be raised to 1000V by the end of lifetime of the detector. The highest occupancy ASICs will have pixel hit rates of 800 Mhits/s and produce an output data rate of over 15 Gbits/s, with a total rate of 1.6 Tbits/s anticipated for the whole detector.

The VELO upgrade modules are composed of the detector assemblies and electronics hybrid circuits mounted onto a cooling substrate, which is composed of thin silicon plates with embedded micro-channels that allow the circulation of liquid CO₂. This technique was selected due to the excellent

thermal efficiency, the absence of thermal expansion mismatch with silicon ASIC's and sensors, radiation hardness of CO₂, and very low and uniform contribution to the material budget. The front-end hybrids host the VeloPix ASICs and a GBTx ASIC for control and communication. The signals are routed to the electronics mounted outside the vacuum tank via 56~cm copper data tapes running at 5 Gb/s and custom vacuum feedthrough boards.

The secondary vacuum in which the modules are located is separated from the beam vacuum by a thin custom made foil. This foil is manufactured through a novel milling process and possibly thinned further by chemical etching.

The upgraded VELO is currently under construction and module pre-production is underway. The performance of the ASICs, bump bonded sensors and double sided electrical module will be described, along with the first results from the prototype modules in terms of electrical, mechanical and thermal performance, along with the status of the mechanical construction and preparation for assembly.

Poster section / 9

Design and Test of ASIC driver and readout for scientific CCD detectors

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In order to implement the driver and readout functions for several types of scientific CCD detector, decreasing the size of electronics of CCD detector system and reducing the total power dissipation for a large scale mosaic CCD detector system, ASIC driver and readout chip was designed using Global Foundry 180nm BCDlite technology. The CCD driver which is called BCDA (Bias Clock Driver ASIC) provide multi-channel clocks and Bias voltage. The CCD video sampling is called CVRA (CCD Video Readout ASIC). The main referenced CCD detectors are detectors from E2V company. A testing system was developed for ASIC test. In addition to the driver module and the readout and sampling module, the testing board includes a FPGA module to control the ASIC, a USB 2.0 interface to communicate with a host computer and a voltage monitoring module. The CCD controller based on ASICs is tested by a scientific CCD simulation and test system which is used to simulate CCD47-20 and generate the required CCD waveform. Additional power board is used to provide complex power supplies. We have carried out functional test and performance test for driving circuit and readout circuit respectively. The waveform shape of the CLOCKS, including the rise time, the fall time and the switching speed, can fit the readout speed of CCD47-20. The readout circuits have low noise. The ASIC testing system was combined with the software on host computer and the scientific CCD simulation and test system to take a picture of 1500*1032 pixels whose brightness decreases with equal difference from the left to the right.

Pixel system upgrade / 17

The Upgrade of the CMS Inner Tracker for HL-LHC

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The entire CMS silicon Tracker will be replaced at HL-LHC with a new detector featuring increased radiation hardness, and capability to handle higher data rate and longer trigger latency. The Inner

Tracker will be exposed to the most extreme conditions, requiring advanced technologies and novel solutions notably for the readout and powering electronics. The new detector will also feature extended rapidity coverage. The high-luminosity upgrade of the CMS silicon pixel detector will be presented, discussing on the novel features of the detector layout and electronics system, and the expected performance in high pileup conditions.

Poster section / 12

A TOSA/ROSA-Based Optical Transmitter (MTx+)/Transceiver (MTRx+) for High-Energy Physics Experiments

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We present a dual-channel optical transmitter (MTx+) and an optical transceiver (MTRx+) for front-end readout electronics. MTx+ utilizes two Transmitter Optical Sub-Assemblies (TOSAs) (Truelight Part No. TTF-1F59-427) and MTRx+ uses a TOSA and a Receiver Optical Sub-Assemblies (ROSA) obtained from CERN. Both MTx+ and MTRx+ receive multimode fibers with standard Lucent Connectors (LCs) as the optical interface and can be panel or board mounted to the motherboard with a standard Enhanced Small Form-factor Pluggable (SFP+) connector as the electrical interface. MTx+ and MTRx+ employ a dual-channel Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC called LOClD65. LOClD65 is designed in a commercial 65-nm CMOS technology with a power supply of 1.2 V. Each channel of LOClD65 can be individually turned on or off. LOClD65 features input and output equalizers. LOClD65 is packaged in a 24-pin 4 mm x 4 mm open-cavity Quad-Flat No-leads (QFN) package. MTRx+ has a GBTA embedded in the ROSA. We design an optical latch to hold two LC connectors and two TOSAs/ROSA together and a metal cage to attach the module to the motherboard. We printed prototype latches with a 3-Dimension printer and are producing latches in injection molding. The prototype cage has been fabricated. The dimension of MTx+/MTRx+ is 44.5 mm (length) x 18.2 mm (width) x 5.8 mm (height). Each transmitter channel of MTRx+/MTRx+ is tested to operate up to 14 Gbps with typical power dissipations (the VCSEL included) of 68.3 mW/channel and 62.1 mW/channel at the VCSEL voltages of 3.3 V and 2.5 V, respectively. MTx+ and MTRx+ survive 4.9 kGy(SiO₂). MTx+ and MTRx+ with an evaluation board can be obtained for further development.

Poster section / 14

The read-out ASIC of Gotthard-II Detector

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The European X-ray Free-Electron Laser (XFEL.EU) is operating with bunch trains at a repetition rate of 10 Hz since October 2017. Each train consists of 2700 photon bunches with a temporal separation of 220 ns corresponding to a frame rate of 4.5 MHz. Each photon pulse has a duration less than 100 fs (rms) and contains up to 1012 photons in an energy range between 250 eV and 25 keV. This machine will not only open the way to new scientific opportunities but also sets extreme challenges for the detectors, such as AGIPD, DSSC and LPD.

Gotthard-II is a microstrip detector developed for XFEL.EU. The applications include but are not limited to: energy dispersive experiments at 4.5 MHz frame rate, and veto signal generation. In Gotthard-II a silicon microstrip sensor with a pitch of 50 μm or 25 μm is wire-bonded to the read-out ASICs. Each read-out channel on the ASIC consists of an adaptive gain charge sensitive Pre-Amplifier (PA), followed by Correlated-Double-Sampling (CDS) amplifier, 12-bit 18 MSPS Analog-to-Digital Converter (ADC) and Static Random-Access Memory (SRAM) for storing all 2700 images in an XFEL bunch train.

The charge generated in the sensor is collected and converted into voltage signal by the PA. The CDS amplifier removes the reset noise and converted the single-ended input signal into the fully differential output signal. The analog output signal of the CDS amplifier is digitized by the ADC. Every 4 channels share 1 CDS amplifier and 1 ADC. The digital outputs of the ADC are stored in the SRAM, and will be read out during the breaks of the bunch trains. The final ASIC will have 16 blocks. Each block includes 8 PAs arranged with a pitch of 50 μm , 2 CDS amplifiers, 2 ADCs and 1 SRAM of 112 x 2720 bits.

The implemented ADCs are a type of asynchronous successive approximation register (SAR) ADC. It consists of 2 differential split-capacitor arrays serving as digital-to-analog converter (DAC), a comparator and a control logic circuit. Two DACs alternatively works on sampling the input signal and digitizing the sampled signal during each conversion cycle. The comparator is implemented with a differential amplifier followed by a dynamic latch. The comparator outputs generates the asynchronous clock called READY signal to trigger the following steps during the conversion in order to avoid using a power-hungry high frequency clock. Due to the mismatch of the capacitors in the DAC, the raw outputs of the ADC include missing codes and wide codes, and need to be calibrated. Several prototype designs of the analogue front-end (PA + CDS) and the ADC have been fabricated in UMC 110nm CMOS technology. The last prototype, which was submitted in November 2017, consists of a full signal chain: 8 front-end channels + 2 ADCs + 1 SRAM and was received in April 2018. The measurement results show that the equivalent number of bit (ENOB) of the ADC is bigger than 10 with a power consumption less than 1 mW at a sampling frequency of 18 MHz. The measured full dynamic range covers 1 – 104 12 keV photons. The noise is lower than 1.6 keV. The measured DNL of the ADC is less than ± 0.5 LSB and the INL of the ADC is less than ± 0.4 LSB after calibrating the 12-bit raw ADC outputs to 10-bit data. The final full scale chip including 128 front-end channels, 32 ADCs and the SRAM to store 2700 images is foreseen to be submitted in November 2018.

Pixel system upgrade / 22

Upgrade of the ALICE Inner Tracking System

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The Inner Tracking System (ITS) of the ALICE experiment will be upgraded during the second long LHC shutdown in 2019-2020. The main goal of the ALICE ITS Upgrade is to enable high precision measurements of low - momentum particles ($< 1\text{GeV}/c$) by acquiring a large sample of events, benefiting from the increase of the LHC instantaneous luminosity of Pb – Pb collisions to $\mathcal{L} = 6 \cdot 10^{27} \text{cm}^{-2} \text{s}^{-1}$ during Run 3. Working in this direction the ITS upgrade project is focusing on the increase of the readout rate, on the improvement of the impact parameter resolution, as well as on

the improvement of the tracking efficiency and the position resolution. The major setup modification is the substitution of the current ITS with seven layers of silicon pixel detectors. The ALPIDE chip, a CMOS Monolithic Active Pixel (MAP) Sensor, was developed for this purpose and offers a spatial resolution of $5\mu\text{m}$. The use of MAP sensors together with a stringent mechanical design allows for the reduction of the material budget down to $0.3\% X_0$ for the innermost layers and $1\% X_0$ for the outer layers.

During the research and development period a variety of tests were performed on all components for the validation of the detector design. A series of ageing tests were done to validate the assembly procedure and to ensure the proper performance of modules and staves after several years of operation in ALICE. The production phase has started with all the new assembled components undergoing different tests that aim to characterise the modules and staves and determine their qualification level. Measurements with a radioactive source were also done and are indicative of the response of the ALPIDE chips even after being assembled in a larger scale structure. This contribution will focus on the detector design, on the measurements performed during the research and development phase, as well as on the production status and the first results from quality assurance.

Poster section / 21

Module Development for the Phase-2 ATLAS ITk Pixel Upgrade

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For the high luminosity upgrade of the Large Hadron Collider (HL-LHC), the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch crossing. To cope with the resultant increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of ITk will consist of a state-of-the-art pixel detector, with an active area of about 14 m^2 , which will provide tracking capability up to $|\eta|=4$.

Detector requirements in terms of radiation hardness and occupancy, as well as thermal performance depend strongly on the distance from the interaction region. Therefore, the innermost layer will feature 3D silicon sensors, due to their inherent radiation hardness and low power consumption, while the remaining layers will employ planar silicon sensors with thickness ranging from $100\mu\text{m}$ to $150\mu\text{m}$. All hybrid detector modules will be read out by novel ASICs, implemented in 65nm CMOS technology and thinned to $150\mu\text{m}$, which will be connected to the silicon sensors using bump bonding.

With the recent arrival of the first readout chip prototype, the RD53A chip, prototype modules are being built to study sensor and chip properties, thermal performance, as well as bump bonding yield in lab measurements and beam test campaigns. Irradiation studies are ongoing.

The talk will present latest results from the module characterization measurements both before and after irradiation.

Poster section / 25

A 5.12 Gbps serial data receiver for active cable for ATLAS Inner Tracker Pixel Detector readout upgrade

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In the ATLAS inner tracker pixel Detector (ITK) upgrade for HI-LHC, the up stream data from the detector has to go through a 5-meter thin cable before it is received by an optical module for optical link to control room. The cable mass is expected to be minimized, which limits the bandwidth of the cable that is much less than the data rate. Due to the high-frequency loss of the cable, the electric signal is serious degenerated. The significant Inter Symbol Interference (ISI) jitter causes a fully closed eye of the signal which make it is not qualified for optical module input specification. We present a design of a serial data receiver to equalize the signal and retime the data with a recovered clock. The output jitter of the receiver expected to below 10 ps when the cable is an American wire gauge (AWG) 34 Twinax cable. The chip has four channel of receivers and each channel consumes power of 75 mA current.

The diagram of one channel receiver is shown in Figure 1. The equalizer is based on a two-stage continuous time linear (CTLE) structure. After the equalizer, the ISI jitter is significantly reduced. The following clock and data recovery (CDR) module recovers the clock signal and retimes the data. The CDR module is modified based on the original design in lpGBT. The ISI jitter of the retimed data signal is minimized. A Current Mode Logic driver is used to drives the retimed data for optical module. Users also can bypass the CDR module to for the test purpose.

This chip is expected to be submitted in November 2018. The post-layout simulation of the design will be presented on the meeting.

Poster section / 27

A Readout Network for High-Density Electrode Array Targeting Neutrinoless Double-Beta Decay Search in TPC

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Among the current and planned experiments of neutrinoless double-beta decay ($0\nu\beta\beta$), the high-pressure gaseous Time Projection Chamber (TPC) stands out for its excellent energy resolution, very low radioactive background level and good scalability. Moreover, high position resolution can be maintained with an appropriate charge readout scheme for gaseous TPC to further suppress the background through ionization imaging. A pixelated charge readout plane without gas-electron avalanche is desirable. Based on a 0.35um CMOS process, a low noise sensor, Topmetal-S, is being developed which, even without gas gain, the energy resolution requirement could be met. Since $0\nu\beta\beta$ tracks are extended to tens of cm in length in high-pressure gas, Topmetal-S is designed to have mm-sized charge collection electrode, followed by a charge sensitive amplifier and an ADC in the first prototype. To realize a ton-scale high-pressure gaseous TPC, approximately 1×10^5 Topmetal-S sensors need to be laid on a meter-sized plane. The greatest challenge is a reliable high-density channels readout.

This paper proposed a distributed, self-organizing and fault-tolerance readout network. As a node of the network, each Topmetal-S integrates a router. The scheme establishes local connection between nearby sensors to form a sensor network. Each sensor not only generates and transmits their own data, but also forwards data from nearby sensors, and data packet is finally received by a computer that is connected at the edge of the network. In order to simplify the complexity of router, 2D-Mesh is chosen as the topology of the network. A distributed routing algorithm, extended-XY, is implemented. The routing algorithm is also fault-tolerant. Failed sensors will not disable a large

section of the network. Faulty node detection is implemented by sending test packets by the computer. After fault detection, through configuration the computer will form a set of rectangular region called faulty blocks to contain detected faults. The extended X-Y routing follows the regular X-Y routing until the packet reaches a boundary node of a faulty block. At that point, the packet is routed around the block clockwise to pass through. The design of the router is complete. The whole network performance is being simulated. The details of the routing algorithm, the fault detection scheme, the micro-architecture of the router, the throughput, and latency of the network will be presented.

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ATLAS ITk Pixel Detector Overview

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For the high luminosity era of the Large Hadron Collider (HL-LHC) it is foreseen to replace the current Inner Detector of the ATLAS experiment with a new, all-silicon detector to cope with the increase in occupancy, bandwidth and radiation damage that result from the increase of the instantaneous luminosity by a factor of 5 to 7.5. The new Inner Tracker (ITk) will consist of an inner pixel and outer strip detector aiming to provide tracking coverage up to $|\eta|=4$. The layout of the pixel detector is foreseen to have five layers of pixel silicon sensor modules in the central region and several ring-shaped layers in the forward region. This results in up to 14 m² of silicon depending on the selected layout.

While the outer 3 layers of the Pixel Detector are designed to operate for the full HL-LHC data taking period, the innermost 2 layers of the detector will be replaced around half of the lifetime. The innermost layer of the ITk Pixel Detector will feature 3D silicon sensors, due to their inherent radiation hardness and low power consumption, while the remaining layers will employ planar silicon sensors with thickness ranging from 100 μ m to 150 μ m. All hybrid detector modules will be read out by novel ASICs, implemented in 65nm CMOS technology, which will be connected to the silicon sensors using bump bonding. With about $4 \cdot 10^4$ pixels per cm² the bump bond density is a much higher than in previous hybrid detectors.

In order to reduce the amount of services needed, a serial powering scheme for the detector modules will be adopted. The pixel off-detector readout electronics will be implemented in the framework of the general ATLAS trigger and DAQ system with a readout speed of up to 5 Gb/s per data link for the innermost layers.

The talk will give an overview of the layout and current status of the development of the ITk Pixel Detector.

Poster section / 29

A Time-to-Digital Converter Based on DLL with High Accuracy Measurement Using 130nm Technology

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Time measurement is the basic measurement requirement in high-energy physics experiment and also one of the two basic measurements in nuclear electronics which are time measurement and energy measurement. Time measurement in nuclear physics and particle physics experiments is mainly for high-precision measurement of short time intervals, and time-to-digital converters are the central components of time measurement. Nowadays, TDC is not only used in high-energy physics experiments, but also widely used in aerospace and medical fields. TDC is an indispensable technology in navigation, space technology, communications, industrial production and electric power. We use a 130nm technology to implement a DLL-based TDC with a measurement resolution of 12.5 ps. The whole TDC consists of three levels with different measurement resolutions: a coarse counter with 800 ps resolution, a fine TDC with 100 ps resolution and an ultrafine Vernier-type TDC with 12.5 ps resolution. The whole design uses the DLL-based delay line and Vernier method to get the high measurement accuracy with the least influence of variety of process, temperature, and voltage. This TDC is a time-stamp style.

The TDC design has been fully simulated under different corners. The simulated results show that the delays of delay line are stable with a jitter less than 3 ps. The output codes of three level are all correct. The die is about 1 mm * 2 mm has been taped out for fabrication.

A testing board has been designed including FPGA, power module, high-speed transmission module. When the test system starts working, the power-on sequence of the FPGA is controlled by STM32. Then the clock generator LTC6951 is configured through the FPGA to generate a clock signal and a trigger signal. In order to test different time intervals, the frequency of the trigger signal is adjustable. After receiving the clock signal and HIT signal, the TDC will quantize the time interval of the adjacent HIT pulses and then output the quantized digital signal to the FPGA. The output signal of TDC is divided into two types. One is high-speed differential signals, such as Vernier-TDC-codes, Fine-TDC-codes, low-order Coarse-TDC-codes and output enable signals. The other type is low-speed signals, such as TDC test signals, high-order Coarse-TDC-codes, and so on. The high speed differential signal is a CML level standard that can connect to the FPGA's SerDes after AC coupled. The low-speed signal level standard is LVCMOS1.2, so it needs to be converted to LVCMOS1.8 level standard by SN74AXC and then transmitted to the FPGA. When the test system is working, the FPGA will receive a 23-bit code from the TDC, including 16-bit Coarse-TDC-code, 3-bit Fine-TDC-code, and 4-bit Vernier-TDC-code. Then the FPGA will calculate the time interval between the adjacent HIT pulses. Finally, the FPGA transmits the calculated data to the host computer. And we can calculate the accuracy of TDC by uploading data.

Poster section / 30

A 14-Gbps/ch VCSEL Array Driving ASIC in 65 nm CMOS for High-Energy Physics Experiments

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850nm VCSEL array light source combined with multi-mode fibers has been prevalingly employed in the commercial short-range data transmission scenarios with the advantages of relatively easy driven, low cost, high density and reasonably high bandwidth. Besides, the natural radiation-tolerant feature of the GaAs-based VCSEL also makes this combination very competitive in the high-energy physics readout applications. As a continuous study on the radiation-tolerant custom array optical module development and VCSEL driver design, here we report the design and test results of a 4 x 14 Gbps/ch VCSEL array driver ASIC implemented in 65nm CMOS technology. Each channel of the

driver receives 200 mVp-p differential CML signals, and outputs a 2 mA bias current and a 5 mA modulation current at 14 Gbps/ch with the power consumption of 52 mW/ch.

The driver die features a size of 2000 $\mu\text{m} \times 1230 \mu\text{m}$, and the channel height is 250 μm to be compatible with the VCSEL array die. The analog core of each channel consists of a limiting amplifier (LA) and a novel output driving structure. The LA is composed of an equalizer stage and a four-stage pre-driver. The output driver adopts the on-chip AC-coupling and a stacked tail-current source to remove the traditional cascode voltage-drop NMOS to improve the bandwidth. The bandwidth bottleneck of the output driving stage is effectively resolved for the 14-Gbps application without using any complex peaking or pre-emphasis structures.

This driving ASIC has been taped out and fully evaluated after wire-bonded to the four channel VCSEL array and integrated into an array optical transmitter. Widely-open 14 Gbps optical eyes have been captured, and full channel optical test results will be reported in the meeting.

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Study of Charge Collection Diode in a Monolithic Active Pixel Sensor for beam monitoring in heavy ion beam therapy facility

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Heavy ion beam therapy is becoming an ideal treatment for cancer. China is building a heavy ion beam therapy facility in Lanzhou. Beam monitoring system in the therapy facility ensures the beam energy deposition can accurately cover the dedicated tumor region. On the purpose of building a high-precision beam monitoring system, we are developing a Monolithic Active Pixel Sensor (MAPS) in a 180 nm CMOS Imaging Sensor process with deep p-well. This process has been chosen mainly because it allows the integration of the full CMOS circuitry within the pixel array without reducing the full charge collection efficiency. The charge collection diode is the critical part in this MAPS. The charge collection diode is formed by an n-well - p^- epitaxial layer junction. The p^- epitaxial layer is a high resistivity ($>1\text{k}\Omega\cdot\text{cm}$) layer with thicknesses (18 μm), significantly widening the depletion region. To reduce diode capacitance, the n-well structure is designed with an octagon shape instead of a square shape. And the p-well can be biased to a negative voltage, significantly increasing the depletion region. Meanwhile, considering about improving charge collection efficiency and reducing charge collection time, the diameter and spacing of diode, the location and depth of the heavy ion hit and the deep p-well area has been studied to optimize the structure.

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Developments towards a Serial Powering scheme in a monolithic CMOS technology for the ATLAS pixel upgrade

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CMOS monolithic pixel detector technology is one of the options considered for the outer layer of an upgraded ATLAS pixel detector in 2026. A Serial Powering scheme is foreseen for the new inner tracking detector for the Phase-II upgrade of the ATLAS experiment. The modules will be placed in series and powered on by a constant current source to reduce material budget and power losses. At the module level, shunt regulators are used to generate local supply voltage of 1.8 V to polarize the electronics from the input current. In contrast to hybrid pixels, the bias for monolithic sensors is sometimes limited and not sufficiently large to allow a common bias for all sensors in the serial powering chain. In order to meet the requirements of the ATLAS ITk outer pixel layers, new developments have been made in Shunt-LDO regulator and sensor biasing which are designed in modified TowerJazz 0.18 μm CMOS imaging technology. The Shunt-LDO regulator is capable of generating constant voltage of 1.8 V with a minimum drop out voltage of 200 mV and a maximum input current of 1.4 A. Moreover, a charge pump circuit was designed to provide the sensor bias. Two prototype variants were designed with 6-stages and 19-stages to provide negative bias down to -6 V and -20 V, respectively. Shunt-LDO regulator and charge pump test chips were submitted this summer. In this poster, a description of Serial Powering with CMOS sensor specificities will be shown.

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A 110nm CMOS process for fully-depleted pixel sensors

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Fully depleted pixel sensors with a thickness ranging from the 10s to the 100s of micrometers find many applications in X-ray, particle and near infrared imaging. Unlike the mature technologies used to fabricate visible-light image sensors, that rely on a few micrometers of active silicon, the fabrication of fully-depleted image sensors on thick silicon substrates still poses several technological challenges. Deep-submicron CMOS processes need to be made compliant with the high-resistivity substrates used as active sensing layers, and a high bias voltage needs to be applied to obtain a full depletion of the sensor. In most applications, a low-capacitance sensing node is also desirable for low-noise charge readout and a low-voltage digital electronics should be implemented on-chip to ensure low-power digital functions.

In this talk, a 110nm CMOS process on high-resistivity substrate tailored for the realization of fully-depleted pixel sensors is presented. Double-sided processing is used to define the backside electrode and the termination structures needed to bias the sensors at high voltage. A set of dedicated test structures for the assessment of the process was designed together with a 24×24 pixels array with $50 \mu\text{m}$ pitch.

A first run showing the feasibility of $300 \mu\text{m}$ -thick fully-depleted sensors was completed. The main technological challenges and the customization of the process will be discussed. TCAD simulation results and electrical measurements on dedicated test structures will be presented together with a characterization of the pixel sensor prototype.

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Development of 3D Trenched-Electrode Pixel Sensors with improved Timing performance

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The high luminosities expected at collider experiments over the coming years will put stringent requirements on the vertex detectors used in these experiments. The increased pile up will require improved spatial and timing resolution to distinguish between particle tracks while also requiring the devices to have an increased radiation hardness. 3D sensors have already been proven as a viable technology with good radiation hardness due to the short distance between electrodes and are also capable of achieving the desired spatial resolution. 3D sensors have so far not been fully exploited to achieve good timing resolution due to the non-uniformity of the electric field in the sensors.

The TIMESPOT project aims to develop a complete integrated system for tracking with high precision in both space and time. Novel 3D sensors are being developed for this purpose, providing the normal advantages of this technology (such as radiation hardness and low depletion voltage), with the trench geometry also providing more uniform electric and weighting fields, optimized for timing.

This presentation will describe the recent progress that has been made towards the development of these sensors. TCAD simulations have been carried out to optimize the design of these sensors and to estimate their performance, finding a compromise between the capacitance and the intrinsic speed. Technological tests have also been carried out at FBK to determine the manufacturing constraints of these sensors. A first layout including pixel sensors compatible with the TIMEPIX read-out chip and several test structures has been submitted to FBK and is currently being fabricated.

Poster section / 51

Development of the pixel detector for the ΔE -E telescope system at the HIRFL-CSR

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The ΔE -E telescope system at the HIRFL-CSR External Target Facility is proposed to study the reaction mechanism and unique structure of weakly bound nuclear in elastic scattering and burst reaction experiment. The silicon pixel detector is one of the major sub-detectors in this telescope system. In order to fulfill the requirements of spatial resolution, energy resolution, linear range and response time, the 10mm x 10mm square silicon has been chosen as the pixels. Each detector pad is packaged with 10x10 square silicon pixels with the process of planar technology on microelectronics manufacture line. Together with the detector pads, a dedicated electronics system has

also been designed to realize the readout functionalities. In this paper, the design, manufacture and first performance results of the silicon pixel detector will be discussed. The reverse leakage currents of each pixels are measured to less than 60 nA at full depleted voltage and the energy resolution of each pixels is calculated to be 1.1%.

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Microchannel CO₂ cooling for the LHCb VELO Upgrade

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The LHCb Vertex Detector (VELO) will be upgraded for the run III (scheduled to start in 2021) to a lightweight, pixel detector capable of 40 MHz readout and operation in very close proximity to the LHC beams. The thermal management of the system will be provided by evaporative CO₂ circulating in micro-channels embedded within thin silicon plates. This technique was selected due to the excellent thermal efficiency, the absence of thermal expansion mismatch with silicon ASICs and sensors, radiation hardness of CO₂, and very low contribution to the material budget.

The upgraded VELO modules will each host 4 silicon hybrid pixel tiles, each readout by 3 VeloPix ASICs with a total power consumption of up to 30 W. The implementation of a efficient and radiation hard cooling system is mandatory in order to remove the heat produced by the ASICs and keep the sensors below -20°C, which mitigates the radiation damage. The solution created is to use a cooling substrate composed of thin silicon plates with embedded micro-channels that allow the circulation of boiling CO₂. The direct advantages of this technique include the low and uniform material contribution, matching thermal expansion coefficients between the sensor-ASIC tiles and cooling substrate, and high heat transfer capacity.

This talk will cover the key points of the microchannels R&D with includes design optimization, fabrication, robustness tests, cooling performance and fluidic characterization.

A major challenge to be overcome concerned the reliable connection of the input cooling pipes to the substrate, via the fluidic connector. The connection must be completely leak tight to maintain the integrity of the vacuum and able to withstand the highest operational pressures. A flux free connector soldering solution was developed, in order to protect the cooling network from any long term chemical degradation. This solution also respects the planarity and correct positioning required for the subsequent construction of the precise tracking system. The procedure is a many step process, using formic acid cleaning and very close temperature control in both vacuum and atmospheric pressure environments. The integrity of the final joint is checked by tomography and helium leak tests. During the development phase of this procedure the solder joints were also tested for long term effects of creep and fatigue. The creep effects were enhanced by applying high temperatures and mechanical tension. The fatigue was studied with temperature (-40 to 60 degrees) and pressure (1 - 200 bar) cycles.

Various experimental setups were used to characterise the cooling performance. For proof-of-principle a setup was used that mimics the power dissipation of the final module via by special heaters designed to simulate the heat pattern in the ASICs and sensors, and measuring the temperature difference between the coolant and the irradiated module tip. The fluidic characteristics of the final system were assessed for a range of flows, including the nominal one of 0.4 g/s per module. In addition, setups with module pairs were used to study the cooling flow interplay between modules, in extreme situations such as loss of power on one module.

Two alternative solutions were pursued in parallel to the microchannel development, and these will be briefly described. In the end the microchannel evaporative cooling was selected due to the superior physics performance,

The status of the project, production, and prototypes will be described.

Pixel fast timing / 16

A High-Granularity Timing Detector for the Phase-II upgrade of the ATLAS Calorimeter system: detector concept, description and R&D and first beam test results

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The expected increase of the particle flux at the high luminosity phase of the LHC (HL-LHC) with instantaneous luminosities up to $L \approx 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ will have a severe impact on the ATLAS detector performance. The pile-up is expected to increase on average to 200 interactions per bunch crossing. The reconstruction and trigger performance for electrons, photons as well as jets and transverse missing energy will be severely degraded in the end-cap and forward region, where the liquid Argon based electromagnetic calorimeter has coarser granularity and the inner tracker has poorer momentum resolution compared to the central region. A High Granularity Timing Detector (HGTD) is proposed in front of the liquid Argon end-cap calorimeters for pile-up mitigation and for bunch per bunch luminosity measurements.

This device should cover the pseudo-rapidity range of 2.4 to about 4.0. Two Silicon sensors double sided layers are foreseen to provide a precision timing information for minimum ionizing particle with a time resolution better than 50 pico-seconds per hit (i.e 30 pico-seconds per track) in order to assign the particle to the correct vertex. Each readout cell has a transverse size of $1.3 \text{ mm} \times 1.3 \text{ mm}$ leading to a highly granular detector with about 3 millions of readout electronics channels. Low Gain Avalanche Detectors (LGAD) technology has been chosen as it provides an internal gain good enough to reach large signal over noise ratio needed for excellent time resolution.

The requirements and overall specifications of the High Granular Timing Detector at the HL-LHC will be presented as well as the technical proposal. Extensive LGAD R&D campaigns are carried out to investigate the suitability of this new technology as timing sensors for HGTD (sensor optimisation such as thickness, dead zone..., related ASICs, and radiation hardness). Laboratory and test beam results before and after irradiation will be presented.

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MAPS sensor for cosmic applications designed in 180 nm SOI CMOS technology

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The radiation tolerance is considered the main obstacle for space research with cosmonauts and in the colonization of the Solar system. The orbit radiation has a destructive effect for the electronic

systems (unreliability, Single Event Upset (SEU), degradation of component properties), device mechanics (natural damage) and naturally to the living organism, including humans. The ionizing radiation properties in the universe are qualitatively different from the terrestrial radiation sources. Therefore, the cosmic dosimetry concerning the instrumentations and effects is very different from the terrestrial dosimetry.

Since the end of the Apollo mission, human-flight is conducted in the Low Earth Orbit (LEO), where Earth's magnetosphere considerably protects astronauts. Flights beyond the LEO boundary, which are planned for the next decade by space agencies and private companies, are complicated due to radiation damage. A compact device that allows for the measurement of not only regular dosimetric quantities, but also the determination of the type of ionizing radiation and the biologic effect of radiation, is highly demanded by space agencies. The other required property of the device is the detection of the fast neutrons from energy events of the Sun magnetosphere, which can be a precursor to the arrival of a cloud of charged particles from the solar eruption and provides early warnings to the cosmonauts.

The Monolithic Active Pixel Sensor (MAPS), which is a revolutionary ionizing radiation detector, significantly improves the detection of physical parameters and enables new types of the measurement of physical quantities. A unique type of the dosimetric MAPS sensor, Lightweight Orbital Radiation Detection System (LORDS), was developed using a 180 nm deep submicron Silicon On Insulator (SOI) CMOS commercial technology, Figure 1, [1]. The design of LORDS, as shown in Figure 2, as well as circuit simulation and experimental results of the previous prototypes, will be presented. The experimental and simulation results are of great importance for the further development of the dosimetric MAPS detector, designed in SOI technologies, for the cosmic applications.

[1] T. Benka, M. Havranek, M. Hejtmanek, J. Jakovenko, Z. Janoska, M. Marcisovska et al., 2018 Characterization of pixel sensor designed in 180 nm SOI CMOS technology JINST 13 C01025

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Development of Time-over-Threshold ASICs for radiation sensors

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Time-over-Threshold (ToT) method is a time width signal processing applied to various area such as high energy physics and medical application. It can obtain not only a trigger timing information as an output signal rise edge, but also an incident radiation energy as an output signal time width. We have been developing ToT processing based ASICs for gamma-ray imaging devices. The current mode ToT ASIC for MPPC realizes high timing performance. For improving ToT's non-linearity between time width and incident radiation energy, we also developed dynamic ToT ASIC and slew-rate limited type ToT ASIC.

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Tracking with timing: a system approach

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High Luminosities planned at colliders of the next decades pose very severe requirements on vertex detector systems in terms of space resolution (tens of μm), radiation hardness (5 to 10×10^{16} $1 \text{ MeV neq cm}^{-2}$ and some Grad) and data throughput (nxTbit/s). Expected event pile-up (more than 100) introduces the need to add high resolution time measurements (better than 100 ps) already at the single pixel level, for both real-time and off-line track reconstruction.

This demand pushes towards a new concept of vertex detector system, where all these features must operate at the same time.

The TIMESPOT project (TIME and SPace real-time Operating Tracker), started in the end of 2017 is an R&D project whose strategy consists in facing this experimental challenge at system level. It consists of a research team gathering together state-of-the-art knowledges from different expertises and disciplines, in such a way to finalize existing technologies in the direction of an innovative tracking apparatus. This organic approach is a key point of the project. Our experience as experimentalists is that high performance is only possible by optimizing the details of a system as a whole, in particular considering the interplay of sensor and electronics.

The TIMESPOT activity is organized in several Work Packages (WP). Two WP are dedicated to sensor design and characterization (3D silicon and diamond sensors respectively). Their aim is a rad-hard device with optimized timing performance. One WP is dedicated to front-end design. Its target is the development of a high resolution time and space pixel read-out circuit. Other two WP are dedicated to the implementation of high speed, high density read-out boards, capable of real-time reconstruction of tracks. The final target is realizing a proto-tracker system demonstrator, having at least 4 fully equipped tracking layers, high speed data-taking and real-time processing.

Many interesting results are already available as an outcome of the TIMESPOT activity. In sensor development, a 3D trench-based geometry has been chosen to be the best one concerning high time resolution applications, desined and submitted for fabrication. Activity on the design of dedicated front-end in 28-nm CMOS has led to the submission of a complete pixel read-out circuit, also integrating a TDC with 15 ps r.m.s. resolution. A special care is being dedicated to the development of real-time reconstruction algorithms for tracking. Pre-processing is based on the concept of so-called stubs or tracklets, which are pre-constructed and combined already at the front-end level.

A full overview of the project will be given, covering its different aspects and activities. Results obtained during this first year, from sensor developments to front-end and back-end electronics, will be illustrated. Emphasis will be also given to real-time processing strategies and developments for real-time tracking, which concern both detailed simulation studies and first hardware demonstrators.

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Development of a front-end ASIC for CdTe Hybrid Pixel Detector

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We developed a front-end ASIC for a CdTe pixel detector as a part of a R&D effort toward advanced hard X-ray or gamma-ray imaging devices for applications in a variety of fields such as astronomy, medical research and non-destructive analysis. The ASIC is designed for a hybrid configuration where each CdTe pixel can be vertically bump-bonded to a corresponding pixel circuit. The chip consists of 28-by-28 identical cells of 250 μm -by-250 μm in silicon area, and is implemented with TSMC 0.35- μm CMOS technology. The signals are acquired either in the peak-hold or sample-hold mode before being fed into a column-parallel A-to-D converter. We tested circuit performance and confirmed that its equivalent noise charge was 40 electrons, its integral non-linearity about 1%, and the power consumption 0.2mW per pixel.

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Feasibility study of the algorithm for identifying multiple gamma-ray scattering sequence in a pixelated CdZnTe detector

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Cadmium Zinc Telluride (CZT) detectors have been of interest for X-ray and gamma-ray spectroscopy operating room temperature [1]. The use of CZT detectors has helped to increase both efficiency and effectiveness of detector performance in many applications, such as nuclear medical imaging and industrial imaging systems. However, the performance of the pixelated CZT detectors in the imaging applications is often limited not only by the inefficient charge collection within the detector [2] but also by the intrinsic spatial resolution based on the geometric size [3]. Moreover for the pixelated CZT detector as a component of the gamma-ray imaging device, such as a Compton camera, multiple scattering of gamma rays in the CZT material results in poor image resolution and image sensitivity. Generally only single-pixel photo-peak events are used in the imaging resolution, multiple gamma-ray events in the image reconstruction are not included even those events are dominant for the pixelated CZT detector [4]. To overcome this problem, multiple gamma-ray scattering sequence in the pixelated detector should be known.

In this work we present the algorithm for identifying multiple gamma-ray scattering sequence to improve the energy resolution and determine the interaction positions in a 16-pixelated CZT detector with dimensions of 5.9 mm x 5.9 mm x 5mm which has an array of 4 x 4 pixels with a pitch of 1.1 mm manufactured by eV Products. Two-pixel events were selected for the gamma-ray tracking from the Monte Carlo simulation studies using a GEANT4 simulation toolkit [5]. In order to determine the interaction depth in the detector, we used the correlation function between the pulse rise-times and the depths in the analysis. Two neighboring anode pulse shapes were digitally recorded with a 64-channel 62.5 MS/s digitizer (v1740B) manufactured by CAEN. By using data obtained for gamma rays emitted from a ²²Na standard source, we were able to conduct depth sensing and determining gamma-ray sequences.

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Single-Event-Hardened Timing Generator for Waveform Digitizer based readout electronics

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Analog waveform sampler, the soul of radiation detectors performing a multitude of functions has to evade Single-Event Transients (SETs) in its timing reference. The propagation of transients from the timing generator to the analog memory causes timing non-linearity due to variation in the inverter delay responsible for the sampling speed leading to catastrophic failure of the waveform sampler. The TG using Mixed-Signal Delay-Lock Loop (MSDLL) implements the triple combination of

body-feed technique allowing rail-to-rail operation for delay control, the pseudo differential structure regulating duty cycle reducing the jitter impacts optimizing the linear operating range of the Voltage Controlled Delay Line (VCDL) and the MSDLL embedded with dual-edge synchronization enhances the mitigation of Single-Event Upsets (SEUs). The simulation results at the circuit level using 180 nm and 90 nm CMOS PDKs show a 28% increase in the linear operating range and bettering jitter performance of the MSDLL. Furthermore, there is only negligible variance in the INL and DNL between the irradiated and non-irradiated values for reference clock of 500 MHz to 1 GHz and the resolution is between 16 to 25 ps with jitter of 10 ps.

The proposed TG circuit have exhibited performance benefits by mitigating the missing pulses and arresting the propagation of SEUs, there is a negligible difference of around 0.1 % between the irradiated and non-irradiated amplitude and timing non-linearity values of analog memory. The proposed analog memory achieves time resolution about 50 ps and is more SET tolerant.

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Beam-tests of prototype modules for the CMS High Granularity Calorimeter at CERN

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As part of its HL-LHC upgrade program, CMS is developing a High Granularity Calorimeter (HG-CAL) to replace the existing endcap calorimeters. The HG-CAL will be realised as a sampling calorimeter, including 36 layers of silicon pads and 16 layers combining both silicon+scintillator detectors interspersed with metal absorber plates. Starting from 2016, prototype modules, based on 6-inch hexagonal silicon pad sensors with pad areas of 1.0 cm², have been constructed. In 2017 and 2018, beam tests of different sampling configurations made from these modules have been conducted at CERN's SPS using beams of charged hadrons and electrons with momenta from 20 to 350 GeV/c. The setup was complemented with CALICE's AHCAL prototype, a scintillator-based sampling calorimeter, mimicking the proposed design of the HG-CAL's scintillator part. Most importantly, the new Skiroc2-CMS readout ASIC has been used in the silicon modules, facilitating the study of its timing capabilities in practice. This talk summarises the test beam efforts in 2017 and 2018. In particular, the setups and the encountered challenges are discussed. Preliminary results, including gain characterisation, calibration with minimum ionising particles and energy reconstruction performance of electron- and hadron-induced showers are shown. Finally, a first impression on the timing capabilities is given.

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jPix - a multiplatform acquisition package for Timepix 3

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We present a newly developed modular and multiplatform acquisition and control package dedicated for high performance Timepix 3 pixel detector. The software package was originally developed for operation at Atlas experiment. Afterwards, it was further extended as an independent package for general purpose measurements with Timepix 3.

Timepix 3 detector is a semiconductor detector of 256x256 square pixels providing information about energy and time of arrival with resolution less than 2 ns, which generate a high amount of data to

be processed in real time with the data acquisition package. The processed data stream from the detector can be stored on a hard drive and also displayed online using graphical interface with capability to control several number of acquisitions and display measured data using variable modules. Moreover, due to the architecture it can be further extended using external libraries working independently on the software. The software is developed in Java standard edition, which gives the possibility of deployment on various operating systems (Windows, Linux, MacOS, etc.). All peaks in data transmission can be further balanced by several buffers, which size depends on the available random access memory.

The software package architecture is based on independent modules. The modularity of the package and possibility of extensions working independently make the software unique. Also, basically, any number of detectors is supported. The possible number of connected detectors depends on the performance of DAQ computer and it is not limited by the software architecture. The package was tested to process 7 millions events per second when using SSD as a data storage.

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FPGA Accelerated Computing for Particle Identification in High-Energy Physics Experiments

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The key challenges in the recent nuclear and High-Energy Physics (HEP) experiments are high reaction rate and data rate. The data rate, the product of the event size and the reaction rate, ranges from 107 up to more than 1011 Bytes/s. This huge amount of data cannot be entirely recorded and processed during offline analysis. Interestingly, physicists have interest only in a very small proportion of all the event data that occur only once within one million interactions. Hence it provides the possibility to utilize an efficient online Data Acquisition (DAQ) and Trigger system to reject uninteresting events while identify and retain interesting ones in real-time.

The paper assesses the machine learning assisted particle identification algorithms on an FPGA based computing platform for HEP experiments. To achieve the highest classification accuracy in particle identification the combination of particle recognition algorithms and random decision forests algorithms are laid on an accelerated computing platform utilizing the FPGA cluster to classify the particles of interest. The simulation results of this implementation achieve many benefits through dynamic and intelligent design management, such as efficient resource utilization and high performance-cost ratio.

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Alpha calibration of the Timepix pixel detector exploiting energy information gained from a common electrode signal

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An alternative calibration method of pixel detector Timepix has been developed. Unlike a standard per-pixel calibration method where just single pixel tracks of low energy gammas and fluorescence roentgens are used as an input, the new method is based on the evaluation of charge distribution within multi pixel tracks of energetic alpha particles.

The new method gets practicable if energy of interacting alpha particles is precisely known. The Timepix pixel detector allows a simultaneous run of measurement in the pixel part as well as in the common electrode when a specialized read-out interface FITPix COMBO is used. The common electrode, opposite one to the pixel electrode, provides a natural sum of energy of all affected pixels among which the particle deposited charge has been shared.

The distribution of energy between pixels belonging into alpha tracks has been evaluated and dependency between partial energy and time over threshold value counted in individual pixels has been solved. Knowing the energetical dependency, it is possible to form a matrix of calibration parameters. The method has been proved for alpha particles of regular energies. The energy resolution of the pixel detector after calibration is comparable to the resolution of common electrode signal.

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The All-sky Medium Energy Gamma-ray Observatory: Instrument and Mission Capabilities

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The All-sky Medium Energy Gamma-ray Observatory (AMEGO) is a probe-class mission in consideration for the 2020 decadal review designed to operate at energies from ~200 keV to >10 GeV. Both Compton scattering and pair-production events must be considered in the AMEGO design since the interaction cross section has a crossover at a few MeV. AMEGO is made of four major subsystems: a plastic anticoincidence detector for rejecting cosmic-ray events, a silicon tracker for measuring the energies of Compton scattered electrons and pair-production products, a CZT calorimeter for measuring the energy and location of Compton scattered photons, and a CsI calorimeter for measuring the energy of the pair-production products at high energies. The prototype subsystems are under development; in this contribution we focus on the details on the development of the silicon tracker subsystem including the potential role of silicon pixel detectors in preparation for beam tests and a balloon flight.

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First CMS results on 3D pixel sensors interconnected to RD53A readout chip after high energy proton irradiation

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In this presentation results obtained in beam test experiments with 3D columnar pixel sensors interconnected with the RD53A readout chip are reported. RD53A is the first prototype in 65nm

technology issued from RD53 collaboration for the future readout chip to be used in the upgraded pixel detectors. The interconnected modules have been tested on hadron beam at CERN before and after irradiation, in the CERN IRRAD facility, to an equivalent fluence of $1E16$ neq/cm² (1MeV equivalent neutrons). All results are obtained in the framework of the CMS R&D activities in view of the pixel detector upgrade for the High Luminosity phase of the LHC at CERN (HL-LHC). The sensors were made in FBK foundry in Trento, Italy, and their development was done in collaboration with INFN (Istituto Nazionale di Fisica Nucleare, Italy). Preliminary analysis of collected data shows hit detection efficiencies around 97% measured after high energy proton irradiation.

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The CMS High Granularity Calorimeter for HL-LHC

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Calorimetry in high-energy physics is rapidly evolving, with new challenges and a wide variety of technologies being employed, both for signal creation and detection. Advances in large-area highly-segmented detectors are providing possibilities for high-granularity calorimetry. The CMS HGCAL, being designed to replace the existing CMS endcap calorimeters for the HL-LHC era, is one example. It is a sampling calorimeter, featuring unprecedented transverse and longitudinal readout segmentation for both electromagnetic (CE-E) and hadronic (CE-H) compartments. This will facilitate particle-flow calorimetry, where the fine structure of showers can be measured and used to enhance pileup rejection and particle identification, whilst still achieving good energy resolution. The CE-E and a large fraction of CE-H will use hexagonal silicon sensors as active detector material. The lower-radiation environment will be instrumented with scintillator tiles with on-tile SiPM readout. An overview of the HGCAL project will be presented, covering motivation, engineering design, readout and trigger concepts, and performance in simulation.

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Beam test results of an SOI monolithic pixel sensor SOFIST for the ILC vertex detector

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The ILC experiment needs a vertex detector with satisfactory space and time resolutions to reconstruct decays of heavy flavor quarks and tau leptons for precise measurement of the Higgs boson and search for physics beyond the Standard Model. We have been developing a monolithic pixel detector for the ILC, SOFIST, with Silicon-on-Insulator technology; this is fabricated using a 200 nm FD-SOI CMOS process developed by LAPIS Semiconductor Co., Ltd. We aim to achieve a 3 μ m single-point resolution required for the ILC with a 20 \times 20 μ m² pixel size. Each pixel is to record the charge and time stamp of a hit to identify a collision bunch for event reconstruction. Necessary functions include the amplifier, comparator, shift register (memory sequencer) and multiple analog and time stamp memories implementation in each pixel, and column ADCs and Zero-suppression logic per chip.

Our second prototype sensor, SOFIST ver.2 has the analog memories and the time stamps but in separate pixels of 25 \times 25 μ m² to evaluate the functions individually. We tested SOFIST ver.2 with

120 GeV proton beam at Fermilab Test Beam Facility in February 2018. An array of 64×80 pixels has about 2 mm² active area in an overall chip size of 4.45 mm square. Preliminary result of timing resolution better than 2 μs has been obtained.

We report the results of the beam test and recent status of the third and fourth SOFIST developments.

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Estimation and imaging of recoil electron with event-driven SOI sensor and deep learning in Compton imaging system

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In conventional method of Compton imaging, only the information of gamma rays is used to estimate the location of radiation source. However, because of the information deficiency of recoil electrons occurred in Compton scattering process, signal-to-noise ratio (SNR) and angular resolution will be reduced. Recently, deep learning has become an increasingly important hot pot. With deep learning, the correct label of recoil electrons energy deposit image is made and divided into practice data for learning and test data for prediction. With the prediction results of direction vector and scatter plane deviation (SPD), the imaging of recoil electrons is carried out.

Based on it, we explore a new approach for recoil electrons tracking using trigger-mode Silicon-On-Insulator (SOI) sensor with a pitch of 36μm which named XPRIX6c. The XRPIX series is one of the "SOIPIX" detector, which is an active pixel sensor based on SOI complementary metal-oxide-semiconductor (CMOS) pixel technology [1]. XPRIX6c consists of 48×48 pixels, and each pixel has a charge integration circuit and trigger circuit [2][3]. The ejected direction of a recoiled electron is detected on the SOI pixel detector. And then, using Geant4, ¹³⁷Cs whose energy is 662keV was simulated to get the data of recoil electrons trajectories. In this simulation, the distance of source and detector was 5cm and 200 files of which each contained more than 700 Compton scattering information was used for deep learning. Through the combination, the ejected direction in three-dimension can be identified and the accuracy of imaging can be improved.

We obtained the recoiled electron trajectories of ¹³⁷Cs with trigger-mode SOI pixel detector and through deep learning, we did prediction to get more accurate imaging. We will show the results.

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Improvement and Evaluation of Event-driven Performance with Double-SOI Pixel Detectors for X-ray Astronomy

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We have been developing a monolithic active pixel sensor with the silicon-on-insulator (SOI) CMOS technology for use in future X-ray astronomical satellite missions. Our objective is to replace the X-ray Charge Coupled Device (CCD), which is the standard detector in the field, by offering high coincidence time resolution (~ 50 ns), superior hit-position readout time (~ 10 μ s), and wide band-pass (0.5 – 40 keV) in addition to having comparable performances in imaging spectroscopy. We have been developing prototype detectors, called “XRPIX” series. XRPIX contains comparator circuit in each pixel to detect an X-ray photon injection; it offers intra-pixel hit trigger (timing) and two-dimensional hit-pattern (position) outputs. Therefore, XRPIX is capable of direct access to selected pixels to read out the signal amplitude. In our previous study, we evaluated its basic imaging spectroscopic performance and obtained the X-ray spectra by this system. Recently, we designed a prototype device named XRPIX6D, to which we introduced a Double-SOI structure, to improve an X-ray responsivity. The difference from the conventional SOI wafer is that the Si layer, called middle-silicon is added to the buried oxide layer. The Double-SOI structure reduces the parasitic capacitance between the sense-node and the CMOS circuit by fixing the potential of middle-Si layer, and suppresses crosstalk between them. This structure is also expected to increase in conversion gain due to reduction in the sense-node parasitic capacitance and increase in closed-loop gain due to reduction in the feedback parasitic capacitance. XRPIX6D has the chip output gain of 40.5 μ V/e⁻, and the readout noise of 16 e⁻(rms), the energy resolution of 290 eV in full width at half maximum for 6.4 keV X-rays in all pixel readout mode. We successfully improved the spectroscopic performance also in the event-driven readout mode. Furthermore, we improved the event determine rate by introducing a hit-pattern processing circuit in XRPIX.

Pixel SOI, X-ray / 35

Evaluation of X-ray astronomical SOI CMOS pixel sensor aimed at improving charge-collection efficiency

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We have been developing monolithic active pixel sensors for X-ray astronomy, referred to as “XRPIX”, based on silicon-on-insulator (SOI) CMOS technology. Each pixel has a buried p-well (BPW) around sense node at the pixel center to suppress the back-gate effect. In our early device, XRPIX1b, charge-collection efficiency (CCE) was degraded because the in-pixel circuitry placed outside the BPW affected the electric fields of the sensor layer. Our next device, XRPIX2b, improved the CCE by rearranging the placement of the circuitry on or near the BPW. However, the CCE at the pixel borders was still lower than that at the pixel center. Based on this result, We developed a new device, XRPIX6H, with more concentration of the circuitry inside the BPW. We measured the X-ray response of XRPIX6H and confirmed further improvement of the CCE at the pixel borders. A simulation study on the electric field convergence toward the sense node about XRPIX2b and XRPIX6H are also presented.

Pixel for upgrade / 7

Performance of FBK/INFN/LPNHE thin active edge n-on-p pixel detectors for the upgrade of the ATLAS Inner Tracker

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In view of the LHC upgrade phases towards the High Luminosity LHC (HL-LHC), the ATLAS experiment plans to upgrade the Inner Detector with an all-silicon system.

The n-on-p silicon technology is a promising candidate to achieve a large area instrumented with pixel sensors, since it is radiation hard and cost effective.

The paper reports on the performance of thin (100 and 130 μm thick) and edgeless n-on-p planar pixel sensors produced by FBK-CMM. The production featured standard 50 $\mu\text{m} \times 250\mu\text{m}$ pixel pitch modules,

compatible with the ATLAS FEI4B readout chip, and small 50 $\mu\text{m} \times 50\mu\text{m}$ and 25 $\mu\text{m} \times 100\mu\text{m}$ pixel pitch modules, compatible with the RD53A readout chip prototype.

After discussing the sensor technology an overview of 2018 testbeam results of the produced devices will be given, before and after irradiation, including charge collection and hit efficiency, with a special focus on the hit efficiency at the detector edge.

Pixel for upgrade / 59

Characterization of RD53A compatible n-in-p planar pixel sensors

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The ATLAS experiment will undergo around the year 2025 a replacement of the tracker system in view of the high luminosity phase of the LHC (HL-LHC) with a new 5-layer pixel system.

Thin planar pixel modules are the baseline technology to instrument all layers of the new pixel system, with the exception of the innermost one, thanks to their high charge collection efficiency after irradiation and reduced power dissipation. Pixel sensors, 100-150 μm thick, produced at MPG-HLL, interconnected to RD53A read-out chips, have been characterized with radioactive source scans and beam tests.

New designs of the pixel cells have been implemented in recent n-in-p planar pixel productions, to address the challenges presented in terms of charge collection by the small pixel pitches of $50 \times 50 \mu\text{m}^2$ and $25 \times 100 \mu\text{m}^2$, under consideration for the ATLAS pixel upgrade.

A comparison of the performance of different sensor designs will be presented, based on the electrical characterization of these devices with IV curves, radioactive sources and beam tests. The main design features that have been investigated regard the implementation of the biasing grid and the inactive edge dimensions, for the two thickness and pitch parameter values under study.

These results give important information to decide on the last open design parameters for the ATLAS ITk planar pixel production

Pixel for upgrade / 50

MALTA: an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade.

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The ATLAS tracking detector will be upgraded with the Inner Tracker (ITk) for the High-Luminosity Large Hadron Collider (HL-LHC) at CERN. The tracking system will be fully made of radiation hard silicon sensors. A process modification in a standard 0.18 micron CMOS imaging technology combines small, low capacitance electrodes of around 2 fF for the sensor with a fully depleted active sensor volume. The measurements on the first prototypes in this technology demonstrate a radiation hardness promising to meet the requirements of the ATLAS ITk outer pixel layers ($1.5 \times 10^{15} \text{ MeV neq/cm}^2$), with a fast signal response, compatible with the HL-LHC 25ns bunch structure. The front-end was optimised for this low capacitance to achieve low noise ($\text{ENC} < 20 \text{ e}^-$) and low power operation ($1 \mu\text{W}/\text{pixel}$).

After the encouraging results, two monolithic CMOS sensor prototypes a $20 \times 20 \text{ mm}^2$ monolithic

CMOS sensor prototype Malta has been designed for the ATLAS ITk outermost pixel layer. Malta features a 512×512 matrix of $36.4 \times 36.4 \mu\text{m}^2$ pixels with a small electrode size of $\sim 2 \mu\text{m}$, without clock distribution over the matrix and a fully asynchronous readout, designed to meet the challenging hit-rate requirements of up to $2 \text{MHz}/\text{mm}^2$ in the outer layers of the ITk detector.

The sensor presents forty of the LAPA drivers, a pseudo-LVDS differential buffer designed for the data transmission over the full length of the ITk detector, with a data rate up to 1.28 Gb/s. The parallel outputs allow extensively studying the behaviour of the asynchronous pixel matrix.

Extended measurement results show that efficiency after irradiation is degraded especially in the pixel corners due to a higher threshold and larger pixel pitch ($36.4 \times 36.4 \mu\text{m}^2$ instead of $25 \times 25 \mu\text{m}^2$ and $30 \times 30 \mu\text{m}^2$), with respect to the first prototypes. The results have been confirmed by a well established synchronous architecture and different pixel layout, MONOPIX, developed in parallel with MALTA. Detailed comparisons on test beam measurements have correlated efficiency with deep pwell implants layout.

This initiated investigation to improve the lateral field in the pixel corners and achieve the desired radiation hardness, driving the design of new test structures.

The design of Malta will be presented together with laboratory and test beam measurements results, before and after irradiation, together with possible improvements.

Pixel for upgrade / 71

Study of efficiency and noise of fine pitch planar pixel detector for ATLAS ITk upgrade

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In the recent development of pixel detectors for the ATLAS Inner Tracking detector upgrade, thin planar pixel detector has been developed and ready for the production. A half size readout ASIC, RD53A, which supposed to be the last prototype before the pre-production chip is available. The RD53A chip compatible sensors are developed at KEK/HPK in Japan and flip-chipped modules are tested by testbeam before and after irradiation. To minimize the noise from the sensor surface structure, the optimization of the biasing network structure has been performed. The noise level highly depends on the resistivity of biasing network and the capacitance between biasing network and electrode. In this presentation, the efficiency measurement by testbeam and sensor surface structure optimization to reduce noise are presented.

X-ray system / 52

Calibration of the AGIPD detector system at the European XFEL

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The Adaptive Gain Integrating Pixel Detector (AGIPD) is a hybrid pixel detector developed by DESY, PSI, and the Universities of Bonn and Hamburg for the European XFEL. The first 1 MPix system was installed in 2017 at the SPB beamline, and has been successfully used in the first user experiments. Several other AGIPD systems (1 MPix for MID, 1 MPix for HIBEF, and 4 MPix for SFX) are currently being constructed and installed at the European XFEL beamlines.

The AGIPD was designed to cope with the extraordinary requirements of the European XFEL beam structure. The detector features a high frame rate, large dynamic range, and single photon sensitivity. Each pixel utilizes an adaptive gain switching technique with three gain stages and contains 352 storage cells.

The size and complexity of the system results in more than a billion calibration constants for a 1 MPix detector. The constants are determined using a combination of dark and x-ray measurements and on-chip calibration sources. In this talk, we will present the calibration concept currently implemented for the 1 MPix system, the acquisition and analysis of several TB of calibration data, and planned improvements, as well as the challenges that will come along with the addition of the new of AGIPD systems.

X-ray system / 45

EIGER: High frame rate pixel detector for synchrotron and electron microscopy applications

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The EIGER detector is since a few years the gem of single particle counting detectors for synchrotron applications. EIGER is a hybrid pixel detector featuring $75 \times 75 \mu\text{m}^2$ pixel size and the low noise (down to 100 e^- ENC RMS). The chip design and the complete readout system development was done at the Paul Scherrer Institut, Switzerland. A few detector systems (ranging from 0.5 to 9 Mpixels) are installed at beamlines at various synchrotrons. The detector is able to acquire data at 22000 frame/s with 4-bit counter depth, independently from the system size. This very high frame rate has opened the path to time resolved experiments at unprecedented scales: results from experiments at synchrotrons will be shown. Insights on the challenges given by the large data volume handling at this high frame will be given.

The similarities between data collection techniques at synchrotrons and with transmission electron microscopes (TEMs) have lead to the trial of EIGER as an electron detector. EIGER has been tested

at electron energies 100–300 keV, typical for TEMs. The stopping power of electrons varies a lot with these electron energies and the multiple scattering can be substantial. EIGER shows good performance at 100 keV, where the size of the electron interaction is still contained in a single pixel. However, the high frame rate capability makes EIGER still suitable even at 200–300 keV, despite the large multiple scattering, for applications where a rotation method (electron crystallography) or a raster scan (scanning TEMs) require a fast detector to limit the dose on the sample. Similarly, we have also tested the detector for lower electron energies (8–20 keV), interesting for photo-emission electron microscopy. The Si sensor design has been optimized to reduce the entrance window of the sensor, where low energy electrons stop or scatter. We now want to study the detector performance at ≈ 1 MeV electron energy, where electrons start behaving as minimum ionizing particles.

X-ray system / 11

Design of a scientific CCD camera with a large focal plane of 4k x 4k pixels

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A scientific CCD camera with 4k by 4k pixels and compact size is designed which can be used for astrophysics, Particle Physics, biology, medicine and material Science. This camera uses a CCD detector with model CCD230-84 from Teledyne e2v (UK) Ltd. The detector is a back illuminated detector with QE higher than 90% at 500nm to 650nm wavelength, which has split readout registers at both top and bottom with charge detection amplifiers at both ends. The pixel size is 15 μm square. The image area has four separately connected sections to allow full-frame, frame transfer, split full frame or split frame-transfer modes. Depending on the mode, the readout can be through 1, 2 or 4 of the output circuits.

The hardware structure of the camera system includes three parts: vacuum head, CCD controller, and power and temperature controller unit (PTC). The vacuum head and the CCD controller constitute the main body of the camera named “camera head”. In the vacuum head, a thermoelectric cooler (TEC) is used to refrigerate the detector for lower readout noise and dark current noise. Both air cooling or water cooling could be used for the system heat dissipation. The CCD could be refrigerated to -60 degree centigrade with water cooling mode or be refrigerated to 50 degree centigrade below ambient temperature when using air cooling. The vacuum is vacuum sealed with vacuum clamping technology. The signals of the CCD detector and the TEC connect to the CCD controller through four 26 pins vacuum feedthrough connectors. The CCD controller provides interfaces with the host computer and the PTC unit, drive biases and clocks for the detector, and four readout channels with ACDS sampling technology and maximum readout speed of 500kpixels/channel/s. The PTC takes 24V as the input power and generates multiple voltages for the controller. Meanwhile the PTC implements the high precision temperature feedback control for the TEC with a STM32 microcontroller. A 19 pins cable is used for connecting the PTC and the CCD controller.

The whole size of camera head is just $\varnothing 165\text{mm} \times 300\text{mm}$, and the size of the PTC is $183\text{mm} \times 55\text{mm} \times 95\text{mm}$. So the camera is very compact and easy to be assembled. The camera has been tested for the imaging function, gain, dark current and readout noise. The readout noise is measured as 9.3 electrons (rms) with 500 KHz readout speed.

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Radiation Hardness of a P-Channel Notch CCD Developed for the X-ray CCD Camera onboard the XRISM Satellite

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We have investigated the radiation hardness of a P-channel CCD developed for the X-ray CCD camera onboard the XRISM satellite. This CCD has basically the same characteristics as the one used in the previous Hitomi satellite, but newly employs a notch structure of potential for signal charges by increasing the implant concentration in the channel. The new device was exposed up to approximately 8×10^{10} protons cm^{-2} at 100 MeV. The charge transfer inefficiency was estimated as a function of radiation dose with ^{55}Fe . A device without the notch structure was also examined for comparison. The result shows that the notch device has the significantly higher radiation hardness than those without the notch structure including the device adopted for Hitomi. This proves that the new CCD is radiation tolerant for the space application with a sufficient margin.

Pixel radiation study / 3

Modeling Radiation Damage to Pixel Sensors in the ATLAS Detector

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Silicon pixel detectors are at the core of the current and planned upgrade of the ATLAS experiment at the LHC. Given their close proximity to the interaction point, these detectors will be subject to an unprecedented amount of radiation over their lifetime. At the LHC, the innermost layers will receive damage from non-ionizing radiation in excess of a fluence of 1015 1 MeV neq/cm², and at the HL-LHC the detector upgrades must cope with one order of magnitude larger fluence. This talk presents a digitization model incorporating radiation damage effects to the pixel sensors, based on Technology Computer Aided Design (TCAD) model. The model is described in detail and predictions for basic pixel cluster properties such as the charge collection efficiency and Lorentz angle are presented alongside validation studies with Run 2 collision data.

Pixel radiation study / 8

Study of damages induced on ATLAS silicon by fast extracted and intense proton beam irradiation

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The ATLAS silicon tracker detectors are designed to sustain high dose integrated over several years of operation. This very substantial radiation hardness should also favour the survival of the detector in case of accidental beam losses.

An experiment performed in 2006 showed that ATLAS Pixel detector modules (silicon planar hybridly coupled with FE-I3 electronics) could survive to beam losses up to 1.5 10¹⁰ protons/cm² in a single bunch with minimal or no deterioration of performance.

The upgrade of LHC to even higher luminosity (HL-LHC) calls for a new test of these properties.

Two test beam campaigns have been done in 2017 and 2018 at the High-Radiation to Materials (HiRadMat) Facility of the CERN Super Proton Synchrotron in order to establish for the first time the damage threshold of different types of ATLAS IBL pixel and strip detectors under very intense proton beam irradiation.

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BEAST results on SuperKEKB beam induced background with special emphasis on the PLUME pixelated system

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BEAST is an experimental effort to measure the parasitic particle rate induced by the nano-size beam exploited by the high-luminosity SuperKEKB e⁺e⁻ collider.

During its first data taking period, phase 2 in 2018, the inner volume of the Belle II detector was only partially equipped with the final vertex detector technologies. The remaining volume was covered with various other systems as part of the BEAST setup. Among them, the ultra-light PLUME system was made of two double-sided layers of CMOS pixel sensors.

The BEAST sensors operated during the whole phase 2, with single or two beams and with various machine settings. We will report on the characterization of the particle background observed with the BEAST setup and discuss in particular the benefits of the pixelated PLUME system.

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Radiation-induced effects on data integrity and -link stability of RD53A

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The phase-2 upgrade of the LHC will substantially increase the instantaneous luminosity. This requires novel pixel readout chips with highly complex digital architectures, which deliver hit information at drastically increased data rates and unprecedented radiation tolerance, especially close to the interaction point. The RD53 collaboration was formed to approach these challenges by designing a prototype pixel readout chip in 65 nm CMOS technology, which is suitable for the innermost layers of the pixel detector in the ATLAS and CMS experiments.

The large scale prototype chip RD53A has been produced and is available since December 2017. The locking behavior and the stability of the high speed Aurora links of un-irradiated RD53A chips have been investigated in lab environments with different cables, powering schemes, PLL configurations and synchronization patterns. Performance characterization measurements of the output line drivers are ongoing.

In order to perform characterization- and test beam measurements, the readout system BDAQ53 has been developed. It consists of an FPGA-based readout board and a Python-based data acquisition and analysis framework.

First irradiation studies at room temperature up to the design goal of 500 Mrad have shown that the data link fails after ~300 Mrad and that it only partially recovers after annealing. In order to understand the degradation of the clocking- and communication periphery of RD53A, further investigations are necessary.

During the upcoming irradiation campaigns, the chip will partially be operated in a non-default bypass mode, in which the integrated PLL and Command Data Recovery units are not used. This allows to operate the chip in a wider frequency- and digital supply voltages range. Various scan routines will monitor the chip performance during the campaigns. The digital logic of the chip will be monitored by continuously running communication tests and injection-based threshold scans. Variations in the threshold distribution and noise of the analog front-ends will be analyzed as a function of the Total Ionizing Dose.

Based on the results, methods to improve the operating parameters and design changes for the upcoming RD53B chip submission will be evaluated and discussed.

ASICs, Electronics / 19

Development and Performance of the CMS Phase-I Pixel DAQ in 2018

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The CMS Phase-I Pixel detector DAQ system relies on custom and standard microTCA parts. The combination of the robust online software and firmware development during 2018 operation made it possible towards a smooth and efficient data taking for the Pixel detector. We developed several complex software techniques to deal with the regular data-taking problems as they appeared. A significant improvement was brought in by a new firmware for Pixel Front-End Controller (PixelFEC)

which drastically reduced Pixel configuration time and contributed towards a faster and more complete recovery from detected soft errors during physics runs. We discuss here the CMS Phase-I Pixel DAQ system, its performance and operational experience during 2018.

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VeloPix readout and ASIC

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This presentation will describe the ASIC and readout system designed for the new pixel vertex detector (VELO) of the upgraded LHCb experiment. All elements of the new electronics readout chain will be designed to cope with the requirement of 40 MHz full event readout rate. The pixel sensors are equipped with the VeloPix ASIC and placed at 5 mm from the beam in a secondary vacuum tank and extremely high and inhomogeneous radiation environment.

The VeloPix ASIC has been designed for data-driven readout in the trigger-less architecture of the experiment, where particle rates reach up to 800 million particles per second per cm², resulting in an unprecedented peak data rate of nearly 15 Gbit/s for a single ASIC. The data rate envisaged for the 41M pixels of the whole VELO will be 1.6 Tbits/s. The use of 'super pixels' and a novel architecture for the internal data-path ensures a nearly dead-timeless and very power efficient readout. Each module houses six VeloPix hybrids, wire bonded to two front end hybrids. These are connected via low mass flex tapes to a control hybrid which routes the high speed signals and transmits the control signals from the GBTx ASIC using one up and one down link of 4.8 Gbps. Small tapes (15 cm) with micro strip lines then route the high speed signals, reducing the material in the acceptance area. In the next step the signals are transmitted to the wall of the vacuum chamber at rates of 5.12 Gbits/s via 56 cm long flexible copper low mass tapes. A custom board routes the signals outside the vacuum tank and once on the air side, an Optical and Power Board converts the electrical high speed signals into optical signals for transmission from the cavern to the surface. Because of the great importance of the (nearly) faultless transmission of data at very high speeds, we have carried out a long campaign of simulations and measurements of the whole transmission chain during the past five years and performed Bit Error Rate, S-parameter, eye diagram and impedance studies.

Given the proximity to the LHC collisions region, the ASIC has to withstand extreme radiation doses of 370 MRad and 8×10^{15} 1MeV neq cm⁻². Test results of a total ionising radiation dose with X-rays and of single event upset and latch-up with heavy ion beams showed that logic cells of a custom library were vulnerable to latch-up, which could be nicely confirmed by use of a micro-focussed laser charge injection and comparing to prediction from CAD layout. The pixel analogue preamplifier and discriminator have been designed for low noise and time-walk to guarantee high efficiency on low charges collected from heavily irradiated sensors. A local in-pixel adjustment circuit provides a very uniform single threshold operation. The ASIC is produced in a commercial 130nm technology and results of wafer-probe tests will be shown.

The architecture of the readout chain from the point of view of high speed signals and the performance will be described, together with the latest results from the VeloPix ASIC.

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Serial Powering for the Phase 2 upgrade of the CMS pixel detector

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A serially powered pixel detector is the baseline choice for the High Luminosity upgrade of the inner tracker of the CMS experiment. A serial power distribution scheme, compared to parallel powering, requires less cable mass, offers higher power efficiency and is less susceptible to voltage transients. A prototype pixel readout chip has been designed for serial powering in 65nm CMOS technology by the RD53 collaboration. Performance results from testing these prototype chips are shown. A comparison of the performance of the chips in conventional powering and operation in a chain consisting of four chips powered in series is presented. Additionally, the performance of the chips in the different operation modes is presented in a high hit rate environment. The results indicate that serial powering is a robust and reliable power distribution scheme.

ASICs, Electronics / 4

Single Event Upsets in the ATLAS IBL Frontend ASICs

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During operation at instantaneous luminosities of up to $2 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ the frontend chips of the ATLAS innermost pixel layer (IBL) experienced single event upsets affecting its global registers as well as the settings for the individual pixels, causing, amongst other things loss of occupancy, noisy pixels, and silent pixels. A quantitative analysis of the single event upsets as well as the operational issues and mitigation techniques will be presented.

Pixel SOI, X-ray / 60

Results from test-beam measurements of monolithic pixel detectors in SOI technology

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Tracking and vertex detectors at future linear colliders such as CLIC require a high-precision position measurement. A single-point spatial resolution of about 3 microns is foreseen for the CLIC vertex detector. In order to achieve this goal, detectors with low material budget and small pitch have to be developed. One solution for this are monolithic pixel structures. These do not require bump-bonding of individual sensor and read-out ASICs, which leads to an overall lower material budget with reduced multiple scattering and improved spatial resolution.

The Silicon-On-Insulator CMOS is one of the modern silicon technologies that allows to fabricate the monolithic pixel structures in which the readout electronics and the sensor matrix are integrated on the same wafer. In this talk, the test-beam data analysis results of Lapis 200nm SOI pixel detectors are presented. The SOI detectors were designed in AGH-UST in Cracow and tested at the CERN SPS

H6 beam line in 2017.

The presented detectors were fabricated on two different wafers type: FZ(n) and Double SOI(p), with thicknesses of 500 μm and 300 μm respectively. The pixel size was 30x30 μm . The tested matrix consisted of two pixel types: source-follower and charge-preamplifier architecture. The data analyses focused on spatial resolution and efficiency estimation. A novel procedure of eta-correction for multi-pixel clusters was introduced. Moreover, the influence of various clusterization methods on single-point resolution was studied. Finally, single-point resolutions below 2.4 μm for the FZ(n) wafer and 3.5 μm for the DSOI(p) was achieved. A high detector efficiency of about 98% was measured. Such performance shows that the tested structures are promising prototypes, fulfilling the condition for spatial resolution, for the CLIC vertex and tracking detectors.

Pixel SOI, X-ray / 37

Subpixel Response of Double-SOI Pixel Detectors for X-ray Astronomy

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We have been developing the X-ray SOI (Silicon-On-Insulator) pixel detector named XRPIX for the future astrophysical satellites. XRPIX is a monolithic active pixel sensor composed of high-resistivity Si sensor, thin SiO₂ insulator and CMOS pixel circuits by utilizing the SOI technology. Since XRPIX is capable of event-driven readout, it can achieve a high timing resolution better than $\sim 10 \mu\text{s}$, which enables a low background observation by adopting the anti-coincidence technique. One of the major issues in development of XRPIX was the electrical interference between the sensor layer and the circuit layer, which caused problems in the detector response: non-uniform detection efficiency and low charge collection efficiency at pixel boundaries. In order to reduce the interference, we recently introduced a Double-SOI structure, in which a thin Si layer (middle Si) was added in the insulator layer of SOI structure. In this structure, the middle Si layer works as an electrical shield to decouple the sensor layer and the circuit layer. In this work, we measured the detector response of the XRPIX with Double-SOI structure at KEK. We irradiated X-ray beam collimated with 4 μm Φ pinhole, and scanned the detector with 6 μm pitch, which is 1/6 of the pixel size. In this presentation, we will present the improvement of uniformity of the detection efficiency and charge collection efficiency in the Double-SOI detectors, and discuss the detailed X-ray response and its physical origin.

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Pushing the Limits of Kyoto's SOI Pixel Sensor for X-ray Astronomy with the Pinned Depleted Diode

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We have been developing SOI pixel sensors for X-ray astronomy, called “XRPIX”, which are fabricated using the silicon-on-insulator CMOS technology. XRPIX aims to detect X-rays in the energy band from 0.5 keV to 20 keV. The device consists of a fully depleted high-resistivity silicon sensor layer, a low-resistivity silicon layer for CMOS readout circuit, and a buried oxide layer in-between. The readout circuit has an event trigger output function, and reads out only pixels with an X-ray signal, thereby achieving a good time resolution and high throughput. Our latest device, XRPIX6E, is equipped with the Pinned Depleted Diode (PDD) structure (Kamehama et al. 2018), which greatly reduces stray capacitance at the charge sensing node, the dark current from the interface between the sensor layer and the buried oxide layer, and capacitive coupling between the sensing node and the readout circuit. The PDD structure also helps to improve the collection efficiency of the signal charge in the sensor layer. With XRPIX6E, we already achieved an energy resolution of 335 eV (FWHM) for 6.4 keV X-rays (Harada et al. submitted). Optimizing various bias voltages applied to the device and also integration time after a trigger output, we have succeeded in further improving the energy resolution and have achieved 200 eV (FWHM) at 6.4 keV in the readout mode using the event trigger output function. In order to characterize the device in more detail, we are conducting various experiments. One of them is a mesh experiment (Tsunemi et al. 1997) to study the sub-pixel response. Another is X-ray irradiation with a back-illumination configuration to evaluate the soft X-ray performance. In the presentation, we will report on the results of these experiments.

Pixel SOI, X-ray / 10

X-ray imaging with high-Z sensors for the ESRF-EBS upgrade

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The European Synchrotron Radiation Facility (ESRF) is being subjected to the second phase of its upgrade. Thanks to this upgrade, the new storage ring will be able to deliver extremely brilliant and coherent X-ray beams, setting advanced requirements for the detection schemes used. Consequently, the detector development is aiming to an improved performance in terms of spatial resolution and detection efficiency.

In this regard, our group is active on the development of pixelated detectors using semiconductor sensors for photon counting. The existing silicon sensors are sufficient for soft X-ray experiments. To counterbalance limitations set to the detection efficiency as the X-ray energy increases and operate our detectors to energies in the range 30-100 keV, we investigate the use of semiconductor sensors made of high-Z materials.

Several prototype modules based on CZT, CdTe and GaAs sensors have been developed and tested in terms of imaging performance at the ESRF beamlines. Each module, consisting of a sensor bonded to a single Timepix chip, is coupled to the MAXIPIX readout system. I will report on the results obtained focusing on the comparison of the performance achieved among different sensors, including measurements of the modulation transfer function (MTF), the detective quantum efficiency (DQE) and the spatial homogeneity.

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R&D status of the Monopix chips: Depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS Inner Tracker upgrade

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We summarize the characterization status for two different depleted monolithic CMOS active pixel sensor (DMAPS) prototypes with a fully synchronous column-drain read-out architecture: LF-Monopix and TJ-Monopix. These chips are part of a joint effort aiming towards a suitable implementation of a radiation-hard DMAPS with a fast readout architecture for the HL-LHC ATLAS Inner Tracker (ITk) upgrade.

LF-Monopix (March 2017) was designed using a 150nm CMOS process on a highly resistive substrate ($> 2k\Omega - cm$), while TJ-Monopix (March 2018) was fabricated using a modified 180nm CMOS process with a $1k\Omega - cm$ epi-layer. The sensors differ on their front-end design, biasing scheme, pixel pitch, dimensions of the collecting electrode relative to the pixel size and the placement of read-out electronics within such electrode. The size of the pixel matrices is in the order of the current ATLAS Inner Detector chip (FE-I3) and their digital logic is able to cope with the projected hit rates in the out-most layers of the ITk.

Both chips were operational after thinning down to $100\mu m$ and backside processing for total bulk depletion in the case of LF-Monopix. Our results include measurements of their leakage current,

gain, noise, threshold dispersions, timing, response to radioactive sources and efficiency in test beam campaigns. Moreover, we discuss the promising outcomes from the measurements after irradiation with protons up to a dose of 50Mrad and neutrons up to $1 \times 10^{15} n_{eq}/\text{cm}^2$.

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Development of CMOS pixel sensor prototypes for the CEPC vertex detector

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The Circular Electron Positron Collider (CEPC) is proposed as a Higgs factory, targeting a high precision study of the properties of the Higgs boson. To achieve the required sensitivity of experiment, the CEPC vertex detector should provide unprecedented position resolution with very low material budget, and low power consumption. CMOS Pixel Sensors (CPS), as one of the promising candidate technologies, has been studied within the R&D activities for the CEPC vertex detector. This talk introduces the development of CPS prototypes in a 180 nm CMOS Image Sensor process. We will present the detailed design of three prototypes: JadePix1, JadePix2 and MIC4. The JadePix1 consists of 36 pixel sub-matrices, each one containing several versions of analog pixel design. The JadePix2 and MIC4 chips both feature digital pixels and differ essentially by their different readout schemes. The JadePix2 employs the rolling shutter readout approach, which allows for small pixels ($22 \times 22 \mu\text{m}^2$). The MIC4 is based on a data-driven readout architecture, and is particularly suited to the ambitioned readout speed and power consumption. The chip characterizations of JadePix2 and MIC4 will be also reported.

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Performance of the ATLASPix1 pixel sensor prototype in ams aH18 CMOS technology for the ATLAS ITk upgrade

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Monolithic active pixel sensors (MAPS) based on commercial high-voltage CMOS processes are an exciting technology that is considered as an option for the ATLAS inner tracker upgrade. Here, particles are detected using deep n-wells on a p-type substrate as sensor diodes with the depleted region extending into the silicon bulk. With readout electronics and sensor integrated on the same device, the detector complexity and the material budget are greatly reduced. The ATLASPix1 pixel sensor prototype is a large-scale pre-production monolithic prototype that implements the full readout chain on a single physical chip. It is based on a large sensor electrode and is produced using the ams aH18 high voltage technology. Three pixel matrices with different readout architectures, triggered and untriggered, and pixel designs are implemented. We will show a systematic performance evaluation of this prototype for unirradiated and irradiated samples of up to $10^{15} n_{eq}/cm^2$, discuss its applicability as an option for the ATLAS inner tracker upgrade, and outline the future plans.

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Characterization of the prototype CMOS pixel sensor JadePix-1 for the CEPC vertex detector

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The proposed Circular Electron Positron Collider (CEPC) will allow measurement of the Higgs properties with precision beyond the (HL-)LHC. To meet the stringent physics requirements, its vertex detector will have to be constructed with the state-of-the-art pixel detector technologies that promise high spatial resolution, low power consumption and low material budget. We have conducted R&D based on the emerging CMOS pixel sensor technology and developed the first prototype JadePix-1. In this talk, we will describe the sensor structures that are primarily designed to verify the impacts of diode geometry on charge collection. We will present the detailed test results obtained with radioactive sources and electron test beams, and the sensor performance before and after neutron irradiation up to 10^{13} 1 MeV n_{eq}/cm^2 .

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Performance of the large scale HV-CMOS pixel sensor MuPix8

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The Mu3e experiment is searching for the charged lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$, aiming for an ultimate sensitivity of one in 10^{16} decays. In an environment of up to 10^9 muon decays per second the detector needs to provide precise vertex, time and momentum information to suppress background. The detector consists of cylindrical layers of 50 μm thin High Voltage Monolithic Active Pixel Sensors(HV-MAPS) placed in a 1 T magnetic field, which allow a precise vertex and momentum reconstruction. Additional layers of fast scintillating fibre and tile detectors are providing sub-nanosecond time resolution.

The MuPix8 chip is the first large scale prototype, proving the scalability of the technology. It was produced in the AMS aH18 180 nm HV-CMOS process. It consists of three sub-matrices, each providing an untriggered datastream with more than 10 MHits/s. The latest results from laboratory and testbeam characterisation will be presented, showing an excellent performance with efficiencies $> 99.6\%$ and a time resolution better than 10 ns achieved with time walk correction. Further, first results from the new prototype MuPix9 will be highlighted and the R&D roadmap towards the final Mu3e chip will be shown.

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Enhanced Lateral Drift Sensors: charge sharing and resolution studies

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Future experiments in particle physics foresee few-micrometer single-point position resolution in their vertex detectors, motivated by e.g. b- and light-quark-tagging capabilities. Silicon is today's material of choice for high-precision detectors and offers a high grade of engineering possibilities. Instead of scaling down pitch sizes, which comes at a high price for an increased number of channels, our new sensor concept seeks to improve the position resolution by increasing the lateral size of the charge distribution already during the drift in the sensor material. To this end, it is necessary to carefully engineer the electric field in the bulk of this so-called enhanced lateral drift (ELAD)

sensor. This is achieved by implants deep inside the bulk which influence the charge carriers' drift paths.

In order to find an optimal sensor design, detailed simulation studies were conducted using SYNOPSIS TCAD. The geometry of the implants, their doping concentration and the position inside the sensor were optimised. The electric field simulation shows that the deep p- and n- implants create repulsive and attractive areas inside the bulk of the sensor. Transient simulations with a traversing particle were used to optimise the charge carriers drift path inside the sensor. Finally, to estimate the position resolution of an ELAD sensor, test beam simulations using the AllPix2 software have been performed using the realistic electric field profile from the TCAD simulations.

Results of the geometry optimisation are shown realising an optimal charge sharing and hence position resolution. A position resolution of a few micrometers is expected by using deep implants without relying on a Lorentz drift or tilted incident angle. A description of the multi-layer production process is presented, which represents a new production technique allowing for deep bulk engineering. Finally, an estimate of the position resolution of ELAD sensors is presented based on the simulations with AllPix2.

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Towards MÖNCH 04, a 25µm pitch hybrid pixel detector for the ATHOS low energy beamline at the SwissFEL

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MÖNCH is a hybrid silicon pixel detector based on charge integration and with analog readout, featuring a pixel size of 25x25 µm². The latest working prototype (MÖNCH 03) consists of an array of 400x400 identical pixels for a total active area of 1x1 cm². Its design is optimized for the single photon regime. The chip has an ENC in the order of 35 electrons RMS and a dynamic range of ~4x12 keV photons in high gain mode, which increases to ~100x12 keV photons with the lowest gain setting.

The ATHOS beamline, in construction at present at the Swiss Free Electron Laser (SwissFEL), has a minimum operating energy of 250eV with an extremely high photon flux. The low noise levels of MÖNCH make it a suitable candidate for X-ray detection at energies below 1 keV. However, the architecture implemented in MÖNCH03 does not provide enough dynamic range for applications at the SwissFEL. For this reason a new large area prototype (MÖNCH 04) is being designed, targeting energy sensitivity down to at least 500eV, single photon resolution down to 800eV and a dynamic range of at least 10000 x 800eV photons. At the same time, a collaboration with FBK (Trento, Italy) has been established to develop thin entrance window sensors, needed to reach enough detection efficiency at low photon energies.

The latest characterization results of the previous MÖNCH prototypes will be presented, with special emphasis on the low-energy results, including the behavior of the first detector samples of different flavors produced by FBK. The design of MÖNCH 04 and the proposed solutions to the challenges that it has to address will be shown. Finally, the prospects for the design, optimization and commissioning of the larger area module (4x6 cm²) required by ATHOS will be discussed.

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Pixel array for 3-D integration with an intracortical electrode array

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ABSTRACT

Here we present a Read-Out Integrated Circuit (ROIC) with metalized topside contacts that is bonded to an array of high aspect ratio insulated microwires to form a platform for in vivo, intracortical recording (fig 1) of unprecedented scale.

The ROIC (fig 2) has 256x256 pixels (fig 3) consisting of an AC-coupled sense-amplifier, followed by an anti-aliasing band filter. In designing a CMOS array for such an application, several features are desirable: (1) it has a metalized top-side contacts on each readout array element (pixel) for bonding to an array of microwire probes, (2) it has lower than 10 μ V RMS noise to record action potentials with high fidelity, (3) it is insensitive to slow changes in electrochemical potential between the recording electrodes and reference electrode, (4) the pixel size should be no bigger than the desired inter-wire spacing for the array, (5) it supports full-frame readout beyond 32,000 fps.

Details and measurements results of this device will be shown.

A glimpse of the next generation device, tackling the data bottleneck, may be given.

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New beam test results of 3D pixel detectors constructed with polycrystalline CVD diamond

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Detectors based on Chemical Vapor Deposition (CVD) diamond have been used extensively and successfully in beam conditions/beam loss monitors as the innermost detectors in the highest radiation areas of Large Hadron Collider (LHC) experiments. Over the last two years the RD42 collaboration has constructed a series of 3D pixel detectors using CVD diamond as the active material and laser fabricated columns in the bulk and characterized them in test beams. The electrical properties and latest beam test results from 2017 and 2018 of the efficiency and spatial resolution of the most recent 3D pixel detectors constructed with polycrystalline CVD diamond will be presented and compared. Our results indicate that the 3D geometry with 50 micron x 50 micron cells ganged in a 1x5 or 3x2 arrangement to match the available pixel readout electronics collected, for the first time, more than 90% of the deposited charge in a polycrystalline CVD diamond detector. In addition, the effects on charge collection in polycrystalline CVD 3D diamond pixel devices due to radiation will be discussed.

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Pixel-detector R&D for CLIC

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The physics aims at the proposed future CLIC high-energy linear e+e- collider pose challenging demands on the performance of the detector system. In particular the vertex and tracking detectors have to combine precision measurements with robustness against the expected high rates of beam-induced backgrounds. A spatial resolution of a few microns and a material budget down to 0.2% of a radiation length per vertex-detector layer have to be achieved together with a few nanoseconds time stamping accuracy. These requirements are addressed with innovative technologies in an ambitious detector R&D programme, comprising hardware developments as well as detailed device and Monte Carlo simulations based on TCAD, Geant4 and Allpix-Squared. Various fine pitch hybrid silicon pixel detector technologies are under investigation for the CLIC vertex detector. The CLICpix and CLICpix2 readout ASICs with 25 micron pixel pitch have been produced in a 65 nm commercial CMOS process and bump-bonded to planar active edge sensors as well as capacitively coupled to High-Voltage (HV) CMOS sensors. Monolithic silicon tracking detectors are foreseen for the large surface (~140 square meters) CLIC tracker. Fully monolithic prototypes are currently under development in High-Resistivity (HR) CMOS, HV-CMOS and Silicon on Insulator (SOI) technologies. The laboratory and beam tests of all recent prototypes profit from the development of the CaRIBou universal readout system. This talk presents an overview of the CLIC pixel-detector R&D programme, focussing on recent test-beam and simulation results.

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The LHCb VELO Upgrade II (2031)

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LHCb has recently submitted a physics case for a an Upgrade II detector to begin operation in 2031. It will follow the Upgrade I which is currently under construction and will run from 2021 onwards. It is designed to run at instantaneous luminosities of $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, an order of magnitude above Upgrade I, and accumulate a sample of more than 300 fb^{-1} . At this intensity, the mean number of visible proton- proton interactions per crossing would be 56, producing around 2500 charged particles within the LHCb acceptance. Efficient real-time reconstruction of charged particles and interaction vertices within this environment represents a significant challenge. To meet this challenge it is foreseen to modify the existing spectrometer components to increase the granularity, reduce the amount of material in the detector and to exploit the use of precision timing.

In particular, the LHCb upgrade physics programme is reliant on an efficient and precise vertex detector (VELO). This subdetector enables real time reconstruction of tracks from all LHC bunch crossings in the software trigger system. The Upgrade II luminosity poses significant challenges which necessitate the construction of a new VELO with enhanced capabilities. Compared to Upgrade I there will be a further order of magnitude increase in data output rates accompanied by corresponding increases in radiation levels and occupancies. To cope with the large increase in pile-up, new techniques to assign correctly each b hadron to the primary vertex from which it originates, and to address the challenge of real time pattern recognition, are needed. These challenges will be met by the development of a new 4D hybrid pixel detector with enhanced rate and timing capabilities in the ASIC and sensor. Improvements in the mechanical design of the Upgrade II VELO will also be needed to allow for periodic module replacement. The design will be further optimised to minimise the material before the first measured point on a track (which is dominated by the RF foil) and to achieve a more fully integrated module design with thinned sensors and ASICs combined with a

lightweight cooling solution. As well as improving the VELO performance, quantified by the impact parameter resolution, these changes will also be beneficial both in improving the momentum resolution of the spectrometer and reducing the impact of secondary interactions on the downstream detectors.

It is envisaged that the readout ASIC will follow the VeloPix/Timepix4 development path and will be designed in 65 nm. A novel design will include in-pixel timing and calibration, allowing the pixel time stamps to reach a precision of 20 ps, and a new custom output serialiser will be included. The R&D programme will explore the capabilities of combining fast timing information with small pixel size, and examine clock distribution issues for fine timing over a full system. The capabilities of the sensor to deliver fast timing will be explored for different sensor designs.

The needs of the Upgrade II VELO will be outlined, along with the R&D steps envisaged to achieve the goal of a 4D pixel tracker.

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Results of larger structures prototyping for the Phase-II upgrade of the pixel detector of the ATLAS experiment

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The current inner tracker of the ATLAS experiment is foreseen to be replaced at the High Luminosity era of the LHC to cope with the occurring increase in occupancy, bandwidth and radiation damage. It will be replaced by an all-silicon system, the Inner Tracker (ITk). This new tracker will have both silicon pixel and silicon strip sub-systems aiming to provide tracking coverage up to $|\eta| < 4$. For a high tracking performance are radiation hard and high-rate capable silicon sensors and readout electronics important. Moreover, services and stable, low mass mechanical structures are essential and give challenges to the system design.

Currently a large prototyping programme is ongoing within the ITk pixel detector community. Components for larger structures with multiple modules based on the FE-i4 front-end chips were produced and are in assembly and evaluation.

By this the system integration and design is prototyped and validated.

In the presentation, the latest evaluation and results of thermo-mechanical prototypes and fully electrical prototypes are presented. Important system relevant aspects and their application will be discussed.

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Development of a readout system for the pixel detector at HIRFL-CSR Internal Target Facility

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The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, inter-disciplinary science and relative applications. The internal target is built on the experiment ring of the HIRFL-CSR for high precision measurements.

Due to the high spatial resolution, a Monolithic Active Pixel Sensor (MAPS) based pixel detector is expected to be a good candidate for the related experiments. In this paper, a versatile radiation-hard readout system has been designed for the tentative MAPS based pixel detector in HIRFL-CSR Internal Target Facility. The readout system consists of the front-end cards and the data aggregator. The front-end card reads data from the customized detector pads, where the MAPS is hosted, processes the data and sends it to the data aggregator through high speed serial link. In addition, the front-end card also provides clocks, power, configurable parameters, debug interface, etc. to the detector pads. To reduce the risk of radiation-induced failures, the Flash-based Microsemi Smartfusion2 FPGA has been chosen as the main FPGA on the front-end card. This FPGA was chosen due to its inherently single event effects tolerant configuration cells. The data aggregator receives data from the front-end cards and ships the data to the data computer through PCIe interface. This paper will present the design, implementation and first test results of this readout system.

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Large pixel SiPMs for single photon detection in the new LHCb large area scintillating fibre tracker

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During the long shutdown of LHC (2019/2020), the complete LHCb tracking system will be replaced to cope with the increased luminosity and trigger less read-out scheme. A large area (300m²) scintillating fibre tracker (SciFi) with more than 500K channels and 250µm readout pitch is under construction. The silicon photomultiplier technology employed for the read-out provides high photon detection efficiency, low correlated noise (optical cross-talk and after-pulse), short recovery time and withstands the foreseen neutron fluence. The Hamamatsu photo-detectors selected have been characterised before and after irradiation with neutrons and protons. We will focus on the study of the performance of these devices in the context of the LHCb SciFi application regarding the single photon detection capability after irradiation. New developed characterisation methods will also be presented.

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Feasibility of PET Detector Readout by High-Density Silicon Photomultipliers with Epitaxial Quenching Resistors

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Silicon photomultipliers (SiPMs), also known as multi-pixel photon counters (MPPCs), represent an alternative solution that to a large extent combines the advantages of PMTs and APDs. They have high gain, low bias voltage, excellent timing properties and are insensitive to magnetic fields. SiPMs perhaps are the best readout choice for advanced positron emission tomography (PET) systems, such as PET/MRI instruments and time-of-flight (TOF) PET imaging. The most popular SiPM technology that is commercially provided by SensL, Hamamatsu and FBK etc., employs poly-silicon or metal quenching resistors at the device surface, and achieved energy resolution about 9% and coincidence time resolution around 120ps.

Unlike most commercial SiPMs, NDL SiPM uses the bulk resistors in the epitaxial layer as quenching resistor (EQR SiPM); it features small micro cells with high fill factor, fast response to even a single photon, and simple fabrication technology. In this conference, we report NDL EQR-SiPM as a candidate for PET detector readout. For detailed characterization of EQR SiPM based PET detectors, an architecture measuring 511keV gamma photons irradiated from a 18F-FDG source was set up, in which two EQR SiPMs are optically coupled to a pair of lutetium oxy-orthosilicate (LYSO) crystals, the outputted signals are fed to a digital oscilloscope to analyze energy information and perform coincidence processing. The EQR SiPM has active area of 3mm×3mm, comprising 90000 individual cells, a dark count rate of 6.3 MHz at 9 V overvoltage, a peak PDE of 34% for 420 nm photons and an intrinsic single photon timing resolution (SPTR) of 81 ps at the same voltage. The energy resolution (ER) of ~10.1 % and the coincidence timing resolution (CTR) of ~195 ps (FWHM) were obtained with the 2.84mm×2.84mm×6mm LYSO crystals. Saturation effects involved in most commercial SiPM with limited micro cells is negligible. Those results verify that EQR-SiPM is promising in applications of PET imaging.

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High dynamic range CdTe mixed-mode pixel array detector (MM-PAD) for kilohertz imaging

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An x-ray imaging mixed-mode pixel array detector (MM-PAD) coupled to a 750 μm thick CdTe sensor is described. The detector comprises a 2×3 tiled array of individual 128×128 pixel ASICs coupled at the pixel level to CdTe sensor. The CdTe sensor significantly improves the detection efficiency for high-energy x-rays when compared to silicon sensors. The detector is capable of continuous framing at 1 kHz and in-pixel mixed-mode circuitry allows for single image well-depths of greater than 4×10^6 80 keV x-rays. The charge integrating front-end allows for quantitative measurement of high flux x-ray images beyond the capabilities of photon counting detectors. Detector performance will be summarized and measurements from the Advanced Photon Source (Argonne National Lab, Lemont, Illinois, USA) will be presented.

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