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Single-Event-Hardened Timing Generator for Waveform Digitizer based readout electronics

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Analog waveform sampler, the soul of radiation detectors performing a multitude of functions has to evade Single-Event Transients (SETs) in its timing reference. The propagation of transients from the timing generator to the analog memory causes timing non-linearity due to variation in the inverter delay responsible for the sampling speed leading to catastrophic failure of the waveform sampler. The TG using Mixed-Signal Delay-Lock Loop (MSDLL) implements the triple combination of body-feed technique allowing rail-to-rail operation for delay control, the pseudo differential structure regulating duty cycle reducing the jitter impacts optimizing the linear operating range of the Voltage Controlled Delay Line (VCDL) and the MSDLL embedded with dual-edge synchronization enhances the mitigation of Single-Event Upsets (SEUs). The simulation results at the circuit level using 180 nm and 90 nm CMOS PDKs show a 28% increase in the linear operating range and bettering jitter performance of the MSDLL. Furthermore, there is only negligible variance in the INL and DNL between the irradiated and non-irradiated values for reference clock of 500 MHz to 1 GHz and the resolution is between 16 to 25 ps with jitter of 10 ps.
The proposed TG circuit have exhibited performance benefits by mitigating the missing pulses and arresting the propagation of SEUs, there is a negligible difference of around 0.1 % between the irradiated and non-irradiated amplitude and timing non-linearity values of analog memory. The proposed analog memory achieves time resolution about 50 ps and is more SET tolerant.

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