This work presents development of special class of Monolithic Active Pixel Sensor (MAPS) which is fabricated in Silicon On Insulator (SOI) CMOS technology. Target applications of the sensor are cosmic dosimetry and radiation imaging. The deep submicron SOI CMOS technology has long been used in many special applications, such as radiation-hardened or high-voltage integrated circuits. It is only in recent years that SOI has emerged as a serious contender for low-power high-performance applications. The main feature of the SOI pixel detectors is the sensor location. A sensor element is implemented on handling wafer. The epitaxial layer which contains the front-end electronics is separated from the sensitive part of structure Buried-Oxide (BOX). This technology has a huge advantage in separating the front-end electronics from the sensor part while maintaining both at the same chip, as shown in Fig. 1 [1,2].

The LORDS was developed with the Center of Applied Physics and Advanced Detection Systems (CAPADS) at the FNSPE CTU in Prague whose main task is development a new type of cosmic dosimeter and X-ray imaging detector using a 180 nm deep submicron Silicon On Insulator CMOS commercial technology and its layout is shown in Fig. 2. LORDS is a special class of Monolithic Active Pixel Sensor.

The basic parameters of the LORDS are following:
- Pixel size: 50 x 50 μm², array of 32x64 pixels
- The detector operates in the ADC mode
- Read-out mode: CMOS (= 50 Mhz)/LVDS (= 500 Mhz)
- Detection threshold from 2400 e⁻
- Octagonal sensor design, Fig. 8
- Sensor bias voltage: - 150 V @ depleted region ≈ 40 μm
- Substrates for analog and digital blocks are separated!

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The Overall architecture of LORDS, Figure 3. The largest part of the sensor area is occupied by the pixel matrix which is sensitive to radiation and holds the analog information about the signal amplitude. The pixel matrix is read out row by row. In ADC mode, the memorized pixel peak voltages by Peak Detector Hold (PDH) are transferred to the 64 Analog to Digital Converters (ADC) and digitized. The digitized data are then transferred to the shift register and transmitted outside the chip by communication LVDS or CMOS.

ADC parameters:
- Resolution: 10 bit
- Speed: 250 kS/s
- Power: 150 μW
- Area: 57.5x482 μm²
- Vref: 1024 mV

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REFERENCES
1. T. Benka et al., Characterization of pixel sensor designed in 180 nm SOI CMOS technology, 2018 JINST 13 C01025
2. M. Havranek et al., MAPS sensor for radiation imaging designed in 180 nm SOI CMOS technology, 2018 JINST 13 C06004

Fig. 1: Cross section of the 180 nm SOI CMOS technology
Fig. 2: LORDS layout
Fig. 3: LORDS block schematic
Fig. 4: Standard sensor design
Fig. 5: Octagonal sensor design
Fig. 6: Top - 10 bit ADC linearity
Fig. 7: 10 bit ADC Layout
Fig. 8: Octagonal sensor design, Fig. 9: Pixel characterization, top - output from CSA, middle - output from PDH with row selector, bottom - 10 bit ADC with DAC output
Fig. 10: LORDS test diagram of the differential signal at 1 Gbps (simulation)

LORDS architecture

Results

AKNOWLEDGMENTS

Lords architecture

Lighweight Orbital Radiation Detection System (LORDS)