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A 110nm CMOS process for fully-depleted pixel sensors

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Fully depleted pixel sensors with a thickness ranging from the 10s to the 100s of micrometers find many applications in X-ray, particle and near infrared imaging. Unlike the mature technologies used to fabricate visible-light image sensors, that rely on a few micrometers of active silicon, the fabrication of fully-depleted image sensors on thick silicon substrates still poses several technological challenges. Deep-submicron CMOS processes need to be made compliant with the high-resistivity substrates used as active sensing layers, and a high bias voltage needs to be applied to obtain a full depletion of the sensor. In most applications, a low-capacitance sensing node is also desirable for low-noise charge readout and a low-voltage digital electronics should be implemented on-chip to ensure low-power digital functions.

In this talk, a 110nm CMOS process on high-resistivity substrate tailored for the realization of fully-depleted pixel sensors is presented. Double-sided processing is used to define the backside electrode and the termination structures needed to bias the sensors at high voltage. A set of dedicated test structures for the assessment of the process was designed together with a 24×24 pixels array with $50 \mu m$ pitch.

A first run showing the feasibility of $300 \mu m$-thick fully-depleted sensors was completed. The main technological challenges and the customization of the process will be discussed. TCAD simulation results and electrical measurements on dedicated test structures will be presented together with a characterization of the pixel sensor prototype.

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