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Developments towards a Serial Powering scheme in a monolithic CMOS technology for the ATLAS pixel upgrade

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CMOS monolithic pixel detector technology is one of the options considered for the outer layer of an upgraded ATLAS pixel detector in 2026. A Serial Powering scheme is foreseen for the new inner tracking detector for the Phase-II upgrade of the ATLAS experiment. The modules will be placed in series and powered on by a constant current source to reduce material budget and power losses. At the module level, shunt regulators are used to generate local supply voltage of 1.8 V to polarize the electronics from the input current. In contrast to hybrid pixels, the bias for monolithic sensors is sometimes limited and not sufficiently large to allow a common bias for all sensors in the serial powering chain. In order to meet the requirements of the ATLAS ITk outer pixel layers, new developments have been made in Shunt-LDO regulator and sensor biasing which are designed in modified TowerJazz 0.18 µm CMOS imaging technology. The Shunt-LDO regulator is capable of generating constant voltage of 1.8 V with a minimum drop out voltage of 200 mV and a maximum input current of 1.4 A. Moreover, a charge pump circuit was designed to provide the sensor bias. Two prototype variants were designed with 6-stages and 19-stages to provide negative bias down to -6 V and -20 V, respectively. Shunt-LDO regulator and charge pump test chips were submitted this summer. In this poster, a description of Serial Powering with CMOS sensor specificities will be shown.

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