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A 14-Gbps/ch VCSEL Array Driving ASIC in 65 nm CMOS for High-Energy Physics Experiments

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850nm VCSEL array light source combined with multi-mode fibers has been prevailingly employed in the commercial short-range data transmission scenarios with the advantages of relatively easy driven, low cost, high density and reasonably high bandwidth. Besides, the natural radiation-tolerant feature of the GaAs-based VCSEL also makes this combination very competitive in the high-energy physics readout applications. As a continuous study on the radiation-tolerant custom array optical module development and VCSEL driver design, here we report the design and test results of a 4 x 14 Gbps/ch VCSEL array driver ASIC implemented in 65m CMOS technology. Each channel of the driver receives 200 mVp-p differential CML signals, and outputs a 2 mA bias current and a 5 mA modulation current at 14 Gbps/ch with the power consumption of 52 mW/ch.

The driver die features a size of 2000 μm × 1230 μm, and the channel height is 250 μm to be compatible with the VCSEL array die. The analog core of each channel consists of a limiting amplifier (LA) and a novel output driving structure. The LA is composed of an equalizer stage and a four-stage pre-driver. The output driver adopts the on-chip AC-coupling and a stacked tail-current source to remove the traditional cascode voltage-drop NMOS to improve the bandwidth. The bandwidth bottleneck of the output driving stage is effectively resolved for the 14-Gbps application without using any complex peaking or pre-emphasis structures.

This driving ASIC has been taped out and fully evaluated after wire-bonded to the four channel VCSEL array and integrated into an array optical transmitter. Widely-open 14 Gbps optical eyes have been captured, and full channel optical test results will be reported in the meeting.

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