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A 5.12 Gbps serial data receiver for active cable for ATLAS Inner Tracker Pixel Detector readout upgrade

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In the ATLAS inner tracker pixel Detector (ITK) upgrade for HI-LHC, the up stream data from the detector has to go through a 5-meter thin cable before it is received by an optical module for optical link to control room. The cable mass is expected to be minimized, which limits the bandwidth of the cable that is much less than the data rate. Due to the high-frequency loss of the cable, the electric signal is seriously degenerated. The significant Inter Symbol Interference (ISI) jitter causes a fully closed eye of the signal which makes it not qualified for optical module input specification. We present a design of a serial data receiver to equalize the signal and retime the data with a recovered clock. The output jitter of the receiver is expected to be below 10 ps when the cable is an American wire gauge (AWG) 34 Twinax cable. The chip has four channels of receivers and each channel consumes power of 75 mW current.

The diagram of one channel receiver is shown in Figure 1. The equalizer is based on a two-stage continuous time linear (CTLE) structure. After the equalizer, the ISI jitter is significantly reduced. The following clock and data recovery (CDR) module recovers the clock signal and retimes the data. The CDR module is modified based on the original design in lpGBT. The ISI jitter of the retimed data signal is minimized. A Current Mode Logic driver is used to drive the retimed data for optical module. Users also can bypass the CDR module for the test purpose.

This chip is expected to be submitted in November 2018. The post-layout simulation of the design will be presented on the meeting.

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