Contribution ID: **14** Type: **POSTER**

The read-out ASIC of Gotthard-II Detector

Monday, 10 December 2018 14:50 (10 minutes)

The European X-ray Free-Electron Laser (XFEL.EU) is operating with bunch trains at a repetition rate of 10 Hz since October 2017. Each train consists of 2700 photon bunches with a temporal separation of 220 ns corresponding to a frame rate of 4.5 MHz. Each photon pulse has a duration less than 100 fs (rms) and contains up to 1012 photons in an energy range between 250 eV and 25 keV. This machine will not only open the way to new scientific opportunities but also sets extreme challenges for the detectors, such as AGIPD, DSSC and LPD.

Gotthard-II is a microstrip detector developed for XFEL.EU. The applications include but are not limited to: energy dispersive experiments at 4.5 MHz frame rate, and veto signal generation. In Gotthard-II a silicon microstrip sensor with a pitch of 50 µm or 25 µm is wire-bonded to the read-out ASICs. Each read-out channel on the ASIC consists of an adaptive gain charge sensitive Pre-Amplifier (PA), followed by Correlated-Double-Sampling (CDS) amplifier, 12-bit 18 MSPS Analog-to-Digital Converter (ADC) and Static Random-Access Memory (SRAM) for storing all 2700 images in an XFEL bunch train.

The charge generated in the sensor is collected and converted into voltage signal by the PA. The CDS amplifier removes the reset noise and converted the single-ended input signal into the fully differential output signal. The analog output signal of the CDS amplifier is digitized by the ADC. Every 4 channels share 1 CDS amplifier and 1 ADC. The digital outputs of the ADC are stored in the SRAM, and will be read out during the breaks of the bunch trains. The final ASIC will have 16 blocks. Each block includes 8 PAs arranged with a pitch of 50 µm, 2 CDS amplifiers, 2 ADCs and 1 SRAM of 112 x 2720 bits.

The implemented ADCs are a type of asynchronous successive approximation register (SAR) ADC. It consists of 2 differential split-capacitor arrays serving as digital-to-analog converter (DAC), a comparator and a control logic circuit. Two DACs alternatively works on sampling the input signal and digitizing the sampled signal during each conversion cycle. The comparator is implemented with a differential amplifier followed by a dynamic latch. The comparator outputs generates the asynchronous clock called READY signal to trigger the following steps during the conversion in order to avoid using a power-hungry high frequency clock. Due to the mismatch of the capacitors in the DAC, the raw outputs of the ADC include missing codes and wide codes, and need to be calibrated.

Several prototype designs of the analogue front-end (PA + CDS) and the ADC have been fabricated in UMC 110nm CMOS technology. The last prototype, which was submitted in November 2017, consists of a full signal chain: 8 front-end channels + 2 ADCs + 1 SRAM and was received in April 2018. The measurement results show that the equivalent number of bit (ENOB) of the ADC is bigger than 10 with a power consumption less than 1 mW at a sampling frequency of 18 MHz. The measured full dynamic range covers 1 –104 12 keV photons. The noise is lower than 1.6 keV. The measured DNL of the ADC is less than ±0.5 LSB and the INL of the ADC is less than ±0.4 LSB after calibrating the 12-bit raw ADC outputs to 10-bit data. The final full scale chip including 128 front-end channels, 32 ADCs and the SRAM to store 2700 images is foreseen to be submitted in November 2018.

Primary author: Dr SHI, Xintian (Paul Scherrer Institute)

Co-authors: ZHANG, Jiaguo (Paul Scherrer Institut); Dr MEZZA, Davide (Paul Scherrer Institut); MOZZANICA, Aldo (PSI - Paul Scherrer Institut); DINAPOLI, Roberto (Paul Scherrer Institut); SCHMITT, Bernd (Paul Scherrer Institut)

Presenter: Dr SHI, Xintian (Paul Scherrer Institute)

Session Classification: Poster section

Track Classification: Front end electronics and readout