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Design and Test of ASIC driver and readout for scientific CCD detectors

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In order to implement the driver and readout functions for several types of scientific CCD detector, decreasing the size of electronics of CCD detector system and reducing the total power dissipation for a large scale mosaic CCD detector system, ASIC driver and readout chip was designed using Global Foundry 180nm BCDlite technology. The CCD driver which is called BCDA (Bias Clock Driver ASIC) provide multi-channel clocks and Bias voltage. The CCD video sampling is called CVRA (CCD Video Readout ASIC). The main referenced CCD detectors are detectors from E2V company. A testing system was developed for ASIC test. In addition to the driver module and the readout and sampling module, the testing board includes a FPGA module to control the ASIC, a USB 2.0 interface to communicate with a host computer and a voltage monitoring module. The CCD controller based on ASICs is tested by a scientific CCD simulation and test system which is used to simulate CCD47-20 and generate the required CCD waveform. Additional power board is used to provide complex power supplies. We have carried out functional test and performance test for driving circuit and readout circuit respectively. The waveform shape of the CLOCKS, including the rise time, the fall time and the switching speed, can fit the readout speed of CCD47-20. The readout circuits have low noise. The ASIC testing system was combined with the software on host computer and the scientific CCD simulation and test system to take a picture of 1500*1032 pixels whose brightness decreases with equal difference from the left to the right.

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