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A Time-to-Digital Converter Based on DLL with High Accuracy Measurement Using 130nm Technology

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Time measurement is the basic measurement requirement in high-energy physics experiment and also one of the two basic measurements in nuclear electronics which are time measurement and energy measurement. Time measurement in nuclear physics and particle physics experiments is mainly for high-precision measurement of short time intervals, and time-to-digital converters are the central components of time measurement. Nowadays, TDC is not only used in high-energy physics experiments, but also widely used in aerospace and medical fields. TDC is an indispensable technology in navigation, space technology, communications, industrial production and electric power.

We uses a 130nm technology to implement a DLL-based TDC with a measurement resolution of 12.5 ps. The whole TDC consists of three levels with different measurement resolutions: a coarse counter with 800 ps resolution, a fine TDC with 100 ps resolution and an ultrafine Vernier-type TDC with 12.5 ps resolution. The whole design uses the DLL-based delay line and Vernier method to get the high measurement accuracy with the least influence of variety of process, temperature, and voltage. This TDC is a time-stamp style.

The TDC design has been fully simulated under different corners. The simulated results show that the delays of delay line are stable with a jitter less than 3 ps. The output codes of three level are all correct. The die is about 1 mm * 2 mm has been taped out for fabrication.

A testing board has been designed including FPGA, power module, high-speed transmission module. When the test system starts working, the power-on sequence of the FPGA is controlled by STM32. Then the clock generator LTC6951 is configured through the FPGA to generate a clock signal and a trigger signal. In order to test different time intervals, the frequency of the trigger signal is adjustable. After receiving the clock signal and HIT signal, the TDC will quantize the time interval of the adjacent HIT pulses and then output the quantized digital signal to the FPGA. The output signal of TDC is divided into two types. One is high-speed differential signals, such as Vernier-TDC-codes, Fine-TDC-codes, low-order Coarse-TDC-codes and output enable signals. The other type is low-speed signals, such as TDC test signals, high-order Coarse-TDC-codes, and so on. The high speed differential signal is a CML level standard that can connect to the FPGA's SerDes after AC coupled. The low-speed signal level standard is LVCMOS1.2, so it needs to be converted to LVCMOS1.8 level standard by SN74AXC and then transmitted to the FPGA. When the test system is working, the FPGA will receive a 23-bit code from the TDC, including 16-bit Coarse-TDC-code, 3-bit Fine-TDC-code, and 4-bit Vernier-TDC-code. Then the FPGA will calculate the time interval between the adjacent HIT pulses. Finally, the FPGA transmits the calculated data to the host computer. And we can calculate the accuracy of TDC by uploading data.

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