Contribution ID: **69**　　　　　　　　　　　　　　　　　　　　　　Type: **POSTER**

Development of a front-end ASIC for CdTe Hybrid Pixel Detector

Monday 10 December 2018 17:10 (10 minutes)

We developed a front-end ASIC for a CdTe pixel detector as a part of a R&D effort toward advanced hard X-ray or gamma-ray imaging devices for applications in a variety of fields such as astronomy, medical research and non-destructive analysis. The ASIC is designed for a hybrid configuration where each CdTe pixel can be vertically bump-bonded to a corresponding pixel circuit. The chip consists of 28-by-28 identical cells of 250um-by-250um in silicon area, and is implemented with TMSC 0.35-um CMOS technology. The signals are acquired either in the peak-hold or sample-hold mode before being fed into a column-parallel A-to-D converter. We tested circuit performance and confirmed that its equivalent noise charge was 40 electrons, its integral non-linearity about 1%, and the power consumption 0.2mW per pixel.

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Session Classification:　Poster section

Track Classification:　Readout ASICs