Monolithic Deep Depletion CMOS Pixel Sensor for Detection of Minimum Ionizing Particles and X-Rays

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Presentation at
Pixel 2018 December 10 – 14, 2018
International Workshop on Semiconductor Pixel Detectors for Particles and Imaging
Outline

- Introduction to Deep Depletion CMOS on High Resistivity Silicon

- Results from 4 devices

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- Summary
Deep Depletion Bulk Process on High Resistivity Si

• CMOS Process on High Resistivity Silicon
  – Technology node: 180nm
  – Wafer material: 8 inch float zone (FZ)
  – Resistivity: $\rho_{\text{Si}} \sim 6.5 \, \text{k}\Omega \times \text{cm}$
  – Conductivity type: N
  – Backside: $P^+$ implant with dedicated electrode
  – Thickness: 50 – 400 micron (application specific)

• Modifications to baseline CMOS process
  – Modified wafer backside to mimic CZ type material
  – Additional implants on front side to create low resistivity region
    • for CMOS circuitry
  – Low dose N implant to form photodiode

• Backside process
  – Thin
  – Etch
  – Implant
  – Anneal

New CMOS Sensor Technology for Radiation Detection in Scientific Applications

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CMOS Process on High Resistivity Silicon

- NMOS Transistors
- PMOS Transistors
- Photo Diode
- 20 µm Pixel
- 50 µm Substrate Thickness
- 3 µm
- 4 µm
- P-type backside implant
- High Resistivity N-Type Silicon Substrate
- Deep Nwell
- Nwell
- Pwell
- Deep Pwell
- Monolithic CMOS Process Equivalent to Fully Depleted CCD

Dr. Name

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Advantage and Challenges of CMOS on high rho N\textsuperscript{−} Si

• Challenges
  – Existing circuit IP only partially compatible
    • Standard CMOS uses P-type substrates
  – Standard PDK’s cannot be fully trusted
    • LVS for new devices must be added
    • DRC for additional layers
    • Antenna rules must be tightened
  – Backside process must be low temperature
    • < 400 C to protect CMOS circuitry on front side
  – For tracking applications very thin = fragile wafers must be handled
  – Limited to 8” wafer size

• Advantages
  – Direct detection of light from UV to ~1064nm, low energy X-rays and MIPs
  – High radiation hardness
  – Novel devices possibilities
    • PIN photodiodes
    • SiPm
    • LGAD
  – Low cost high volume production cost

Monolithic CMOS Sensor Process with Unique Performance Characteristics Complementing Hybrid or CCD

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Cost and Yield Considerations

Cost of $100,000/m² tracking area is achievable with the following assumptions:

- > 75% Yield
- No stitching
- Wafer cost <$2,000 (only achievable using high volume CMOS manufacturing)
TCAD Simulations for High Resistivity Silicon CMOS

Breakdown Voltage for all junctions on front side > 10V
High Speed Detector – 1 ns Response Time

- Response time of vertical PIN diode is < 1 ns
  - Based on Transient TCAD Simulation
- Minimum PIN Capacitance is desirable
  - Maximizes passive gain = eliminates need for charge amplifier
  - Reduces Power Consumption for sensor
- Additional gain achievable with BSI APD
  - TCAD simulations show that existing process is suited for integration of BSI APD

High Rho CMOS Process Offers Integration of Low Noise, High Speed PIN Diode
Backside contacted by copper strip
VDDA/PD2/PD3 3.2 V; 4.1V @PS 100 kOhm; 9 uA
Backside -19.8 V; -26 V @PS 100 kOhm; 62 uA
Sealring and Backside connected
DPW stepped 0 to -20 V
PD1 swept -20 to +45 V

Device thickness 200 µm
PD 1 active area 1 mm x 1mm
Dark current density 0.1 nA /mm² = 10 nA/cm²
Front Side Breakdown Voltage for 15\(\mu\)m Test Key

<table>
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<tr>
<th>Component</th>
<th>Voltage</th>
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<tr>
<td>PD1 Bias</td>
<td>1 V</td>
</tr>
<tr>
<td>PD2/PD3/VDDA</td>
<td>3.3 V</td>
</tr>
<tr>
<td>DPW</td>
<td>5.0 V</td>
</tr>
<tr>
<td>Backside</td>
<td>-20 V (200(\mu)m thick)</td>
</tr>
<tr>
<td></td>
<td>-80 V (400(\mu)m thick)</td>
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QE (\(\lambda=1064\)nm) \(~ 40\%

Devices have no AR coating

High broadband QE from 350nm – 1100nm confirms Full Depletion of Sensors up to 400\(\mu\)m Thickness
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2nd Generation MAPS Sensor

- 4 sensor variations were fabricated
- Sensors have different pixels
  - Electron collection with PMOS: 3x
    - Alternative peripheral substrate isolation
  - Hole collection with NMOS: 1x
- 20 test keys were integrated on the same wafer
  - Independent verification of PD performance
- 4 different wafer thicknesses, \( w_t \)
  - \( w_t = 50 \, \mu m \)
  - \( w_t = 100 \, \mu m \)
  - \( w_t = 200 \, \mu m \)
  - \( w_t = 400 \, \mu m \)
- Dedicated layout for N type silicon
  - Not compatible with standard layout IP
  - Foundry PDK only partially applicable
MAPS Pixel Schematic Version 2: PMOS only

5 terminal isolated PMOS transistor

VDD = 3.3V

DPW < 0.0V

Electron Collecting Photo diode

Monolithic Electron Collecting Pixel with PMOS Readout Circuitry

Vpix

Cint

R_s

Vbias

SN

Vrs

Vr0

out

R_M

R_D

SN

MN

SF

wrt1

C_1

rd_1

wrt2

C_2

rd_2

wrt3

C_3

rd_3

wrt4

C_4

rd_4

V_pix

C_int

V_bck

V_dpp

DPW < 0.0V

VDD = 3.3V
Ceramic Packages For MAPS Devices

Sensor assembly using conventional wire bonds to LCC

Same LCC with open center to minimize material in beam path

Backside of assembled chip (light entrance side)

Test key wire bonded into LGA

Test key flip-chip bonded into LGA

- **Backside contact using conductive epoxy**
  - Backside bias through front contact possible

- **Fabrication of backside contact on-going**
  - Wafers with thicknesses [um]: 50, 100, 200 and 400

Versatile Custom LCC and LGA Package was Developed Together With Matching Sockets

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- SCI’s “master test board” used for various SCI devices
  - Supplies up to 10 bias voltages and up to 10 clocks
  - Up to 24 analog output channels of 16-bit ADCs operating at 30Msamples/sec
- Xilinx-based digital data formatting board with 10 GigE optical fiber output
  - Digital output transmitted via Ethernet at 1-10 Gb/s using industry-standard GigE protocol

Low Noise High Speed Analog Test Environment used for Characterization
Test image taken with 200micron monolithic deep depletion CMOS sensor (after offset subtraction)

Tree rings on 400micron thick monolithic deep depletion CMOS sensor (visible when sensor is biased at ~60V, i.e. less than full depletion; this is normal and does not cause any issues)

Test image taken with 400um thick sensor at 80V backside bias (small ROI only due to damaged backside)

Fixed pattern of high dark current seems to originate on sensor backside

Backside pattern on 400um thick sensor at 80V bias
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Digital Tracking Sensor Specification

- 1024 x 1024 pixels, 20 µm pitch, 25 x 25 mm chip
- High Speed – 50 MHz Frame Rate
- Maximum number of hits per frame: 10
  - 12.5 MHits/cm²/sec
- Low Cost – Monolithic CMOS Process
- High Yield – In Pixel SRAM bit to disable bad pixels
- Low Power: 240 mW/cm²
- Radiation Hard
- In Pixel 1-Bit A/D Converter
- Enabling Technology – High Resistivity Substrates With Quadruple Well Process
- Funding: U.S. Department of Energy DE-SC0013683

New Digital Tracking Sensor Advances State of The Art MAPS Performance While Reducing Fabrication Cost
Orthopix architecture is a fast compression scheme

However, it is sensitive to “hot” pixels

Without any mitigation, 8 “hot” pixels would kill a sensor

Our mitigation scheme is to include an SRAM bit in each pixel to allow for individual pixel disabling
Schematic for Digital Orthopix Pixel

- 1bit SRAM cell
  - SRAM cell is individually programmable for each pixel
- Pixel array power consumption estimated at 1.0 W
  - 240 mW per cm²
  - Charge amplifier determines power consumption in pixel
- Monolithic pixel with extensive complimentary circuitry

**Improved Orthopix Design Overcomes Fatal Yield Impact of Hot Pixels**
Layout of Digital Sensor For Particle Tracking

- 25 x 25 mm$^2$ overall size
- 1024 x 1024 pixels
- 20 µm pixel size
- Four-fold symmetric
- All available 6 metal layers used for power routing
  - Some shared with signal routing
Block Diagram for Digital Orthopix Tracker

- Readout for each projection is the same
  - Identical Layouts
- Clock skew control simplified
- Homogeneous power distribution
- Decongested layout
  - Minimal cross coupling and loading of signal lines
  - Low impedance power planes
- Efficient clock tree implementation
- Simplifies packaging and test electronics

Four-fold symmetry simplifies design effort
Multiple Sensors Fabricated within Internal MPW

All use the same process

1k x 1k tracking sensor

64x64 pixel active sensor

64x64 pixel passive sensor

10 standard test structures with various pixel pitches of 12, 15, 20, 25, 50, 100 um for C/V, I/V and QE characterization

Affordable Prototype Development due to MPW mask sharing

MPW – Multi Project Wafer
Wafer Pictures of Orthopix and HDR X-Ray sensor

8” high resistivity Float Zone (FZ) wafer with monolithically integrated 180nm CMOS circuitry

Sensor Material is available to December 10, 2018
Status

- Wafer front- and backside fabrication completed
  - Backside passivation insufficient
- Electrical verification of Circuitry is on-going
- Backside passivation process must be improved for Orthopix architecture to work properly
  - Yield of backside process must be improved
  - Goal: >99% functioning pixels
- Additional backside process steps have been added to improve yield

Availability of Orthopix Wafers with Improved Backside Process
Q1/2019

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HDR X-Ray Sensor

- 64 x 64 pixels, 50 µm pitch, 25 x 25 mm chip
- Frame rate: 1000Hz
- Dual gain readout
  - Charge transfer to high gain node (center)
  - Overflow to low gain node (donut contact)

**Two separate gain regions extend dynamic Range**
HDR X-Ray Sensor Schematic

Pixel has NMOS and PMOS Transistors with Donut Shaped $tg_1$ and $tg_2$ Gates
High Dynamic Range Pixel – TCAD Simulations

Circular geometry
FD in the middle
OV outside

Net doping concentration underneath collection regions

correct operation of transfer gate

Incomplete closing of transfer gate (deep channel)
High Dynamic Range Pixel Floorplan

- Vertical Scanner
- 64 x 64 active pixel array
- Serial interface I/O circuitry
- Timing control logic supporting 3 different operating modes
  - Single read
  - CDS
  - Pulsed CDS
- Bias generator
- Output pads
  - high density pad arrangement possible because entrance is on backside

Sensor requires 4 clock signal, Serial Interface programming and Power
Photo Currents Can be Directed by Gates

- Measurements on test keys
  - 36x36 HDR pixels, shorted together to increase signal
- Area 3.24 mm²
- 36 x 36 HDR pixels in parallel
- Halogen bulb light source
- Monochromator followed by integrating sphere

HDR Pixel is Fully Functional
First Images from HDR CMOS Sensor – 200μm Thickness

- Top Row
  - Low gain readout node
- Bottom Row
  - High gain readout node

Office illumination
- Backside Bias Voltage: -20V
- Artifacts originate on backside

HDR Sensor Shows Similar Artifacts as 640x512 Imager
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LGAD – Test Key Measurement

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<th>15 µm pixel areas</th>
<th>Size x [number of pixels]</th>
<th>Size y [number of pixels]</th>
<th>Area [mm²]</th>
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<tbody>
<tr>
<td>PD₁</td>
<td>66</td>
<td>66</td>
<td>0.98</td>
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<tr>
<td>PD₂</td>
<td>13</td>
<td>92</td>
<td>0.924</td>
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LGAD – Cross Section of Dopant Distribution

- N-type implant is surrounded by p-type implants
- P barrier below N photodiode
- Detail of the front and the back are shown below

Pixel

Front side

Back side

n-type implant

p-type implant

Backside p-type implant
• The -5 V backside voltage depletes the structure
• The gain region (impact ionization rate) is immediately below the n-type implant
TCAD I/V Curves for LGAD Test Keys

- Reverse bias I/V curve shows avalanche gain starting at ~36 V
- Gain increases to 13x at 36.6 V
  - At 35 V current is $6 \times 10^{-14}$ A/um
  - At 36.6 V current is $2.3 \times 10^{-12}$ A/um
- Gain increases to $>10^6$ at 36.7 V
  - At 36.7 V bias current is $4.6 \times 10^{-6}$ A/um
Measured LGAD Responsivity Test Results

Standard photo diode gain concentrated in 500 nm region

Quantum Efficiency vs. Wavelength

- PD 1 QE (%) 1 V Bias
- Ref Diode S1337-33BQ QE

LGAD photo gain constant throughout visible spectrum

Quantum Efficiency vs. Wavelength

- PD 1 QE (%) 8 V Bias and 4 V PISO
- PD QE (%) 1 Hamamatsu S1337-33BQ

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Summary

• First monolithic imagers with electron collecting photodiodes and PMOS readout circuitry has been presented
  – Pitch: 15micron

• Monolithic high frame rate tracking sensor has been designed
  – Pitch: 20micron
  – Integration of extensive complimentary circuitry inside pixel
  – Functionality currently limited by low yield of backside process

• High Dynamic Range Sensor for direct low energy X-ray detection could successfully be demonstrated
  – Pitch: 50 micron
  – PMOS and NMOS transistor inside unit cell

• Demonstration of avalanche gain in monolithic CMOS LGADs
  – Broadband amplification > 1x0 from 400nm – 1064nm was measured

High rho silicon CMOS process is available to external research groups for evaluation and prototyping
Thank You for your attention!

Sensor Creations
• **n**: number of projections
• **N**: sensor resolution [number of pixels]
• Frame rate of 50MHz and a cluster multiplicity of 4 pixels
• Sensor resolution of **N=1024** pixels in X- and Y-direction
• Number of projections: 4
• At hit rate of 340 MHz/cm$^2$ reconstruction efficiency is 99.9%
  • Full 1k x 1k array can only support up to 119 MHz/cm$^2$.
• Hot pixels look like hit pixels

**Improved Orthopix Design Overcomes Fatal Yield Impact of Hot Pixels**
PS Demo Chip

- All metal layers partially used for power routing
- The diagonal projections are routed on M4 and M5
- Vertical and horizontal projections are routed on M3 and M6