Development of fast, monolithic silicon pixel sensors in a SiGe Bi-CMOS process.

Speaker:
Lorenzo Paolozzi

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Our research

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- **Milestone 1 (this talk)**:

➡ A monolithic pixel detector with **100 ps** time resolution for MIPs and **large pixel size** to be used for TOF-PET applications.

- **Milestone 2:**

➡ A monolithic pixel detector with **sub-100 ps** time resolution for MIPs and **small pixel size** to be used for high-energy and applied physics research.

Technology choice

Time resolution of silicon pixel detectors

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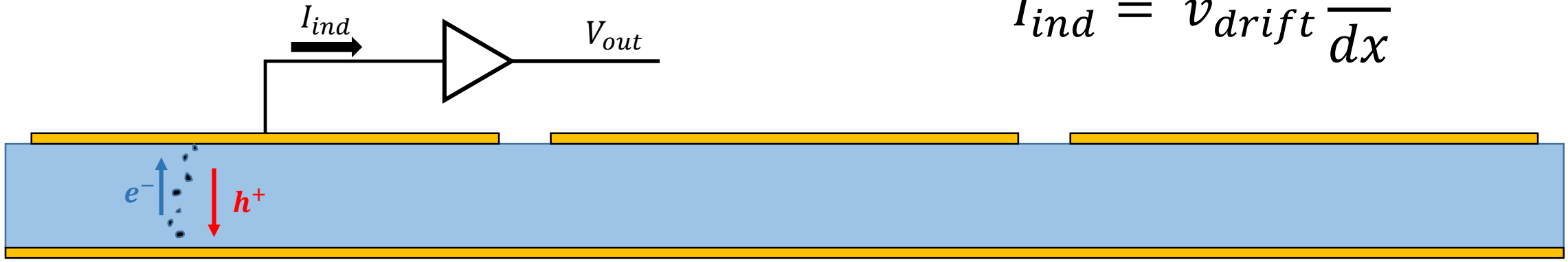
The three main parameters that determine the time resolution of semiconductor detectors:

- Read out geometry (constraint)
- Electronics noise (optimization)
- Charge collection noise (limit)

$$I_{ind} = \sum_i q_i \, \vec{v}_{drift,i} \cdot \vec{E}_{w,i}$$

$$I_{ind} = v_{drift} \frac{dq}{dx}$$



Electronic noise

Detector time resolution depends mostly on the amplifier performance!

$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{Rise\ Time}{Q/_{ENC}}$$

Need a **fast, low-noise, low power consumption** electronics.

The fast, low noise amplifier

Dominating term:
series noise ($\tau < 10\ ns$)

$$ENC^2 \propto \left(2q_e I_C + \frac{4kT}{R_P} + i_{na}^2\right) \cdot \tau + \boxed{(4kTR_S + e_{na}^2) \cdot \frac{C_{in}^2}{\tau}} + 4A_f C_{in}^2$$

Fast BJT integrator

$$ENC_{series\ noise} \propto \sqrt{2kT\langle SNI\rangle \left[(C_{in})^2 \frac{h_{ie}}{\beta} + R_{bb} C_{in}^2\right]}$$

Maximize the current gain (at high frequencies!) while keeping a low base resistance

SiGe technology for low noise, fast amplifiers

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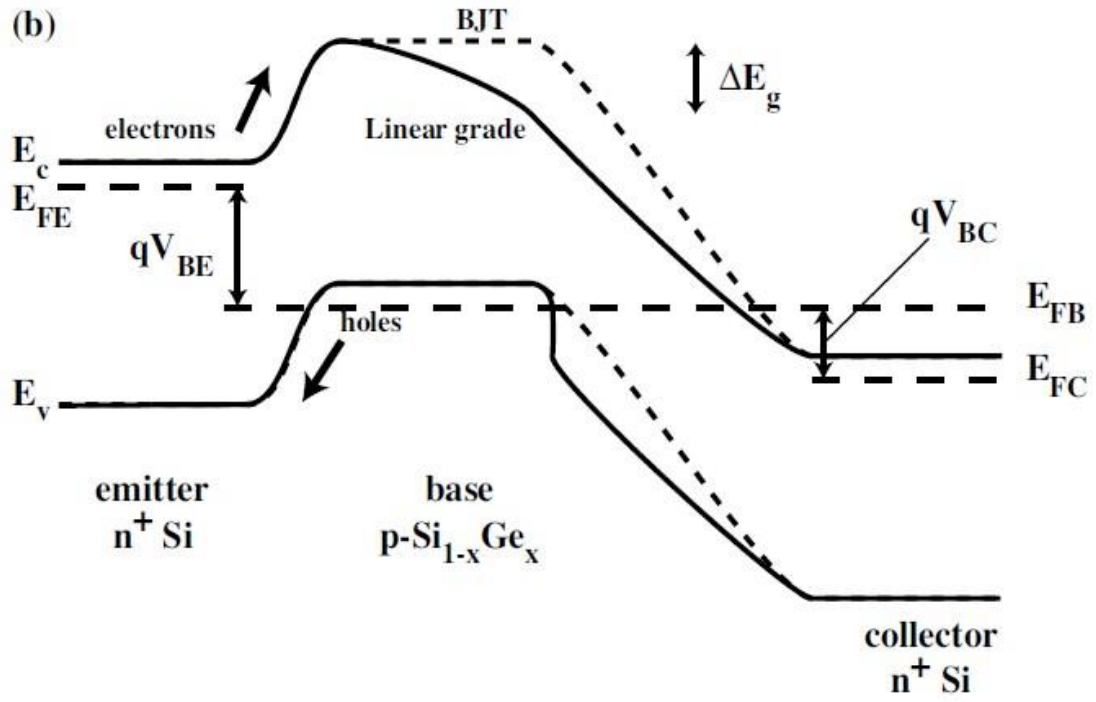
A possible approach: **changing the charge transport mechanisms** in the base from diffusion to drift.



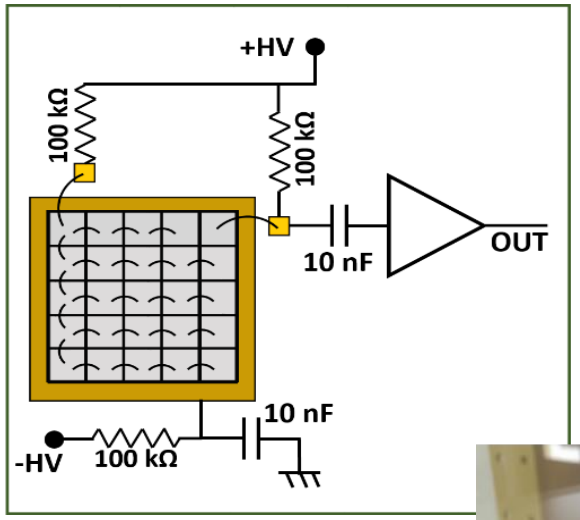
Our choice:

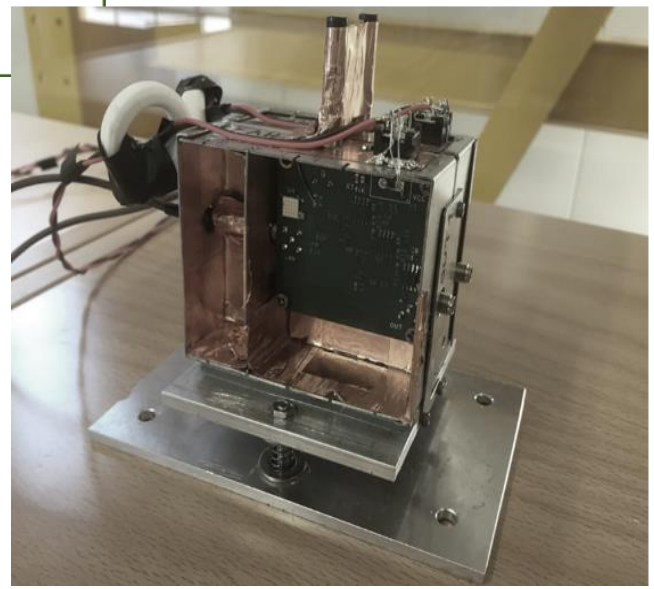
SiGe HBT from IHP microelectronics

$\beta = 900$

$f_t = 250\ GHz$

Proof of principle





November 2015:

Hybrid sensor with **SiGe** discrete component amplifier

- Large pads.
- 100 µm thick substrate.

Beam test with MIPs:

- **Time resolution: 106±1 ps.**
- **Power consumption: 1400 mW/cm^2**

For more information:
M. Benoit et al 2016 JINST 11 P03011
doi: https://doi.org/10.1088/1748-0221/11/03/P03011

ASIC development

SiGe monolithic ASIC for TOF-PET

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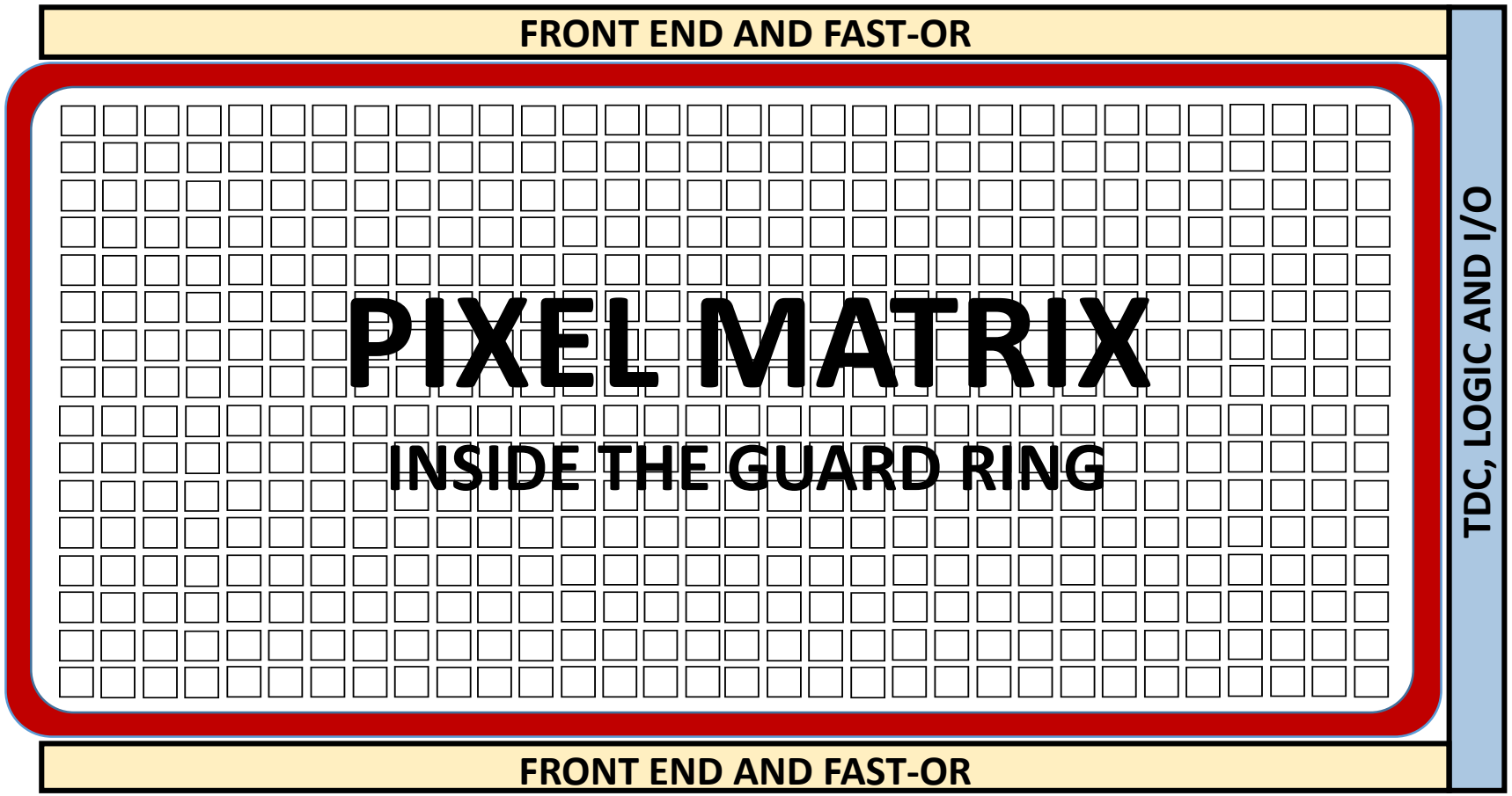
Technology	IHP SG13S
ASIC length	$24\ mm$
ASIC width	$7, 9, 11\ mm$
Pixel Size	$500 \times 500\ \mu m^2$
Pixel Capacitance (comprised routing)	$\mathbf{750\ fF}$
Preamplifier power consumption	$\mathbf{< 80\ mW/cm^2}$
Preamplifier E.N.C.	$600\ e^-\ RMS$
Preamplifier Rise time (10% - 90%)	$800\ ps$
Time resolution for MIPs	$\mathbf{100\ ps\ RMS}$
TDC time binning	$20\ ps$
TDC power consumption	$\sim 0.1\ mW/ch$

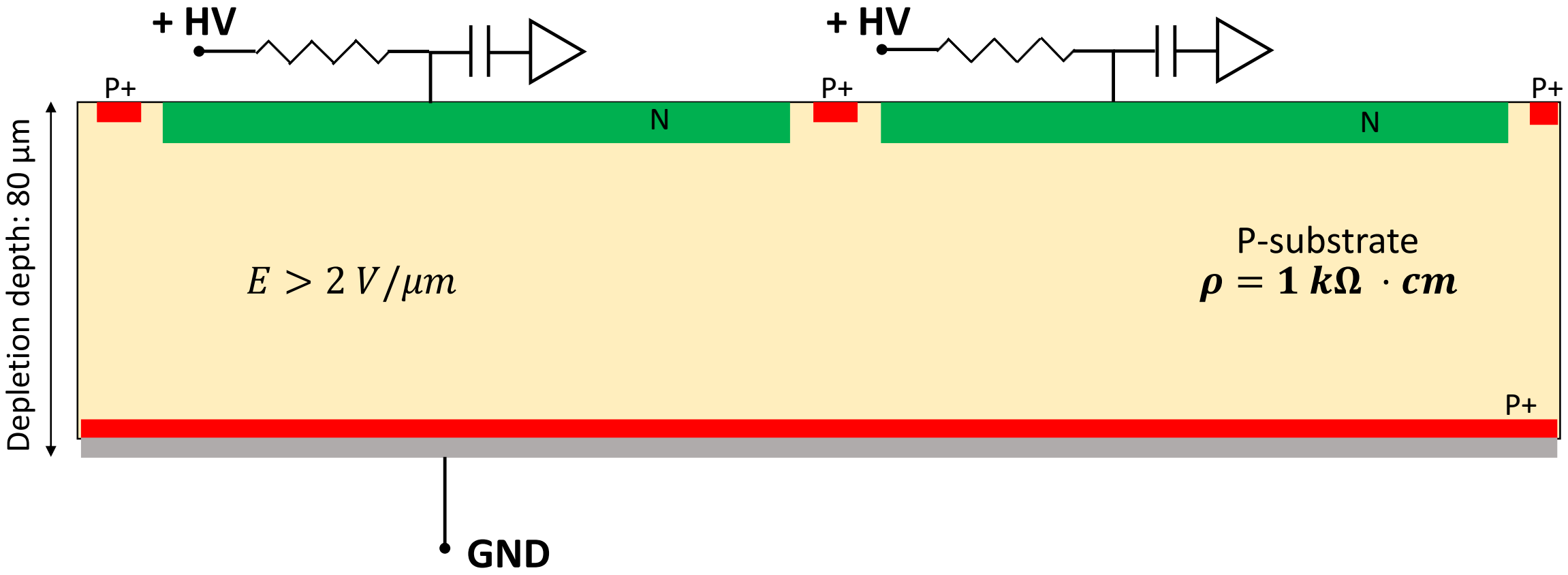
Sensor design

Simplified architecture for **large pixel size**.



- **SG13S technology** from IHP microelectronics.
- N-on-P pixels.
- Substrate to ground.
- Positive high voltage to pixels.
- Signal routed to the front-end on the chip periphery.

Sensor design



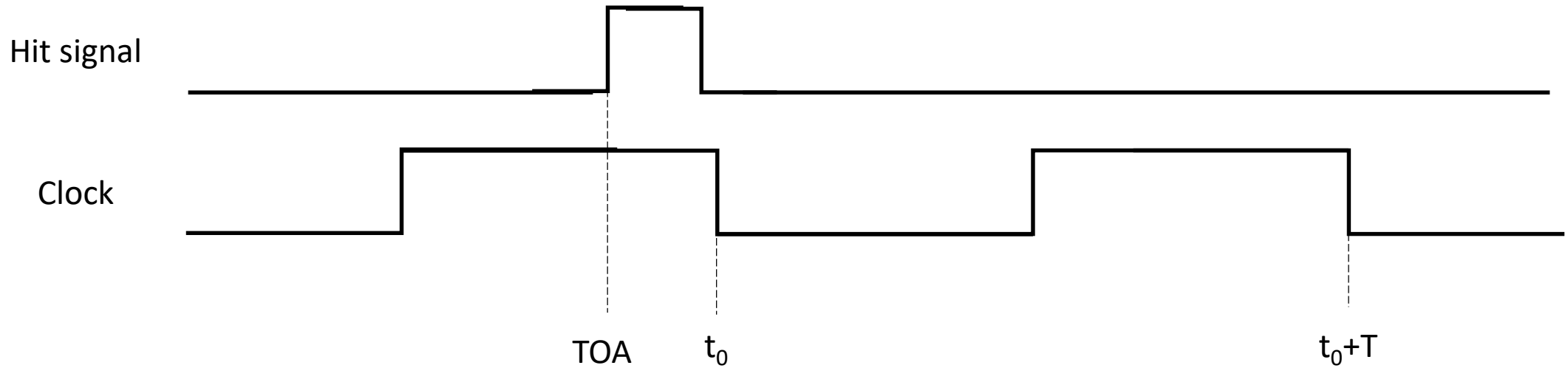
TDC and synchronization

Out target: **synchronize 2000 chips at 10 ps precision** for a TOF-PET scanner.

Synchronization technique (patent pending):

- All chips have **free-running TDCs**.
- A **low-jitter clock** is distributed to the chips.
- The first edge and the period of the clock are measured.
- They are used to provide a time **reference and a frequency calibration** for each TDC.

- Robust solution.
- Synchronization at 10 ps precision with **no PLL.**
- Very low frequency jitter of the TDCs.



TDC and synchronization

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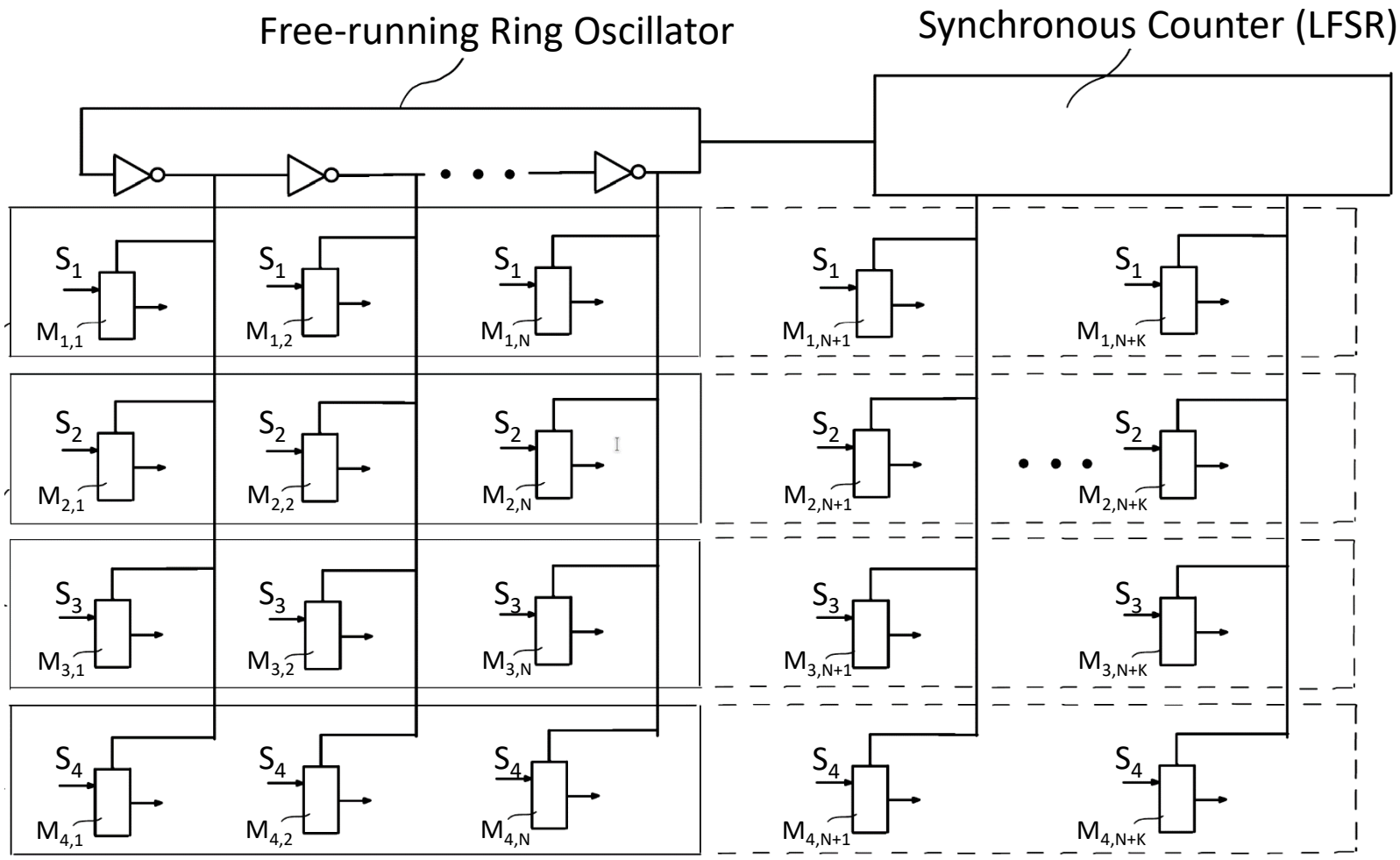
TDC design:

S_1: Hit signal rising edge

S_2: Hit signal Falling edge

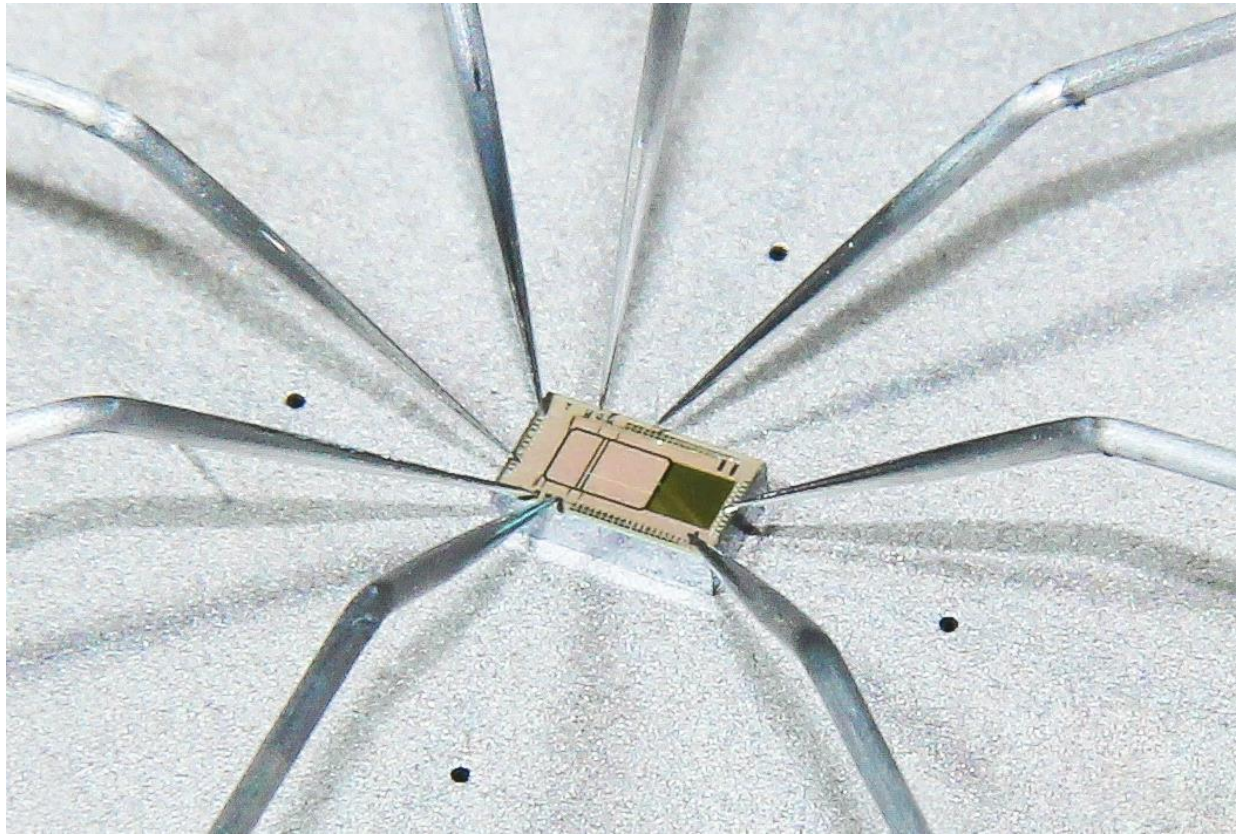
S_3: 1st clock Rising edge

S_4: 2nd clock Rising edge



First test

Concept prototype



December 2017

Monolithic chip: sensor + front-end.

- High wafer resistivity ($1\ k\Omega cm$).
- Breakdown voltage: above 160 V.
- Pixel size: $900\ \times\ 900\ \mu m^2$ and $900\ \times 450\ \mu m^2$.
- **No thinning, no backplane metallization.**

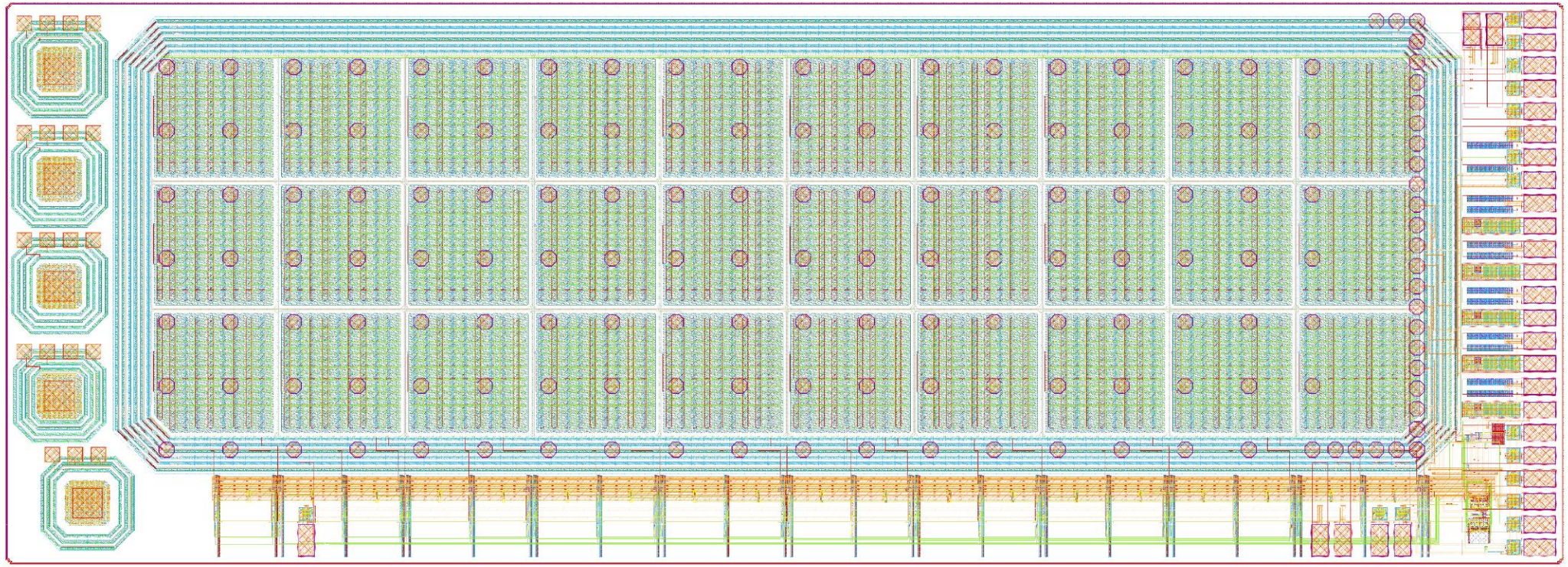
Beam Test with MIPs:

- **Time resolution: 202.3±0.8 ps.**
- **Efficiency 99.8%.**
- **Power consumption: 80 mW/cm².**

For more information:
L. Paolozzi *et al* 2018 *JINST* **13** P04015
doi: https://doi.org/10.1088/1748-0221/13/04/P04015

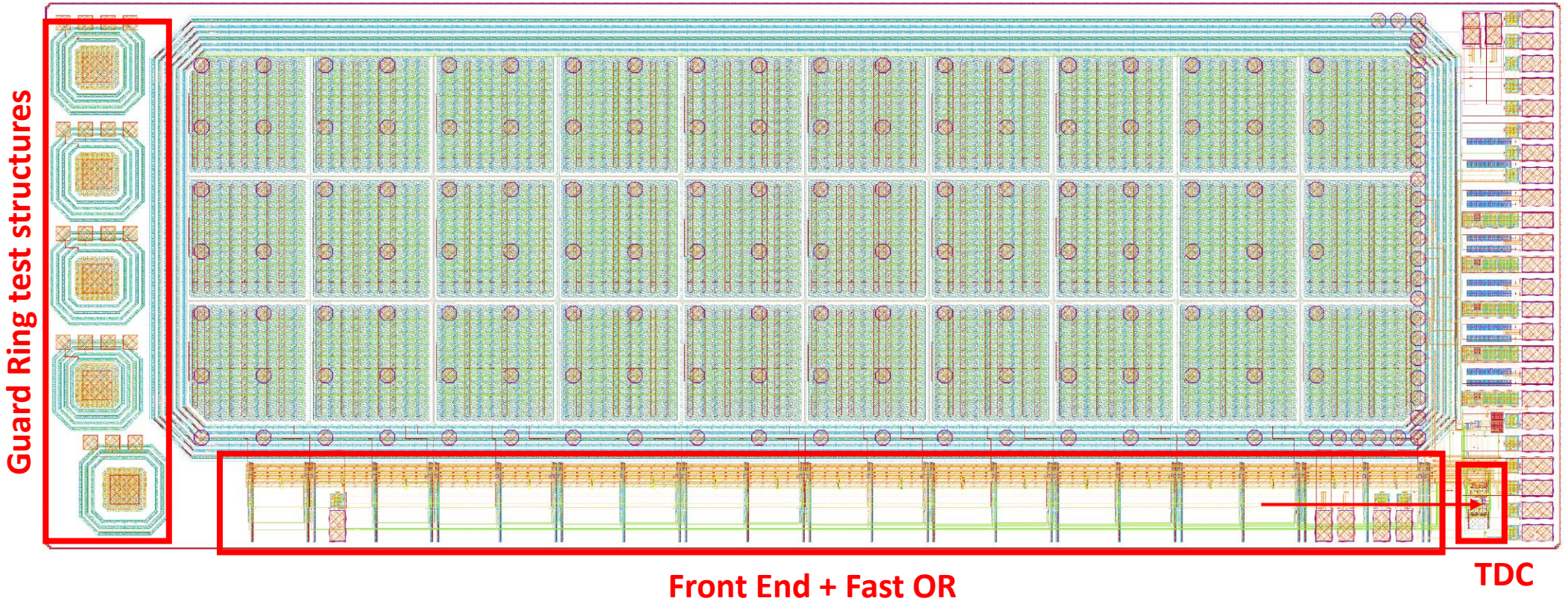
Demonstrator chip

Demonstrator layout

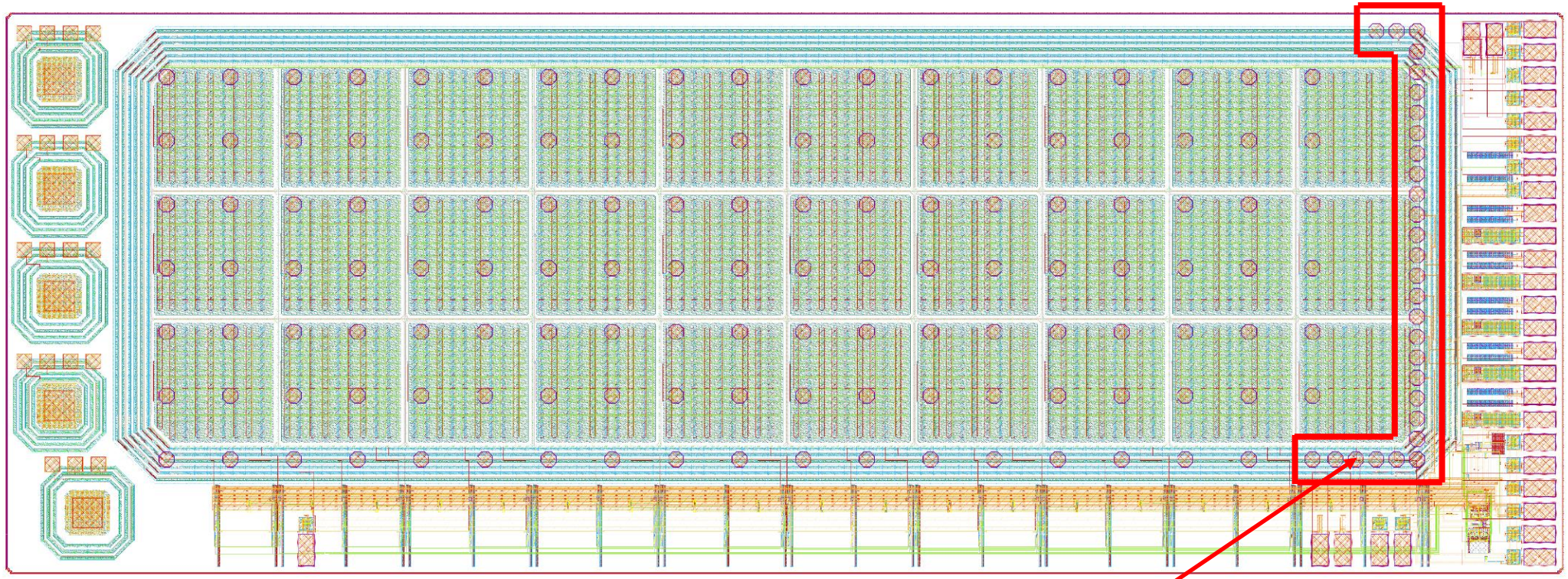


- 3×10 matrix, $500 \times 500\ \mu m^2$ pixels.
- Preamplifier, discriminator, 50 ps binning TDC, logic, serializer integrated in chip.
- Thinned to 100 µm. Depletion depth 80 µm.
- Full backside processing.

Demonstrator layout



Demonstrator layout



Bond-Pads:
Inducing noise from single-ended clock-lines.

Four pixel masked

Beam test with MIPs at CERN SPS

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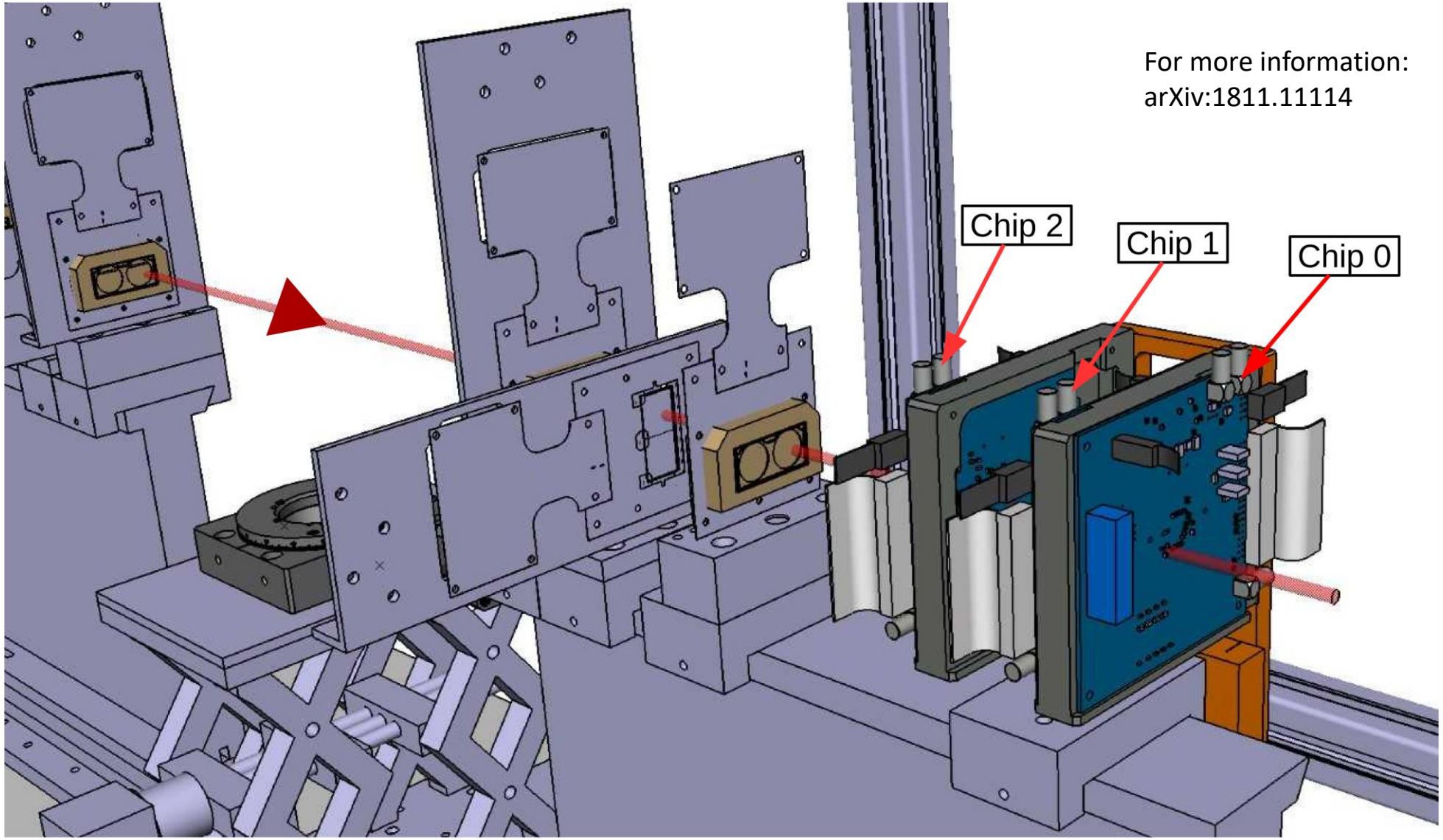
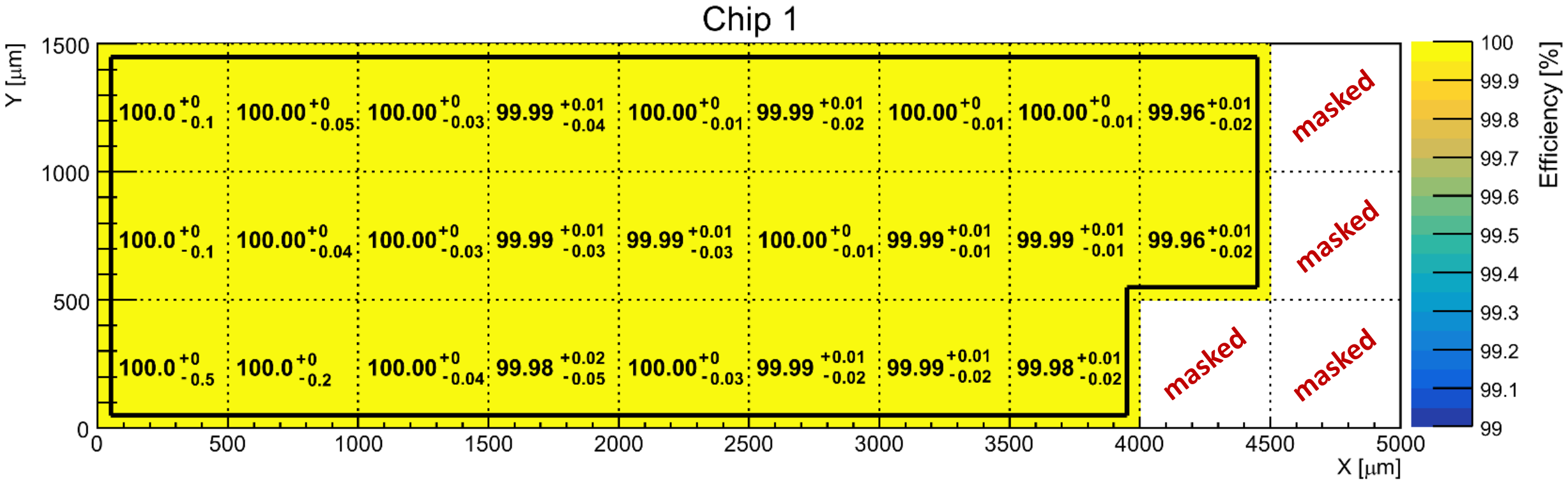


For more information:
arXiv:1811.11114

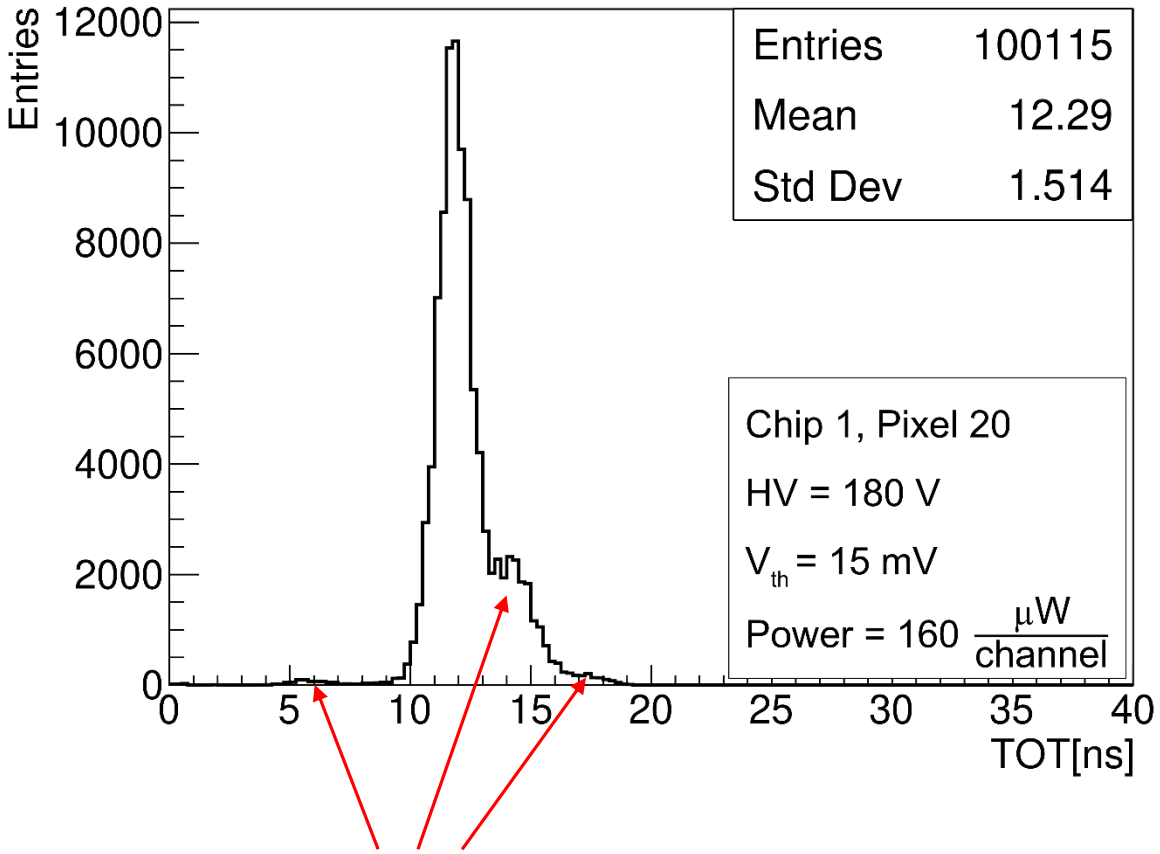
Efficiency



Global efficiency above 99.98%

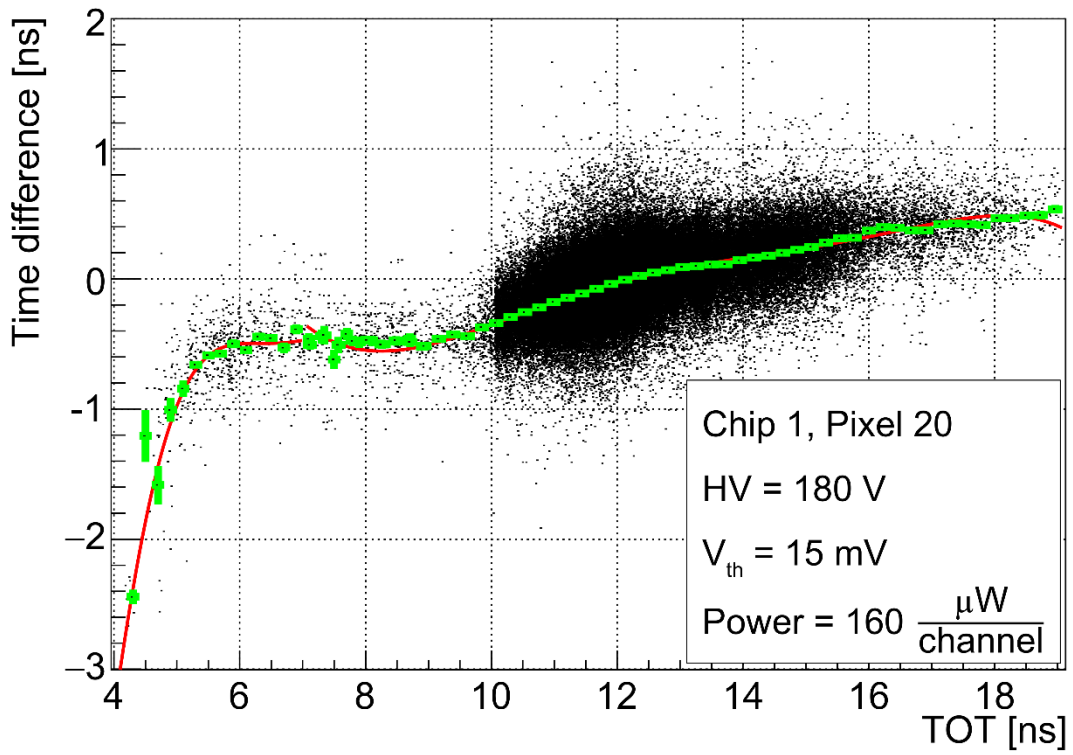
$ENC \cong 350\, e^-$

Calibrations



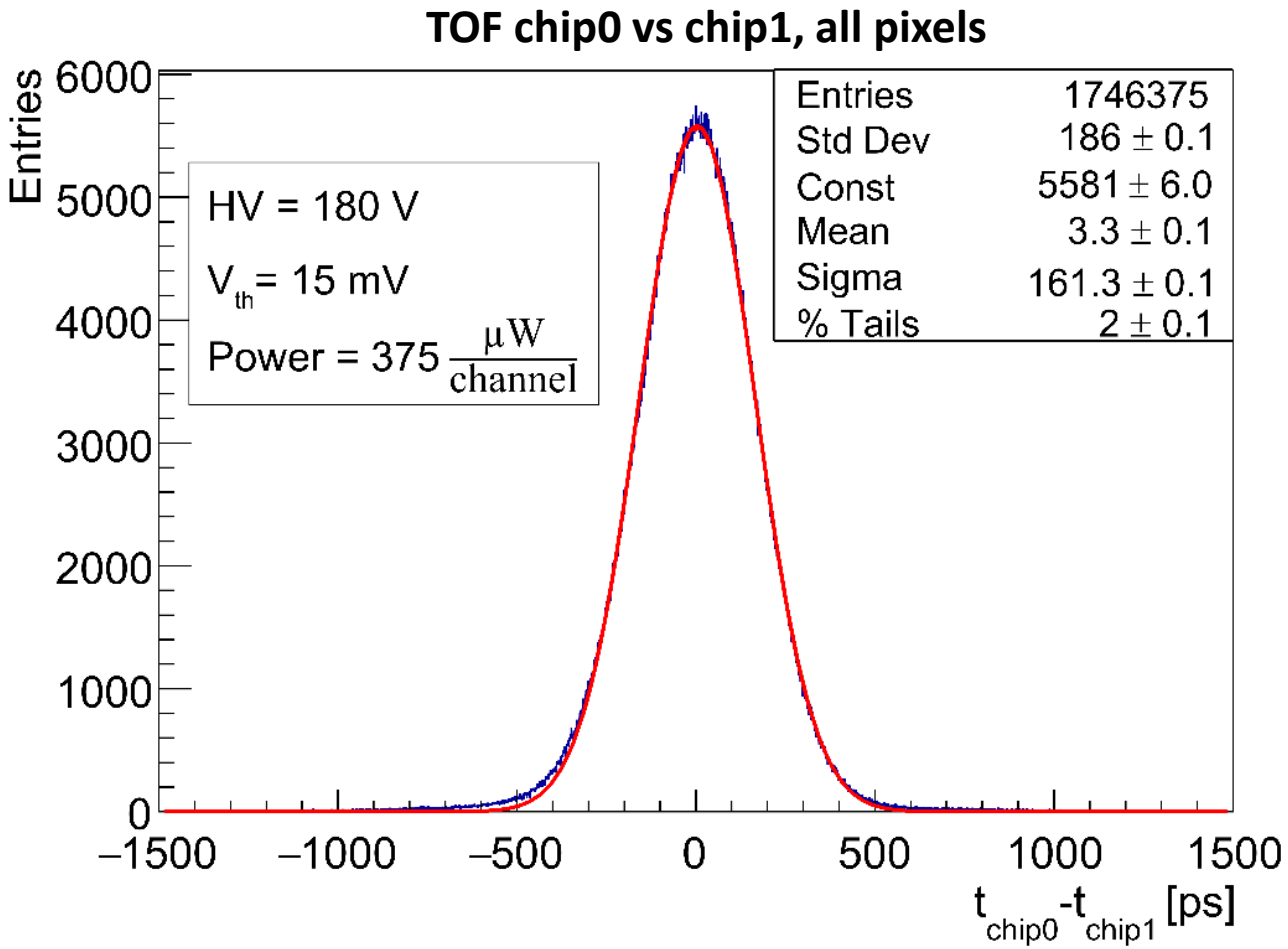
Secondary peaks observed on the TOT

- Possible induced noise from the digital output.
- Non linear response of the discriminator.



Independent time walk correction for each pixel.

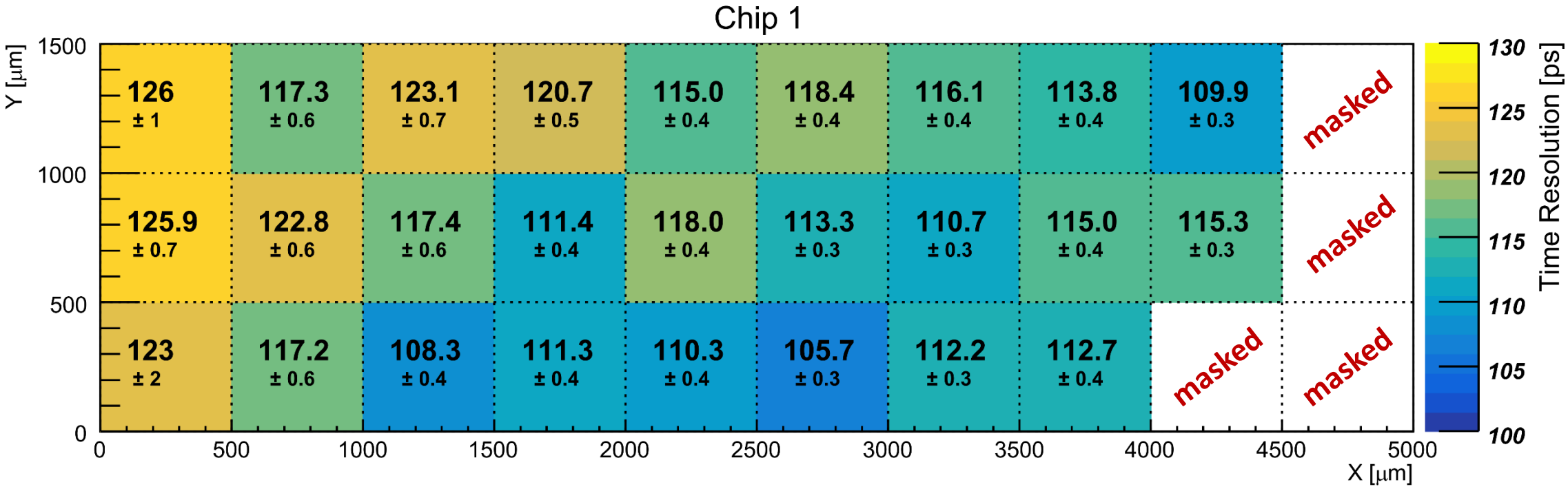
Time resolution



	Time resolution [ps]	
	low-power	high-power
$\sigma_{t,\,chip\,0}$	**127.3 ±0.2**	**111.3 ±0.1**
$\sigma_{t,\,chip\,1}$	**134.2 ±0.2**	**116.7 ±0.1**
$\sigma_{t,\,chip\,2}$	**127.2 ±0.2**	**111.2 ±0.1**

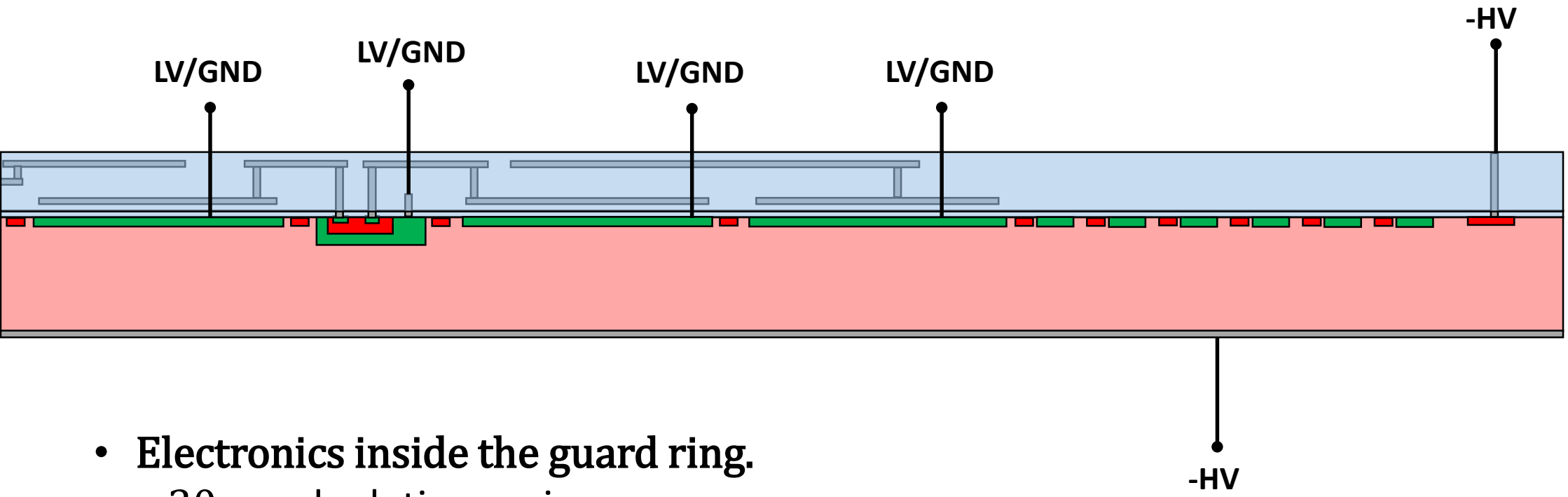
- Low power: $80\,\frac{mW}{cm^2}$
- High power: $160\,\frac{mW}{cm^2}$

Time resolution



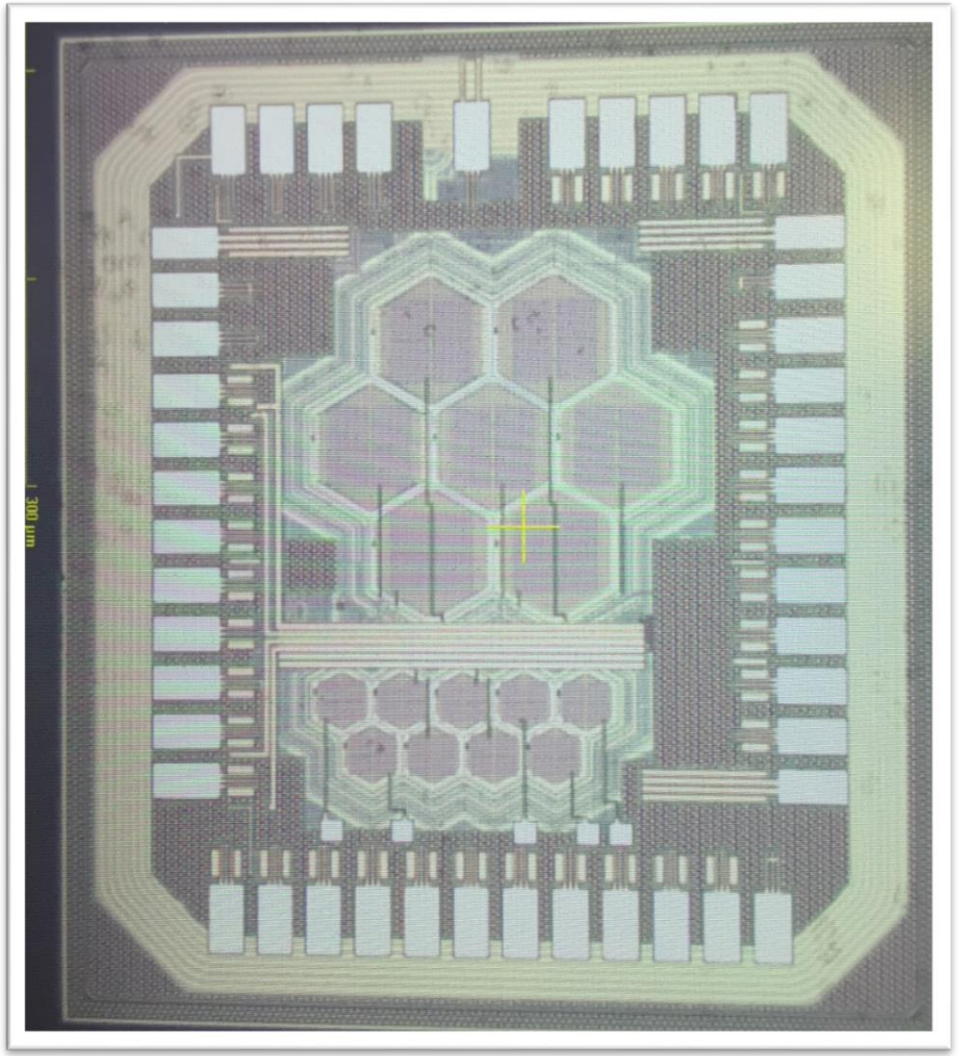
Future steps
Milestone 2

Target: sub-100ps resolution



- **Electronics inside the guard ring.**
- $\sim 30\ \mu m$ depletion region.
- $\sim 100 \times 100\ \mu m^2$ pixel size.
- Standard wafer resistivity $(50\ \Omega \cdot cm)$

Target: sub-100ps resolution



Test prototype – IHP SG13G2 technology:

- Insulated HBT designed with IHP microelectronics and characterized in foundry.
- 50 µm thick, no backside processing.
- High voltage: breakdown at -200 V.
- **Electronics fully functional.**
- **Data taking in progress.**

Conclusions

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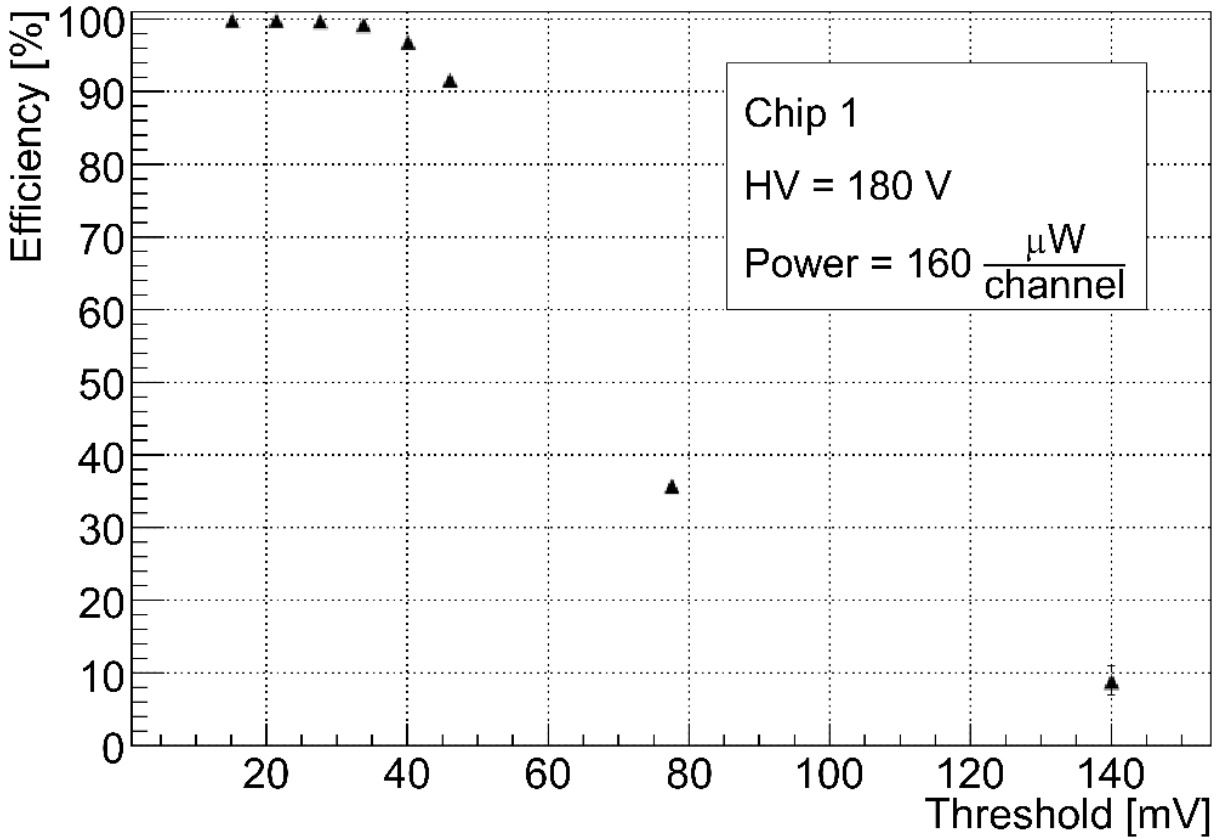
- A **technique to exploit the timing performance of SiGe HBTs** with pixel sensors has been developed.
- Thanks to this technique, we reached our first milestone **with a time resolution of 110 ps** with the first SiGe BICMOS monolithic silicon pixel sensor.
- A **synchronization method for picosecond measurement**, scalable to large area systems was filed for patent.
- Work is ongoing towards the production of **smaller area pixels for sub-100ps time resolutions**.


Zoom: 10x
100µm
Thank you

Backup

Efficiency curve



TT-PET Basic detection element

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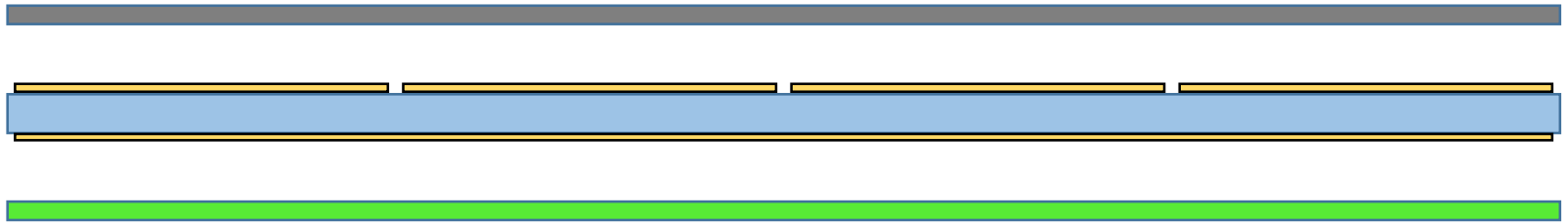
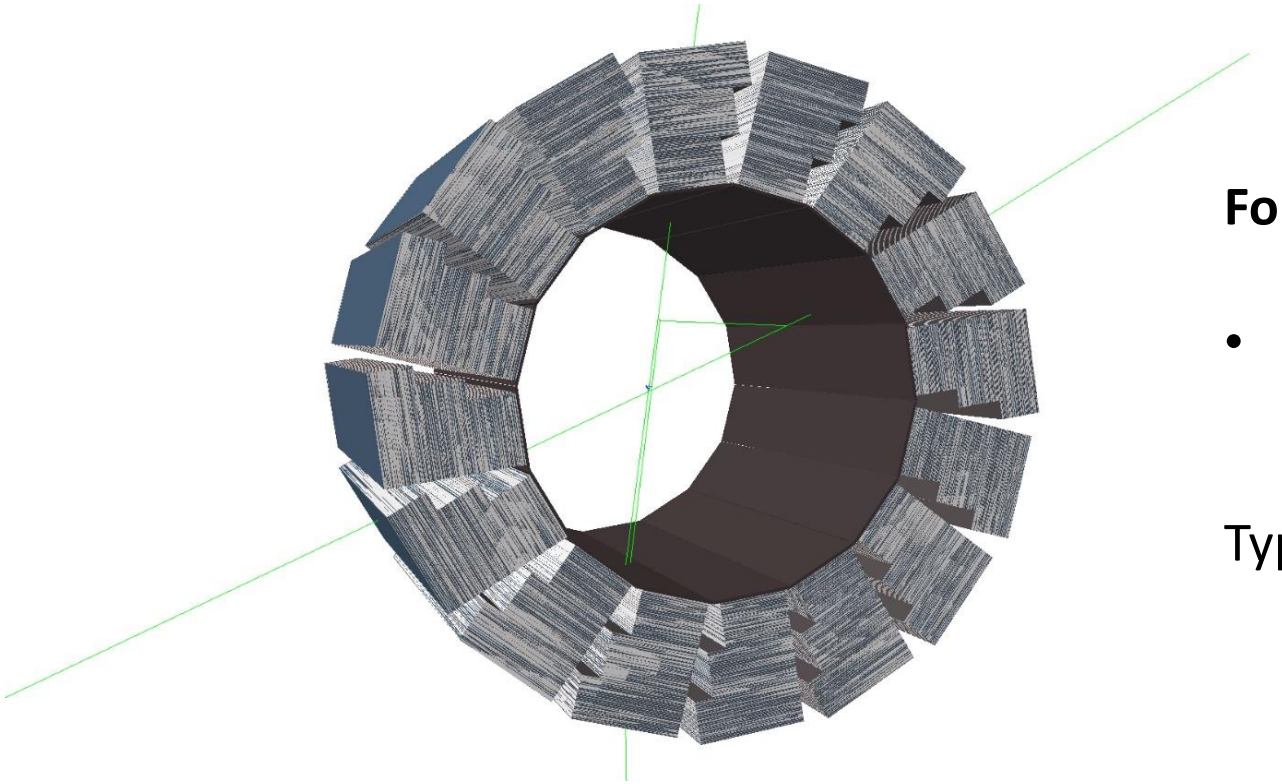
Module



- **Spacer**
  $50\ \mu m$ thickness
- **Monolithic pixel sensor:**
  $100\ \mu m$ thickness
- **Lead converter**
  $50\ \mu m$ thickness

The TT-PET scanner

A Geant4 simulation has been developed to predict the scanner efficiency to $511\ keV$ photons, the expected detection rate per chip and the scanner space resolution.



For 1.5 cm cell thickness

- Scanner sensitivity (coincidences per disintegration):5 %

Typical small animal PET sensitivity: from 1% to 10%