PIXEL 2018 CONFERENCE

Electrical Characterization of AMS aH18 HV-CMOS after Neutron and Proton irradiation

DMSSULTAN

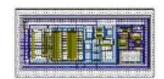
University of Geneva

Taipei, December 10th 2018

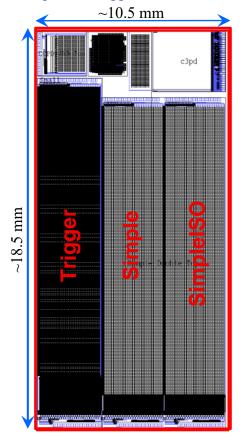
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AMS ATLASPix1 180 nm Monolithic Chip

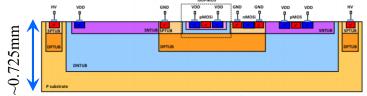


Top View Trigger Matrix





Top View Simple Matrices



Cross Sectional Schematics

- The prototype of 180 nm HV-CMOS Technology (large electrode design)
- Different flavors: Trigger (50X60 μm²) and Simple matrices (130X40 μm²). SimpleISO holds additional deep P-well.
- Several Substrate Resistivity: 20, 80, 200 Ω -cm.
- No active guard-ring is considered

Advantages:

- Commercially cost effective
- High yield and high efficiency
- Radiation Hard Capability

See More: M. Keihn talk at Pixel 2018

Challenges:

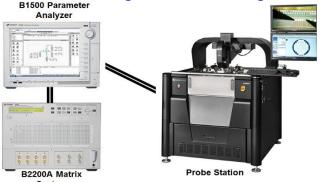
- Partially depleted substrate
- Technology and process dependent radiation hardness
- Highly Granular CMOS comes with additional J_{lk} , leakage
- Careful design and systematic study is required

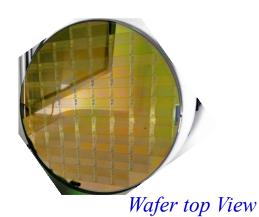


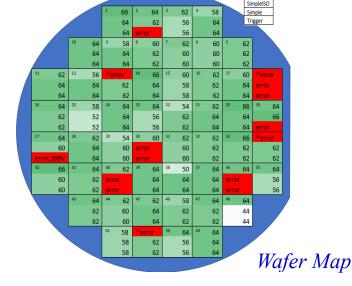
AMS ATLASPix1 180 nm Monolithic Chip

FACULTÉ DES SCIENCES

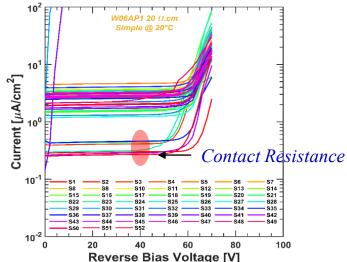






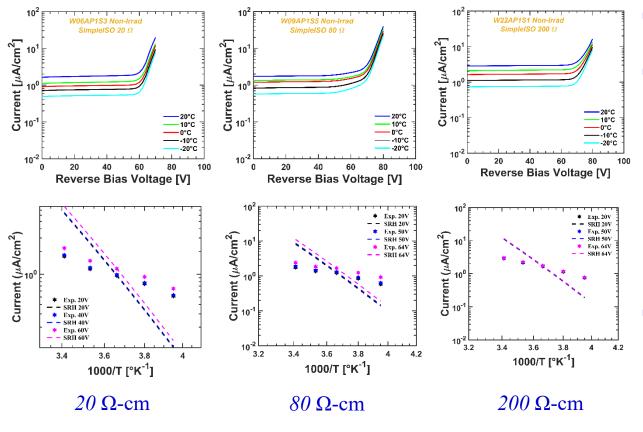


- A systematic study made using Low leakage current complaint B2200A matrix and high precision ATT thermal conditioner used at dry-air condition.
- Electrical probing made with proper biasing to HV, VDDD (1.8V), VDDA (1.8V), and VSSA(1.0V) as per reference of ATLASPix1 design.
- At right, there is the wafer top view. Wafer map shows a systematic summary of ATLASPix pixel-matrices.
- Green marker has assigned to pixel matrix if the V_{bd} is greater than 30 V and leakage current is limited to 5μA/cm² before avalanche breakdown
- Around 80% dies seemed electrically qualified, means they have reasonable higher breakdown and power planes are isolated.
- Typical breakdown voltage \sim 50-60V. Adimensional function used for the breakdown evaluation for k(I,V)=4.





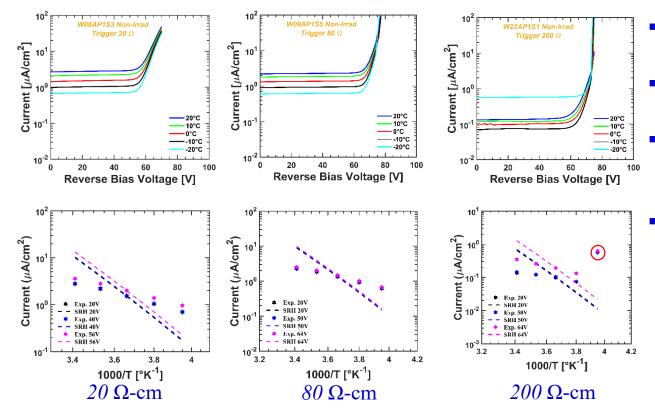




- Breakdown Voltage is beyond 50V
- Leakage current is deviating the Arrhenius prediction.
 - Leakage current is dominated by surface damage
 - AMS Design Kit-Generated HV Guard ring floating
 - MCz substrate wafer procures more thermal donor (oxigatnted vacancies) during processing, a great source to leakage increase.
- Leakage current remains on the order of ~1uA/cm² at -10 °C ambient condition.

- Layout improvement with additional or biased guard-ring should improve the situation.
- Additional long sintering step at the wafer level can improve the situation.

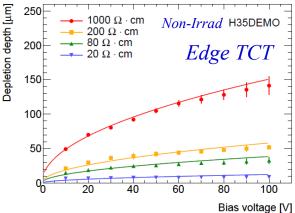




- At 20 °C, some thin candidates show leakage abnormality than its higher ambient conditions.
 - Mean free path is enriched-> leakage current rise.
- Precise control in dicing thinning process could improve the situation

Non-Irradiated Trigger

- Breakdown Voltage is beyond 50V
- Leakage current is deviating the Arrhenius prediction.
 - Leakage current remains on the order of ~1uA/cm² or less at -10 °C.
- Several sample thinned down to ~100 um.



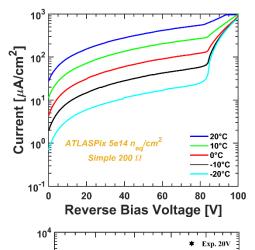
E. Zaffaroni et. al. JINST (P10004)

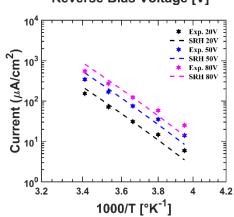
Bern Proton Irradiated 5e14 n_{eq}/cm²



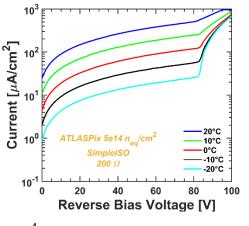
Layout Top View: Simple Matrices

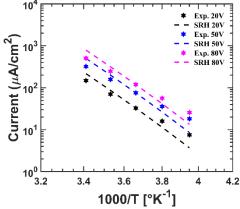
- Sample irradiated at BERN Cyclotron with 16.7 MeV Proton
- Breakdown Voltage improves beyond 80V simple matrices.
- Electrical distribution is not uniform.
- A spatially dependent de-trapping require additional reverse potential
- Leakage current rises 20x magnitude higher.
- Modification of effective doping concentration from both surface and bulk effect
- Damage constant rate is ~8×10⁻¹⁷ (A/cm) before Vbd, bit larger.
- Less significant, requires dedicated depletion measurement
- Peripheral current is still paying the role
- Arrhenius disagreement seen at nonirradiated candidate seems improving.
- Intrinsic leakage is larger in scale





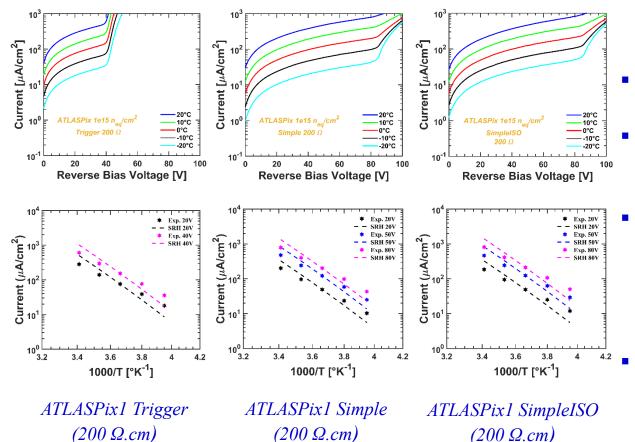
ATLASPix1 Simple (200 Ω .cm)

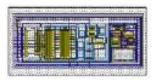




ATLASPix1 SimpleISO $(200 \Omega.cm)$

Bern Proton Irradiated 1e15 n_{eq}/cm²





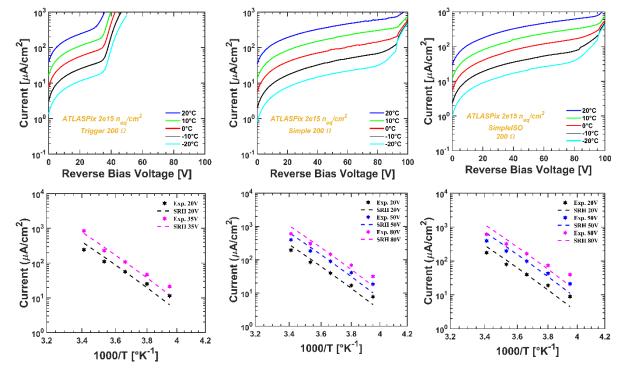
Layout Top View: Trigger

- Breakdown Voltage is beyond 80V (Simple and SimpleISO)
 - As expected, leakage current increases 50x more with higher fluence.
- Damage constant rate is \sim 3- 4×10^{-17} (A/cm) before V_{bd} as expected.
 - Dominated by bulk damage contribution

V_{bd} of Trigger matrix decreases to ~41V

- Deep N-well is almost covering the pixel geometry -> more uniform electric field distribution
- Triggers impact ionization at lower reverse bias

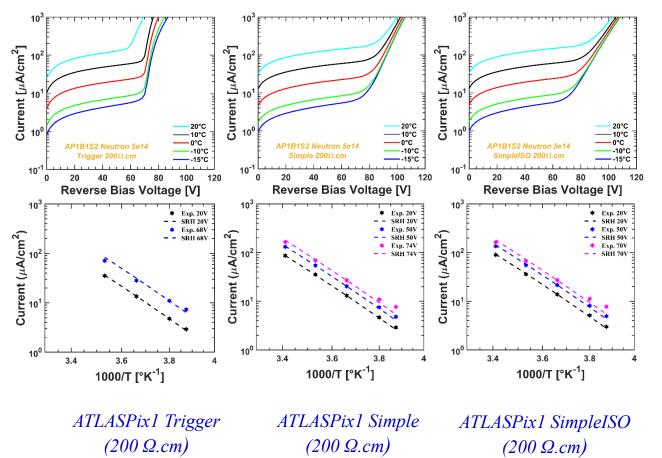
Bern Proton Irradiated 2e15 n_{eq}/cm²



- ATLASPix1 Trigger ATLASPix1 Simple (200 Ω .cm) (200 Ω .cm)
- ATLASPix1 SimpleISO (200 Ω.cm)

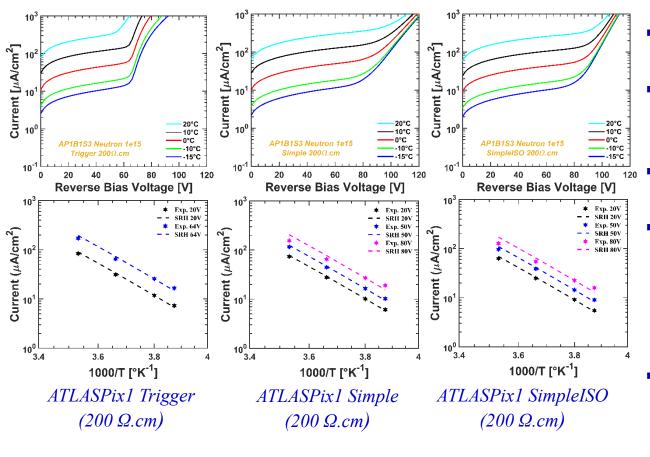
- Breakdown Voltage of trigger matrix is ~36V
- As expected, leakage current increases 2 order magnitude higher fluence than non-irradiated case.
- V_{bd} at simple matrices increase beyond 90V.
- Higher interface states and bulk traps
 larger reverse potential to de-trap the charges (spatially dependent)
- Still in better Arrhenius agreement with expectation
- Peripheral leakage hinders underneath the larger intrinsic leakage scale.
- Damage constant rate, α^* , $\sim 4 \times 10^{-17}$ (A/cm) before V_{bd}, as expected.

JSI Neutron Irradiated 5e14 n_{eq}/cm²



- Breakdown voltage is beyond 70V (Simple and SimpleISO)
- As expected, leakage current increases 40x more with higher fluence.
- Damage constant rate is $\sim 10 \times 10^{-17}$ (A/cm) before V_{bd}.
 - Dominated by surface damage
 - Dedicated edge-TCT investigations is required.
- V_{bd} of Trigger matrix increases to ~68V
 - Deep N-well is almost covering the pixel geometry -> more uniform electric field distribution
 - Triggers impact ionization at lower reverse bias

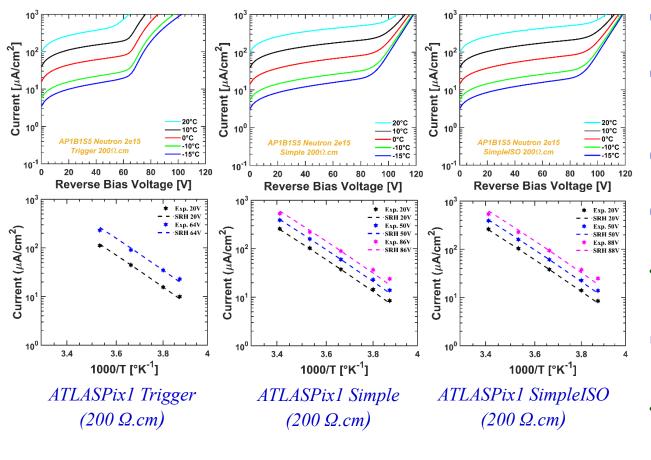
JSI Neutron Irradiated 1e15 n_{eq}/cm²



- Breakdown Voltage is increased to 80V (Simple and SimpleISO)
- As expected, leakage current increases 100x more with higher fluence.
 - Damage constant rate is $\sim 8 \times 10^{-17}$ (A/cm) before V_{bd}.
- V_{bd} of Trigger matrix decreases to ~64V
 - Uniform electric field distribution

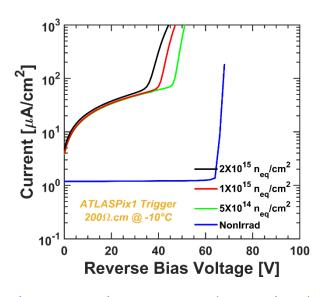
 -> Triggers impact ionization at lower reverse bias
- A dedicated edge-TCT measurement is required.

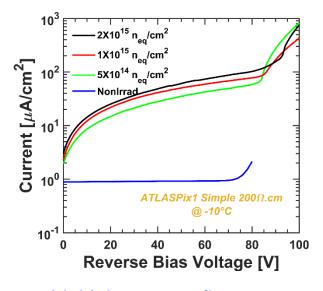
JSI Neutron Irradiated 2e15 n_{eq}/cm²



- Breakdown Voltage of trigger matrix is ~62V
- As expected, leakage current increases 200x higher fluence than non-irradiated one.
 - V_{bd} at simple matrices increase beyond 90V.
 - Arrhenius prediction is well in agreement in all three flavors.
 - Peripheral leakage hinders underneath the larger intrinsic leakage generation.
 - Damage constant rate, α^* , $\sim 6 \times 10^{-17}$ (A/cm) before V_{bd}.
 - Geometry dependent rate calculation.

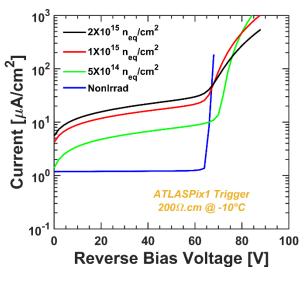
Comparative Analysis ATLASPix1 Proton

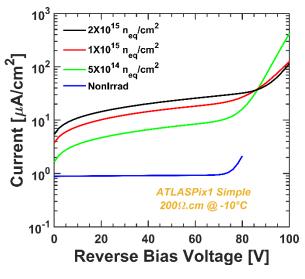




- Trigger matrix goes to a decreasing breakdown with higher proton fluence
 - Peripheral current leads to occur impact ionization earlier
- Simple matrices goes to a increasing breakdown with higher proton fluence
 - Non-uniform electrical distribution beyond N-well, requires higher reverse potential to de-trapping the carrier
- Higher damage contribution with higher fluence leads leakage increase in all matrix flavors.
 - For the highest fluence, it remains $\sim 100 \text{ uA/cm}^2$

Comparative Analysis ATLASPix1 Neutron



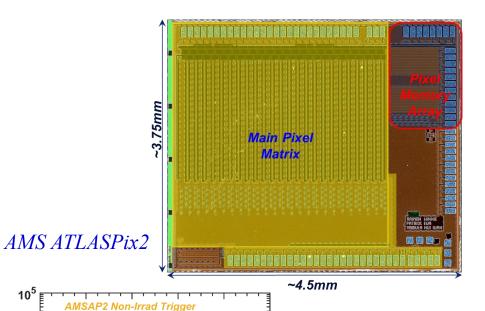


- With higher neutron fluence, breakdown voltage trigger matrix remains almost comparable to non-irradiated case.
 - Mass bulk damage, as expected
- A little decreasing trend of breakdown voltage at trigger matrix at higher fluence
 - Effect of back ground Gamma of reactor
- Breakdown voltage of simple matrices also goes to a increasing breakdown with higher neutron fluence
 - Geometrical difference of pixel pitch
- As expected, leakage current increases in with higher fluence irrespective to pixel

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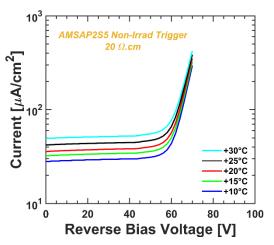
AMS ATLASPix2



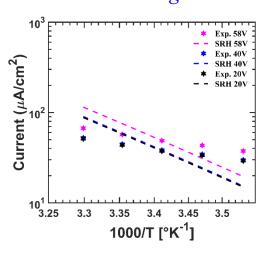
- I-V Curves

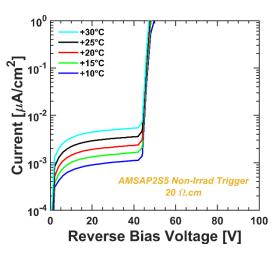
- A small version of ATLASPix1 M2 Trigger matrix having pixel dimension 128X50 μm².
- Standard substrate resistivity (20 Ω .cm)
- Matrix size is of 24X36 pixels.
- Die Thickness ~220 μm.
- Die probing made with proper biasing to HV, VDDD (1.8V), VDDA (1.8V), and VSSA(1.0V).
- The left top-image is showing a die top view. It holds both small pixelated matrix and the Memory type test structures.
- Both Main Pixel Matrix and Pixel memory Array (PMA) share the same HV lines.
- PMA is intended to study SEU tolerant memory cells
- I-V reports the electrical behavior of several pixel matrices.
- Could be expected 1 order magnitude lower in scale @ -10 °C.
- Typical breakdown is beyond 50 V.



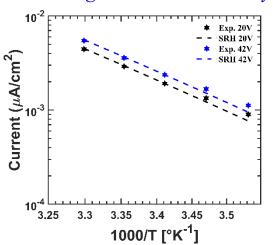


With Enabling CMOS

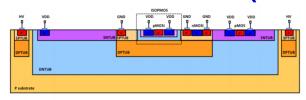




Biasing HV and N-well only

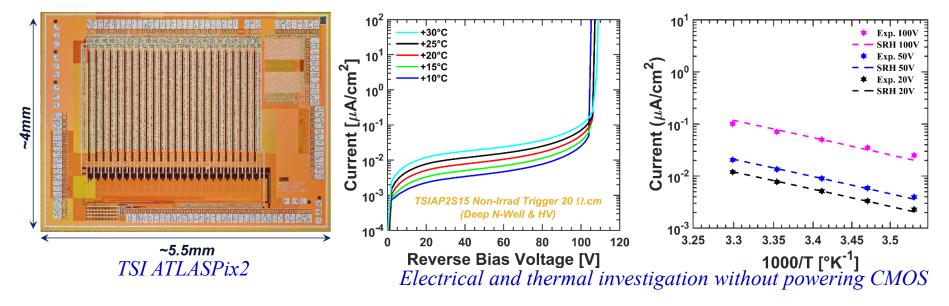


Non-Irradiated ATLASPix2 (AMS)



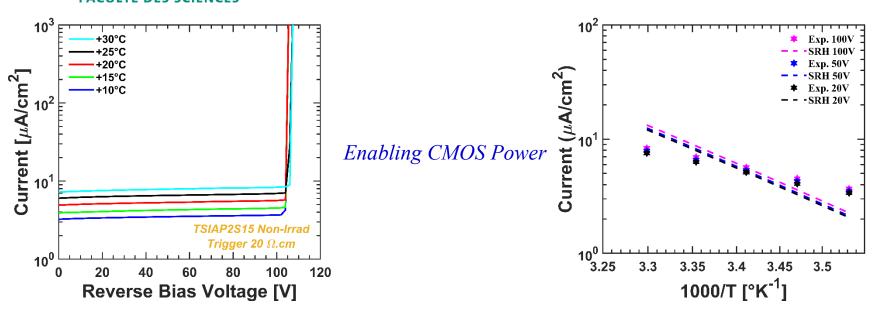
- Tested W/O powering CMOS
- Breakdown Voltage is around 50V
- Investigation was limited near room only.
- Dry-air system is refurbishing currently
- With powering CMOS, both RO and diode leakage studied
- Most share is from CMOS
- As expected, diode driven leakage is well agreement with Arrhenius Prediction
- Arrhenius disagreement seen at proper CMOS powering points surface damage at processing stage.
- Foreseen layout design improvement in coming chip-submission should lead to a better condition.

TSISemi ATLASPix2



- A similar AMS-ATLASPix2 have submitted TSI for reducing the fabrication lead time in very recent.
- It holds same trigger matrix flavour, pixel pitch $128X50 \mu m^2$ and substrate resistivity (20 Ω .cm)
- Matrix size is still of 24X36 pixels and die thickness \sim 254 µm.
- Biasing HV and deep N-Well only, I-V reports similar leakage as seen in similar chip of AMS process at room temperature.
- Arrhenius prediction of thermal dependent carrier generation is well agreement with exp. data.
- Breakdown voltage reports beyond 100V!

TSISemi ATLASPix2



- Breakdown voltage TSI-Semiconductor chip report ~104-108V, as expected.
 - Almost double than AMS-candidates
- Disagreement with Arrhenius predictions still suggest the possible layout improvement (i.e. active guard-ring)
- Sharp breakdown and almost 1 order lower leakage scale than AMS-candidates, denote a greater TSI processing maturity.
 - Processing technology and instrumentation dependent

Summary

- Non irradiated ATASPix1 has ~1uA/cm² leakage at -10 °C, and breakdown voltage beyond 50 V.
- A post sintering step at wafer level (i.e. 420 °C at 60 mins) can be a great remedy to the oxygenated vacancy induced leakage.
- An active guard-ring structure has already accounted within foreseen chip submission to ensure the robust termination structures.
- Simple matrices of ATLASPix1 seem healing the surface peripheral leakage inflation with proton irradiation.
- Trigger matrix of ATLASPix1 also reports hindering the peripheral leakage with larger damage induces leakage. (an already good sign!)
- Neutron damage study proves that surface damage played vital role of earlier breakdown for trigger matrix as fluence increases.
- Non-irradiated AMS-ATLASPix2 chips have leakage ~5uA/cm² near room temperature, V_{bd} is similar to ATLASPix1.
- TSI Processed ATLASPix2 reports V_{bd} almost double of AMS production while leakage is 10x lower.
- More dedicated low temperature measurements, Edge-TCT and Irradiation study have targeted in near future investigations.

Thanking You

