Upgrade of the ALICE Inner Tracking System

Dimitra Andreou
for the ALICE Collaboration
CERN - Nikhef

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OUTLINE

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Introduction

Inner Tracking System (ITS)

- Silicon Pixel Detector (SPD)
- Silicon Drift Detector (SDD)
- Silicon Strip Detector (SSD)

Time Of Flight

Transition Radiation Detector

Projection Chamber

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Upgrade Motivations

**Physics Motivations**
High precision measurements of rare probes over a broad $p_T$ range.

**Examples:**

**Heavy - Flavour particles**
- Thermalisation and hadronisation of heavy quark in medium
- Heavy-quark in-medium energy loss & mass dependence

**Low-mass dielectrons**
- Thermal radiation from QGP
Upgrade Specifications

Higher Tracking Resolution & Efficiency

Current ITS

- 6 Layers
  SPD, SDD, SSD
- Material Budget
  $X/X_0$ 1.14% (inner layers)
- Readout rate
  1kHz (Pb-Pb)
- Pixel size (SPD)
  $50 \times 425 \mu m^2$
- Inner Radius 33mm

Upgraded ITS

- 7 Layers of MAPS
- Material Budget
  $X/X_0$ 0.3% (inner layers)
- Readout rate
  100kHz (Pb-Pb)
- Pixel size
  $29 \times 27 \mu m^2$
- Inner Radius 22mm

Technical Design Report for the Upgrade of the ALICE Inner Tracking System
Seven layers of Silicon Pixel Detectors

**Outer Barrel (OB)**
- 2 Middle Layers ➔ 2 x 4 Modules / Stave
- 2 Outer Layer ➔ 2 x 7 Modules / Stave
- Material budget ➔ 1 % X/X₀

**Inner Barrel (IB)**
- 3 Layers ➔ 48 Staves
- 1 Stave ➔ 1 IB Module
- Material budget ➔ 0.3 % X/X₀

- **10 m² active silicon area**
- **0.5 T Magnetic Field**

Radiation level (IB):
- TID: 2.7 Mrad
- NIEL: 1.7 x 10¹³ 1 MeV nₑq cm⁻²

**Coverage**:
- r coverage: 22 - 400 mm
- η coverage: |η| ≤ 1.22
  for tracks from 90% of the most luminous region
Expected Performance

Impact Parameter Resolution

- ALICE
  - Pointing Resolution (µm)
  - Current ITS (data)
  - Upgraded ITS

Tracking Efficiency

- ALICE
  - Standalone tracking efficiency (%)
  - Current ITS
  - Upgraded ITS
ALPIDE chip

ALICE PIXEL DETECTOR
CMOS MAPS technology

- 512 x 1024 Pixels
- High resistivity
  p-type (25 μm) >1 kΩ cm
- Deep p-well → full CMOS in-pixel circuit
- Substrate bias to increase depletion volume
- Spatial Resolution 5 μm
- HEP & Medical applications

TowerJazz 0.18 μm CMOS imaging process

ALICE
NICA MPD (JINR)
sPHENIX (BNL)
Proton CT

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Detector Design

Outer Barrel HIC

- Copper Flexible PCB (FPC)
- Hybrid Integrated Circuit (HIC)
- Aluminium Cross Cables
- FPC - ALPIDE ➔ Wire-bonding

Outer Barrel Stave

- Aluminium Power Bus
- Lightweight Space Frame
- Water Cooling
- HIC interconnections ➔ Soldering
Detector Design

Inner Barrel Stave
- Flexible PCB
- 9 sensors
- Cold Plate
- Space Frame

First Assembled Inner Barrel Half Layers
- Half-layer 0
- Half-Layer 1
- Half-Layer 2
Mechanics

**Barrel Assembly**
Readout Electronics

Detector

- Readout logic inside ALPIDE
- No additional active components and electronics

Readout Units

- 8 meter cables
- 1.2 Gb/s (data IB)
- 400 Mb/s (data OB)
- 80 Mb/s (ctrl IB/OB)
- Clock
- Power
- 192 Readout Units
- Distribute Trigger & Control Signals
- Interface datalinks to ALICE DAQ
Production & Qualification - Chip level

- Thinning & Dicing of silicon wafers (50μm and 100μm)
- Pick & place to trays
Production & Qualification - HIC level

- Chip selection & FPC verification
- Positioning & gluing of Chips-FPC
- Chip alignment
- HIC testing
- Ultrasonic wedge bonding
  FPC - HIC interconnection
- Shipment to 5 OB stave assembly sites

ALICIA machine
Production & Qualification - Stave level

- Cold Plate positioning
- Glue deposition
- HIC positioning
- HIC to HIC interconnection
- Space frame on CP
- Power Bus position & folding

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ITS Upgrade HIC and Stave Characterisation

• Detailed verification and testing after each production step
  • Assembly
  • Metrology
  • Electrical tests with dedicated software
  • Database storage
• Classification of Components
• Threshold scan
  • Check analogue performance
  • Chip by chip threshold tuning, here shown stave (100M channels), all chips tuned to 100 e (left plot)
  • Typical noise figures ~5e (chips, HICs and half-staves)

**Outer Barrel Stave Threshold & Noise Scan**

\[
\mu = 99.4 \text{ e}^- \\
\text{RMS(\mu)} = 20.6 \text{ e}^-
\]

\[
\sigma = 5.53 \text{ e}^- \\
\text{RMS(\sigma)} = 0.96 \text{ e}^-
\]

**Inner Barrel Module Threshold Scan**

**S-curve measurement**

- data
- fit
- derivative
ITS Upgrade HIC and Stave Characterisation

- Threshold scan
- Check analogue performance
- Chip by chip threshold tuning
- Endurance test (OB HICs)
  - Cycling
  - Triggering
  - Electrical tests
Ageing Tests

Ageing Conditions
- Thermal cycles 10-50 °C
- Humidity 60 % Relative Humidity (RH)

Tested Components
- IB & OB HICS
- IB Staves

Tests
- Electrical tests & Visual Inspection (VI) after one-year equivalent
- Pull tests on wire bonds
- Peel tests chips - FPC (glue adhesion)
- No difference seen in the chip analogue and digital response nor in VI
Summary & Outlook

Current Status

- **ALPIDE production completed**
- **Inner Barrel construction completed**
- **Outer Barrel construction ongoing**
- **Mechanical support structures completed**
- Readout electronics ongoing (completion April 2019)
- Detector assembly 2019
- Upgraded ITS will be commissioned in ALICE 2020
★Upgraded ALICE ITS - 12.5 GPixels
  • CMOS MAPS Technology
  • Low material budget

★Major Improvements
  • Impact parameter resolution
  • Tracking efficiency
  • Increased readout rate
  • Higher granularity
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Thank you!