Tracking with Timing: A System Approach

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& TIMESPOT collaborators
HI-LUMI and Timing: adopted solutions

LHC Hi-Lumi Upgrade program:
\[ \mathcal{L} \approx 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \text{ within } \sim \text{2020} \]
\[ \mathcal{L} \approx 5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \text{ within } \sim \text{2030} \]

High event pile-up (O(100)):
Add the Time coordinate to un-merge space-merged events

CMS (Phase-2, run 2026)
Timing Layer (Barrel: LYSO+SiPM, EndCap: LGAD)). \( \sigma_t \sim 30 \text{ ps} \)
1 point with timing on track (external to Vertex). No timing on IT and OT pixels

ATLAS (Phase-2, run 2026)
HGTD (Endcap): LGAD. \( \sigma_t \sim 30 \text{ ps} \). 1 point with timing on track (external to Vertex). No timing on PIX/ITk

LHCb (Upgrade-2, run 2030)
Strategy under discussion\(^{(*)}\). Need very good resolution in PV timing, for CP studies. Time at Vertex detector level is highly recommended, if not mandatory

*Refer also to Mark R.J. Williams’ talk, this conference
Beyond LHC Hi-Lumi?

<table>
<thead>
<tr>
<th></th>
<th>LHC ALICE ITS</th>
<th>CLIC</th>
<th>HL LHC Outer pixel</th>
<th>HL LHC Inner pixel</th>
<th>FCC pp</th>
</tr>
</thead>
<tbody>
<tr>
<td>NIEL ( (n_{eq}/\text{cm}^2) )</td>
<td>( 10^{13} )</td>
<td>&lt; ( 10^{12} )</td>
<td>( 10^{15} )</td>
<td>( 10^{16} )</td>
<td>( 10^{15} - 10^{17} )</td>
</tr>
<tr>
<td>TID</td>
<td>&lt; 3 Mrad</td>
<td>&lt; 1 Mrad</td>
<td>80 Mrad</td>
<td>1 Grad</td>
<td>40 Grad</td>
</tr>
<tr>
<td>Hit rate ( (\text{MHz/cm}^2) )</td>
<td>10</td>
<td>&lt; 0.3</td>
<td>100-200</td>
<td>2000</td>
<td>200-20000</td>
</tr>
</tbody>
</table>

General specifications for a vertex detector of the next generation (Hi-Lumi and beyond))

- Space resolution: \( \approx 10 \, \mu\text{m} \) (pixel pitch \( \approx 50 \, \mu\text{m} \))
- Radiation hardness: \( 10^{16} \) to \( 10^{17} \) \( 1 \, \text{MeV} \, n_{eq}/\text{cm}^2 \) (sensors) and \( > 1 \) Grad (electronics)
- Time resolution: 100 ps per pixel or better (< 10 ps per track)
- Data rates of the order of \( n \times \text{Tb/s} \) to be handled (real-time?)
Our Project

TIMESPOT (TIME and SPace real-time Operating Tracker) is an initiative for the development of a complete 4D tracker demonstrator.

It has been financed by INFN (Istituto Nazionale Fisica Nucleare – Italy) with about 1 M€ for 3 years of activity (2018, 19, 20). About 20 FTE are involved. P.I.: A. Lai, INFN Cagliari.

The aim of the project is to address the challenge of new-generation trackers from a system point of view, in order to exploit the potentiality of state-of-the-art technologies pushing them to the maximum achievable limit in the direction of a tracker with timing facilities.

Activities on six work packages:
1. 3D silicon sensors: development and characterization
2. 3D diamond sensors: development and characterization
3. Design and test of pixel front-end
4. Design and implementation of fast tracking algorithms
5. Design and implementation of high speed readout boards
6. System integration and tests.
Sensors : Why 3D silicon?

See also G. Forcolin’s talk, this conference

PROS

- Un-matched radiation hardness\(^{(1)}\)
- Already used technology\(^{(2)}\) for vertex detectors
- Strong mitigation of Landau fluctuation by geometry
- Extremely fast signal: optimal potentiality for timing\(^{(3)}\) (not yet exploited!) \(\rightarrow\) optimization by design

CONS

- Fabrication complexity and cost (w.r.t planar standard tech)
- Geometric inefficiency (~blind electrodes) \(\rightarrow\) tilt\(^{(2)}\) or stagger

\(^{(1)}\) J. Lange et al, Radiation hardness of small-pitch 3D pixel sensors up to a fluence of \(3 \times 10^{16} \text{n}_{el}/\text{cm}^2\), 2018 JINST 13, P09009.

\(^{(2)}\) C. Da Via et al., 3D Silicon Sensors: Design, large area production and quality assurance for the ATLAS IBL pixel detector upgrade. NIMA, vol 694 Dec. 2012.

\(^{(3)}\) S. Parker et al., Increased Speed: 3D silicon Sensors; Fast Current Amplifiers, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 58, NO. 2, APRIL 2011.

Charge deposition distance is decoupled from electrode distance
3D silicon: a “geometric” sensor

\[ \sigma_t^2 = \sigma_{\text{Jitter}}^2 + \sigma_{\text{Time Walk}}^2 + \sigma_{\text{Landau Noise}}^2 + \sigma_{\text{Disuniformity}}^2 + \sigma_{\text{TDC}}^2 \]

Sensor + electronics

\[ \sigma_i = \frac{\sigma_{\text{ii}}}{dV} \]

Sensor layout: geometry

3D has “in-time” \( \delta \)-rays by geometry

Sensor layout is a key for its performance

Electronic drift velocity

Hole drift velocity

Electric field

Weighting field

V_{\text{bias}} = 100 \text{ V}
Simulations and sensor Design
2D-based “Ramo maps”

\[ I_{\text{induced}} = qv \cdot E_w \]
Trench geometry and Tools for full-3D simulation

- Total charge deposit for MIP ≈ 2 fC
- Full depletion @ less than 100 V
- 55x55 µm²: TIMEPIX-compatible pitch

Induced current signal simulation:
1. dE/dx detailed physics for MIP (Geant4)
2. Detailed E field and mobility maps (e.g. TCAD)
3. Induced signal evolution (carrier transport):
   - Sentaurus TCAD: > 30 h* for 1 signal and no secondary particles on a 24-cores machine.
   - (Custom) TCODE: < 1 min for full simulation.
*with very accurate and clever meshing

**TCODE, TIMESPOT CODE for Detector design:**

- A C++ based code with multi-thread capabilities
  (by A. Contu & A. Loi – INFN Cagliari)
- Can be run transparently on CPUs and GPUs, with a speed increase according on the GPU used. On a common gaming laptop GPU the speed gain factor is about x50: from minutes to seconds.
- To be licensed very soon on a GPLv3 license
Signals: 2D on yz cut (TCAD) (simplification for processing-time reasons)

9 days 13 hours
Signals: full-3D (TCODE) (same charge deposit)

7 min 12 s

- X = 27; Y = 10.8
- X = 27; Y = 13.7
- X = 27; Y = 3.6
- X = 27; Y = 4.7
- X = 27; Y = 8.4
- X = 27; Y = 15.5
- X = 27; Y = 19
- X = 27; Y = 23.8
3D-trenched sensor layout

Refer to G. Forcolin’s talk, this conference, for further details

3D test structures

Multi-Pixel Strips

Single Pixel

Technological test devices

Pixel Matrix test structures

TIMEPIX pixel area (for bump-bonding)
• Pixels ROC for 4D tracking require a binary readout (with high resolution in time) and one TDC per pixel (or group of pixels)
• The first approach is to rescale a classic circuit (CMS RD53 style) to our purposes, adding a TDC per pixel

RD53 is a CMOS 65-nm: not enough!  
→ Change of technology node

F/E requirements:
• Keep the resolution below 100 ps rms or (better) as close as possible to sensor intrinsic performance (≈ 20 ps)
CMOS 28-nm F/E scheme

- Compact and low-power design (similar to RD53 65-nm CMOS)
- Sensor-modelled with parameters extracted from simulation
- CSA with DC current compensation and DC voltage setting
- Leading edge discriminator with offset compensation

Use sensor model output (induced current waveforms) for a more precise F/E simulation
Electronics: **CSA**

- Output voltage proportional to input charge
- Constant peaking and falling times for better timing (no CR-RC\(^n\) shaping)
- Low noise
- Krummenacher (active) filter: DC current compensation of input leakage current
- Programmable input MOST current (this prototype)

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### CSA Output

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>199.2</td>
<td>mV/fC</td>
</tr>
<tr>
<td>(T_{pk})</td>
<td>11.86</td>
<td>ns</td>
</tr>
<tr>
<td>(\sigma_N)</td>
<td>2.63</td>
<td>mV</td>
</tr>
<tr>
<td>SNR</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td>ENC</td>
<td>82</td>
<td>e⁻</td>
</tr>
<tr>
<td>Jitter</td>
<td>(\sigma_N/V_r)</td>
<td>55*</td>
</tr>
<tr>
<td>*Consumption</td>
<td>2</td>
<td>µA</td>
</tr>
<tr>
<td>Area (LE D. incl.)</td>
<td>30x15</td>
<td>µm(^2)</td>
</tr>
</tbody>
</table>
**Time resolution:**

- To keep the pixel circuit power budget low enough, 2 µA were allowed to the Front-end.
- Minimum jitter (~25 ps) is reached at 5 µA.
- Power budget can be the limit/constraint.

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**Rise time vs power (as a parameter):**

A different approach will be also tried (next version):

- Current amplifier (lower input impedance)
- → too noisy?
The TDC is based on a “ALL digital fully-synthesizable design” (1)
The DCO is standard-cell based
DCO is enabled only on the occurrence of a hit for lower noise and consumption

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**Specifications**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master Clk</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Resolution (LSB)</td>
<td>50 ps</td>
</tr>
<tr>
<td>Resolution (rms)</td>
<td>15 ps</td>
</tr>
<tr>
<td>NOB</td>
<td>10 bits</td>
</tr>
<tr>
<td>Area</td>
<td>20x15 µm²</td>
</tr>
<tr>
<td>Power (conversion)</td>
<td>1.9 mW</td>
</tr>
<tr>
<td>Power (stand-by)</td>
<td>11 µW</td>
</tr>
</tbody>
</table>

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(1) S. Cadeddu et al., *High Resolution Synthesizable Digitally Controlled Delay Lines*, IEEE TNS vol 62 No. 6, Dec 2015
Main purpose: gain confidence on 28-nm CMOS and test technology performance.

All cells are kept independent and directly accessible from external pins (with a few exceptions) → strongly pad-limited.

Next version (planned for 2019) can “built” the complete pixel ROC

Total area: 1.5x1.5 mm²
Fast readout & Real-time Methods

Information amount generated on front-end is huge \((n \times T\text{bits/s})\)  
\((\text{nr of bits} \times \text{event rate} \times \text{occupancy})\)

1) Triggerless approach
2) Real-time processing to save tracks, not pixel information
3) Need to transfer information for processing
4) Processing information costs less than moving it: is it possible some pre-processing at the front-end level?
Pattern Recognition Methods

Our strategy is to follow the RETINA project approach (1), adding time information into the algorithm structure (2).

**RETINA concept:** The detector geometry defines a set of possible tracks. A possible track corresponds to a cellular unit. Any point “seen” by the detector can be associated a weight, according to its distance from the track hypothesis. The algorithm finds tracks as maxima in weight in the track space.

**TIMESPOT concept:** track points are substituted by stubs.

Each cellular unit can be processed in parallel. The algorithm can also be executed on commercial (powerful) FPGA.

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(1) A. Abba et al., Simulation and performance of an artificial retina for 40 MHz real time track reconstr., JINST 10 (2015) no 03, C03008
(2) Neri N. et al., 4D fast tracking for experiments at high luminosity LHC, JINST 11 (2016) no. 11, C11040
**Stub concept**

Track pattern recognition based on hits with no time information compared to track segments “stubs” with time information.

Points should be ordered on front-end using polar coordinates.

After stub construction, only “in time” points are considered by the algorithm.
Methods (4)

Algorithm steps:

1. Identify stubs i.e. couples of hit in adjacent planes compatible in space and time with tracks from the bunch interaction area;
2. Distribute the stubs in parallel to the Engines;
3. Engines identify tracks from clusters of stubs with similar parameters.
Test on a LHCb-like tracker

Stub algorithm tested by simulation on a LHCb-like vertex detector:

- 12 planes of silicon vertex detector
- Pilup = 40
- 1200 tracks/event
- Interaction region of gaussian shape ($\sigma_z = 5$ cm, $\sigma_t = 167$ ps)

Mis-association vs vertex time resolution

The 4D fast tracking algorithm has also been in FPGA on a custom board (1):

- Two Xilinx Virtex Ultrascale FPGAs
- High-speed optical transceivers → up to 1 Tbps input data rate per FPGA
- One Xilinx Zynq FPGA

(1) M. Petruzzo et al., A novel 4D finding system using precise space and time information of the hit, TWEPP 2018
A lot of (stimulating) work, besides algorithm implementation, is in front of us at the read-out level:

Connectivity and, inter-connectivity in particular, appear to be the real bottle neck:

• In order to minimize remote data processing, can we envisage to built in-time-stubs directly on front end?
• Is it possible an intermediate level of connectivity and intelligence?
• 3D inter-connections?
• Technically possible?
• Too expensive?

Kind-of brain cortex for pattern recognition on front-end?
Timing is a mandatory requirement for the next generation of tracking systems, starting from the next decade (high lumi LHC and future colliders).

Besides timing, other requirements have to be satisfied:
- Operation under extremely high radiation levels
- Processing of huge amount of information (pre-processing at the front-end level)
- Extremely fast read-out and/or front-end pre-processing
- Real time tracking

The TIMESPOT project has a system-level approach, starting from state-of-the-art expertise in different fields. Its aim is to trace a possible path towards the solution of this experimental challenge.

First results after less than 1 year of activity have been illustrated.

Future colliders require radically new ideas on detectors and detector systems.
Many thanks to all the TIMESPOT team members

Special thanks to
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Giulio Forcolin (INFN TIFPA)
Providing many of the figures used in this talk

...And thank you for your kind attention!