Beam test results of an SOI monolithic pixel sensor SOFIST for the ILC vertex detector

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SOI Pixel Detector

- **Monolithic pixel detector based on Silicon-On-Insulator**
  - 0.2 μm FD-SOI CMOS process by Lapis Semiconductor Co. Ltd

- **SOI Pixel sensor features**
  - **Monolithic structure: (No bumps)**
    - Small, highly integrated pixel circuit
    - Low material budget
  - **CMOS circuit fabricated on buried oxide layer (BOX)**
    - Low capacitance: High speed, Low power circuit
  - **High resistivity substrate**
    - Fully depleted sensor
  - **Double SOI structure: Additional silicon layer in the BOX**
    - Crosstalk reduction between circuit and sensor layers.
    - High radiation tolerance (~1MGy): compensation of trapped holes in the BOX
International Linear Collider: Detector system

- ILC experiment: e+,e- linear collider
  - Precise measurement of Higgs boson, Search for BSM physics
  - Need vertex detector with high accuracy spatial resolution for reconstructing the physics events
- Development of new pixel detector optimized for ILC experiment
  - Realizing fine pixel detector with SOI technology
Vertex detector requirement

- **Positon resolution**: < 3 um
- **Material thickness**: < 100 um Si thickness
  - Reducing multiple scattering
  - Low power (for reducing cooling system): 50 mW/cm²
- **Time resolution**: ~ 554 ns bunch interval
  - Beam bunch identification
- **Detector occupancy (hit rate)**: 1312 bunches in one train
  - Multiple hits in one pixel
- **Data transfer**: 200 ms beam train interval
- **Radiation Hardness**:
  - TID: 1 kGy/year
  - NIEL: 1011 1MeV neq/cm²/year
Specifications of new SOI detector

- Specification of new SOI sensor optimized for ILC vertex detector
  - Position resolution: < 3 μm
    - Pixel size: 20 × 20 μm²
    - Calculate weighted center of charges → Recording charge signal in each pixel
  - Time resolution: ~554 ns (Beam bunch interval)
    - Identify collision bunches of hit events → Recording hit timestamp
  - Multiple hits in one pixel
    - Store hit informations during one beam train → Implementing multiple memories
  - Data transfer: 200 ms
    - High speed data processing → On-chip ADC, Digital circuits for data sparsification

Design high-functional SOI sensor with measuring both hit-position and time.
SOFIST: Pixel design

- SOFIST: SOI sensor for Fine measurement space and time

- SOFIST Pixel function
  - Pre-amplifier: CSA
  - Comparator: Hit-signal discrimination
  - Shift register: Memory sequencer
  - Multiple Analog-signal memories
    - Record signal amplitude
  - Multiple Timestamp memories
    - Record hit timing by holding ramp voltage
# SOFIST: chip design

<table>
<thead>
<tr>
<th></th>
<th>SOFIST</th>
<th>Ver.1</th>
<th>Ver.2</th>
<th>Ver.3</th>
<th>Ver.4 (3D)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pixel circuit</strong></td>
<td>Analog signal</td>
<td>Hit detection \nTimestamp</td>
<td>Full functionality</td>
<td>Full functionality \n3D stacking</td>
<td></td>
</tr>
<tr>
<td><strong>Chip size (mm)</strong></td>
<td>2.9 × 2.9</td>
<td>4.45 × 4.45</td>
<td>6.0 × 6.0</td>
<td>4.45 × 4.45</td>
<td></td>
</tr>
<tr>
<td><strong>Pixel size (μm)</strong></td>
<td>20 × 20</td>
<td>25 × 25</td>
<td>30 × 30</td>
<td>20 × 20</td>
<td></td>
</tr>
<tr>
<td><strong>Functions</strong></td>
<td>Pre-amplifier \nAnalog signal memory</td>
<td>Pre-amplifier \nComparator \nShift-register \nAnalog signal memory (2hits) \nor \nTimestamp memory (2hits)</td>
<td>Pre-amplifier \nComparator \nShift-register \nAnalog signal memory (3hits) \nTimestamp memory (3hits)</td>
<td>Pre-amplifier \nComparator \nShift-register \nAnalog signal memory (3hits) \nTimestamp memory (3hits)</td>
<td></td>
</tr>
</tbody>
</table>
SOFIST Ver.1

- Pixel circuit
  - Pixel size: $20 \times 20 \, \mu m^2$
  - Pre-amplifier: Gain = 32 $\mu V/e-$
  - Analog signal memories: 2 Hits
- On-chip: 8 bit column-parallel ADC
- Sensor layer: 500 $\mu$m thickness

![Pixel layout](image-url)
SOFIST Ver.1: Test result

- Beam test @ Fermilab Test beam Facility (Jan. 2017)
  - Proton beam: 120 GeV
  - Sensor bias: 130 V, 15 V (Depletion = 500, 200 μm)
  - Readout: external ADC (12 bit), on-chip ADC (8 bit)

- Signal-to-noise
  - Summing 5 x 5 pixels around hit
  - Pixel noise: ~1.4 ADU (External ADC (12 bit))

- Position resolution
  - Calculate weighted center of charges (5 × 5 pixels).
  - Difference between SOFIST hit and reconstructed track

- Readout, Sensor depletion
  - 12 bit ADC, 500 μm (Full-depletion)
  - 12 bit ADC, 200 μm
  - 8 bit ADC (On-chip), 500 μm

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**Signal spectrum**

- Entries: 19110
- Mean: 478
- Std Dev: 147.5
- $\chi^2$/ndf: 1053/67
- Constant: 5369 ± 63.4
- MPV: 421.4 ± 0.6
- Sigma: 33.36 ± 0.32

S/N ~ 300
~ 124

**Residual distribution**

- Entries: 2401
- Mean: 0.1677
- Std Dev: 2.721
- $\chi^2$/ndf: 12.58/9
- Constant: 7.6 ± 227.7
- Mean: 0.0386 ± 0.1668
- Sigma: 0.035 ± 1.367

Sigma = 1.37 μm
= 1.33 μm
= 1.49 μm
SOFIST Ver.2

- Pixel circuit
  - Pixel size: 25 × 25 μm²
  - In-pixel comparator and 2-stage shift-register
  - Analog signal or Timestamp memories: 2 Hits
- Sensor layer: Thinned to 65 μm

Pixel layout

![Pixel layout diagram](image.png)
SOFIST Ver.2: Pixel operation

- Analog signal pixel: Pixel response by test pulse input
  - Operation of in-pixel comparator and Shift-register (memory sequencer)

- Latching hit-signal amplitude by comparator
- Storing two hit signals in two memories by shift-register
SOFIST Ver.2: Pixel operation

- Timestamp pixel: Pixel response by test pulse input
- Calibration of analog timestamp

![Timestamp pixel output](image)

![Timestamp response graph](image)

![Timestamp fluctuation graph](image)

<table>
<thead>
<tr>
<th>Entries</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>249.6</td>
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<tr>
<td>RMS</td>
<td>0.9257</td>
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<tr>
<td>$\chi^2$/ndf</td>
<td>27.03/9</td>
</tr>
<tr>
<td>Constant</td>
<td>433.1 x 11.4</td>
</tr>
<tr>
<td>Mean</td>
<td>249.5 ± 0.0</td>
</tr>
<tr>
<td>Sigma</td>
<td>0.9094 ± 0.0124</td>
</tr>
</tbody>
</table>

Sigma ~ 1 μs
SOFIST Ver.2: Test result

• Beam test @ Fermilab Test beam Facility (Feb. 2018)
  • Proton beam: 120 GeV
  • The data analysis is still underway.

SOFIST Ver.2
Pixel size: 25 × 25 μm²
Active area: 2.0 × 1.6 mm²

INTPIX

MPPC (Trigger detector)

30 mm

SOFIST Ver.2

INTPIX

INTPIX4 (SOIPIX): Tracker
Pixel size: 17 × 17 μm²
Active area: 14.1 × 8.7 mm²

Ver.2 chip Readout board

Proton beam
Beam test result

- Hit detection and time-stamping results of proton beams

**Beam test setup**

**Timestamp difference**

Sigma = 2.19 μs
Intrinsic resolution: Sigma/√2 ~ 1.55 μs
SOFIST Ver.3

- Pixel circuit
  - Pixel size: 30 × 30 μm²
  - In-pixel comparator and 2-stage shift-register
  - Analog signal and Timestamp memories: 3 Hits
- Sensor layer: Thinned to 65 μm
Ver.3 test result

• Pixel response by β-ray (Sr-90)
  • Analog signal memory: charge deposition in each pixel
  • Timestamp memory: detection timing of each β-ray track

Next beam test is planned at February, 2019
Test results and issues

• Position resolution: $< 3 \mu m$
  
  • **SOFIST Ver.1 achieved 1.33 $\mu m$ resolution.**
  
  • Pixel size: $20 \times 20 \mu m^2$, Sensor thickness: 200 $\mu m$

• Time resolution: $\sim 554$ ns
  
  • **SOFIST Ver.2 timestamp has 1.55 $\mu s$ resolution (Preliminary).**
    
    $\rightarrow$ More precise memory and low noise circuits.

• Low material budget: $< 100 \mu m$ sensor and low power circuit.
  
  • **Hit signal can be detected with 65 $\mu m$ sensor.** The position resolution with 65 $\mu m$ is under analyzing.
  
  • Pixel circuit has high power consumption ($\sim 500$ mW/cm$^2$).
    
    $\rightarrow$ Design/Operate lower power pixel.

• Detector occupancy (hit rate): Multiple pixel memories
  
  • **Ver.3 pixel has 3 analog and timestamp memories.** The pixel size became 30 $\mu m$ pitch.
    
    $\rightarrow$ Small and high-integrated pixel by 3D stacking technology.
3D stacking technology

- SOI pixel detector with 3D stacking technology
  - Connect the upper and lower chip by micro-bump: Tohoku MicroTec Co., Ltd.
  - Pixel size reduction: $30 \times 30 \, \mu m^2 \rightarrow 20 \times 20 \, \mu m^2$

**3D-SOI chip: cross-section**

Upper pixel (Inverted)
- Shift-register
- Analog memory x3
- Timestamp x3

**Ver.4: Pixel layout**

- Pre-amp
- Comparator
3D-stacking technology

- Bump production on SOFIST Ver.4
  - SOFIST Ver.4 will be shipped in 2018.
Summary

• SOI pixel detector SOFIST is designed for ILC vertex detector.
  • Design high-functional SOI sensor with measuring both hit-position and time.

• SOFIST has been tested in FermiLab beam
  • SOFIST Ver.1: 20 μm pixel, Depletion layer: 200 μm
    • Position resolution: 1.33 μm
  • SOFIST Ver.2: 25 μm pixel, Depletion layer: 65 μm
    • Time resolution: ~1.55 μs
  • SOFIST Ver.3: 30μm pixel with full-functionality
    • To be tested at FermiLab

• SOFIST Ver.4: 20μm pixel, 3D stacked sensor
  • Fabrication is underway. Stacked chip will be shipped in 2018.
Backup
3D stacking: Micro bump

- 3D integration of SOI sensor chip
  - Micro-bumps are developed by photolithography process
  - Bump size: 3.5μmφ, Minimum pitch: 7μm
  - Connection yield: > 99.5 %
3D stacking: stack process

1. Bump formation
(Micro bumps are formed on both chips.)

2. Stacking and pressing 2 chips
Inducing glue between chips

3. Removing upper substrate
Forming IO pads.