MALTA: an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade.

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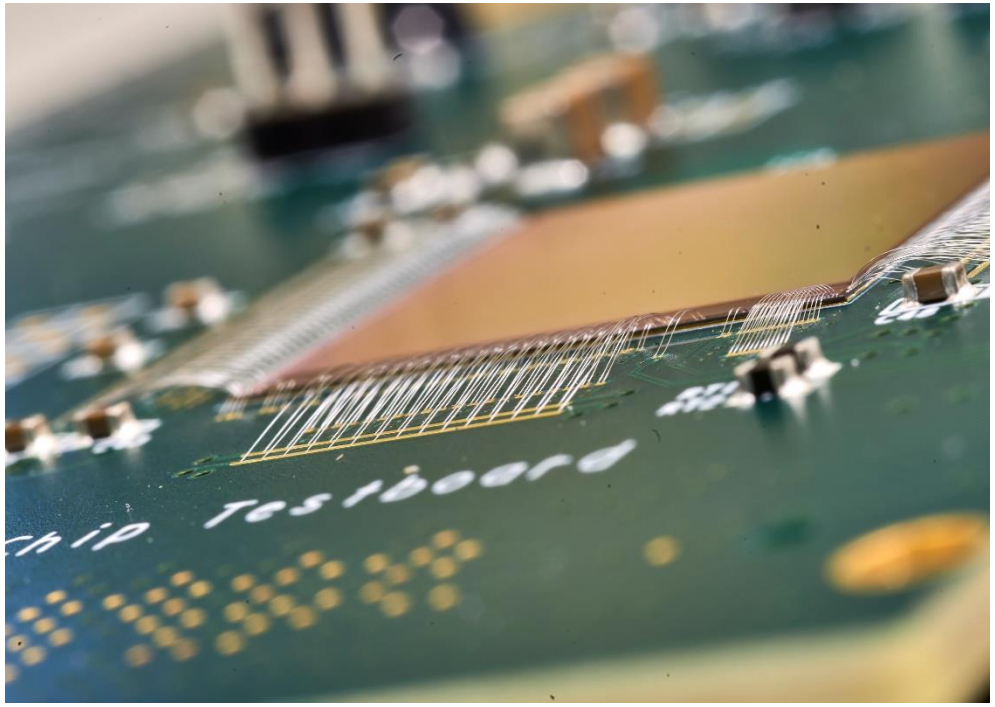
Outline

1. CMOS development for ATLAS ITk
   - TowerJazz 180nm technology
2. MALTA chip
   - Datapath: From the pixel to the output
   - Measurements results
   - Module design
3. Parallel R&D on MALTA
4. Conclusions



CMOS considered for ATLAS ITk

Outermost layer of ITk Pixel Barrel

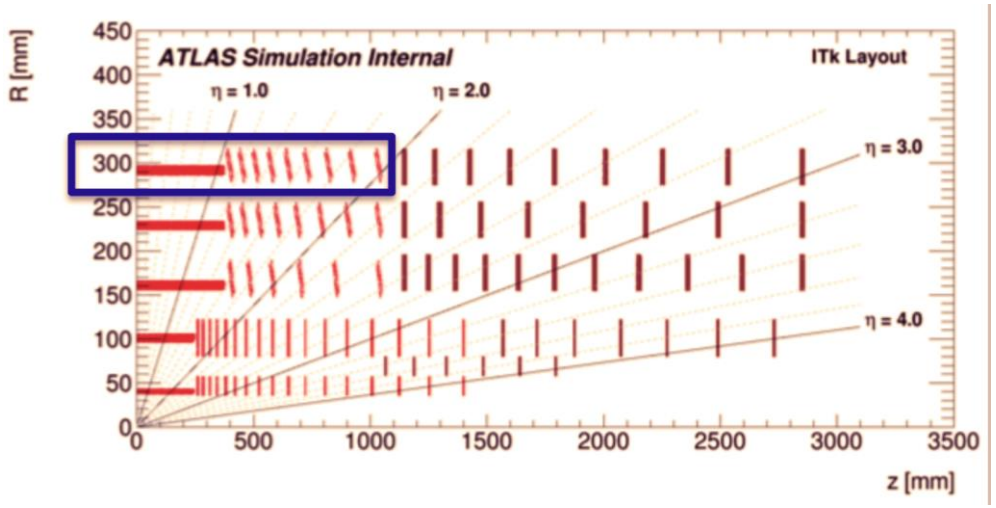
- 2016 quad modules
- 3m^2 (~45% of outer barrel layers)

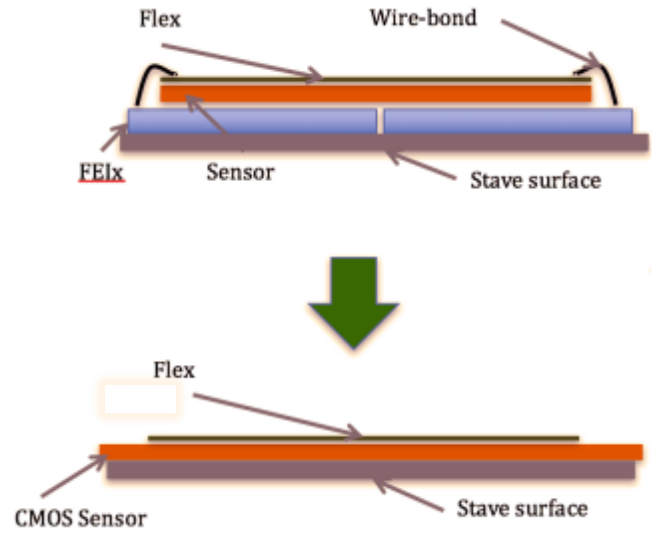
For 4000 fb-1 integrated luminosity

- TID = 80Mrad
- NIEL 1.5 x 10^{15} neq/cm^2

Monolithic CMOS sensors are considered as option for the outermost layer

- Saves bump bonding for ~45% of outer barrel system
- Substantial cost reduction and reduced module assembly time
- Requires “Drop-In” module compatibility to hybrid module





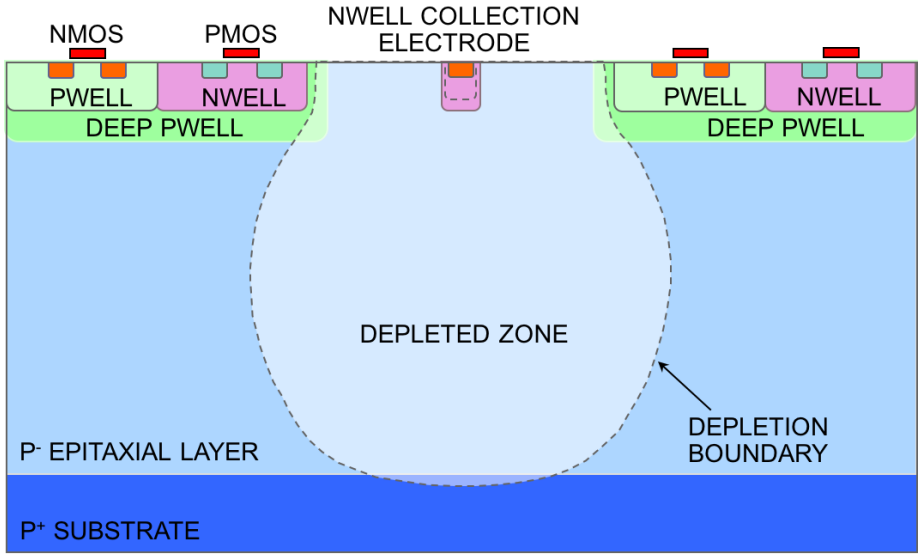
Sensors in the TowerJazz 180 nm technology

Standard Process

Small collection electrode design with high resistivity (> 1 kΩ cm) p-type epitaxial layer (25 µm → MIP ~1500 e^-)

Deep p-well shielding n-well to allow **full CMOS**

Reverse bias (~6 V): reduce input capacitance and increase depletion volume

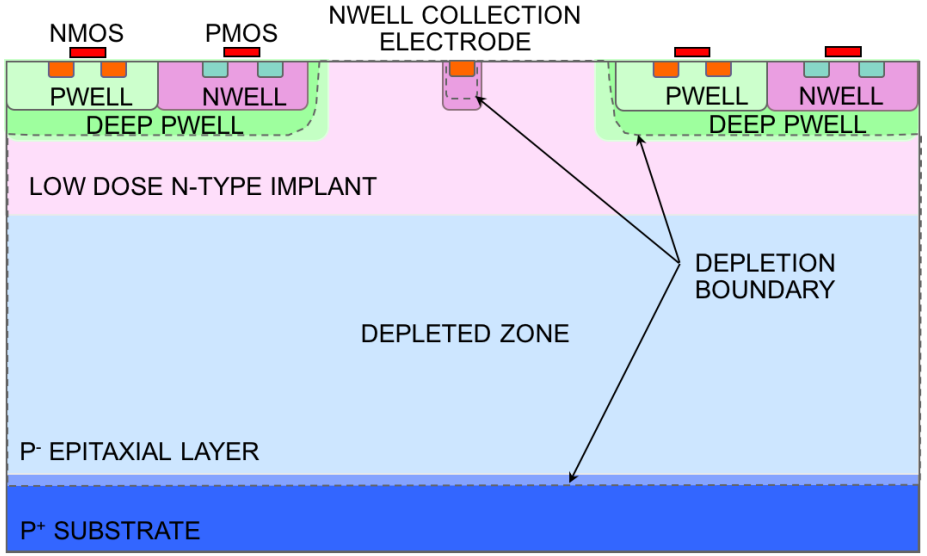


Modified Process

Adding a **planar n-type layer** to improve depletion under the deep p-well near the pixel edges

A fully depleted epitaxial layer results in faster charge collection and **better radiation tolerance**

No circuit or layout changes required



W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

Sensors in the TowerJazz 180 nm technology

Standard Process

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Deep p-well shielding n-well to allow **full CMOS**

Reverse bias increase depl

Modified Process

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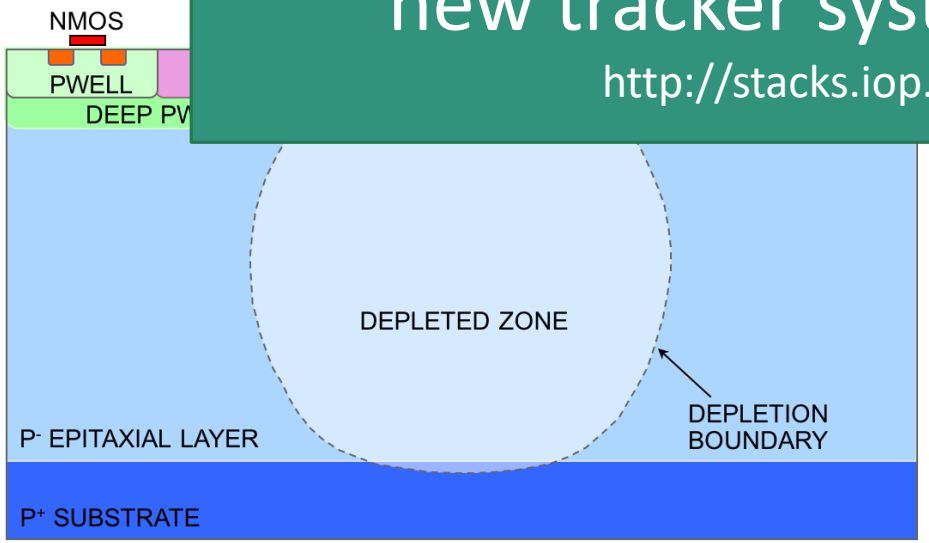
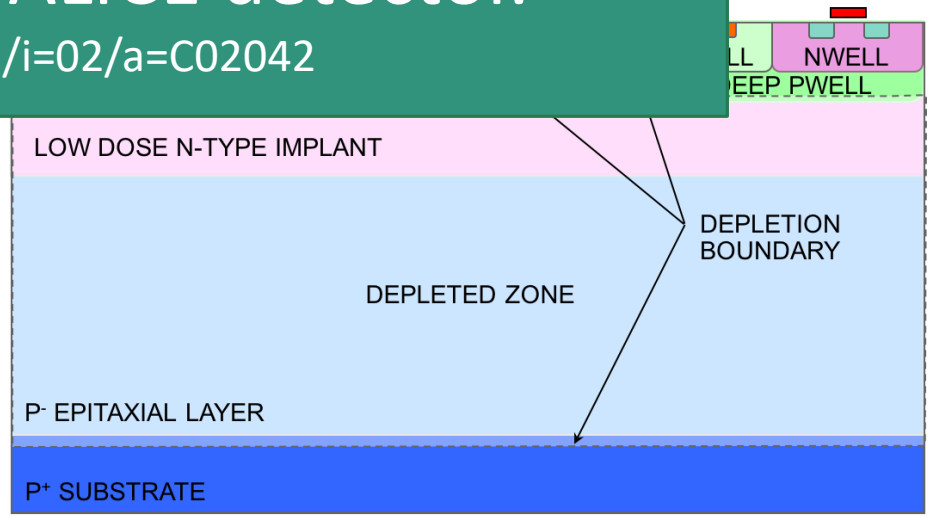
A fully depleted epitaxial layer results in faster charge collection and **better radiation tolerance**

ALPIDE (standard process) will be installed in the new tracker system of the ALICE detector.

http://stacks.iop.org/1748-0221/11/i=02/a=C02042





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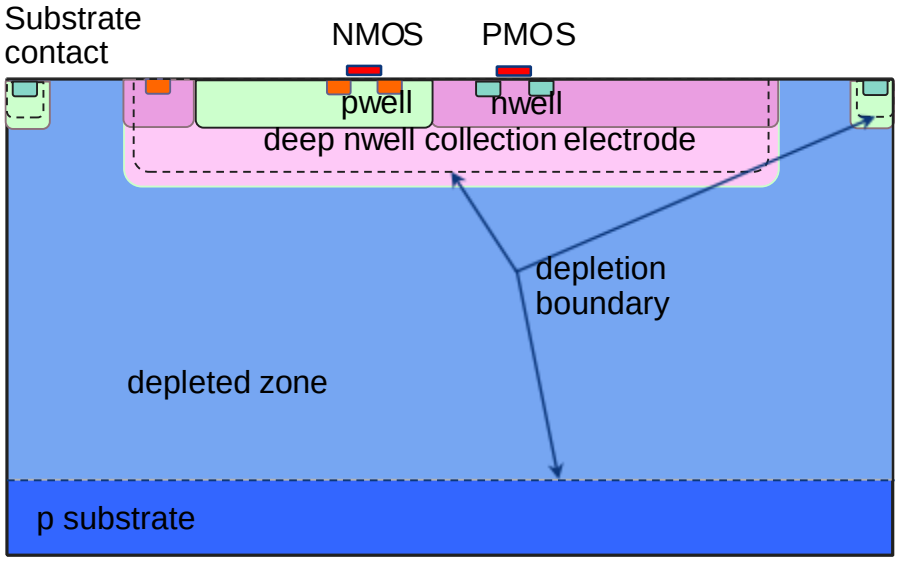
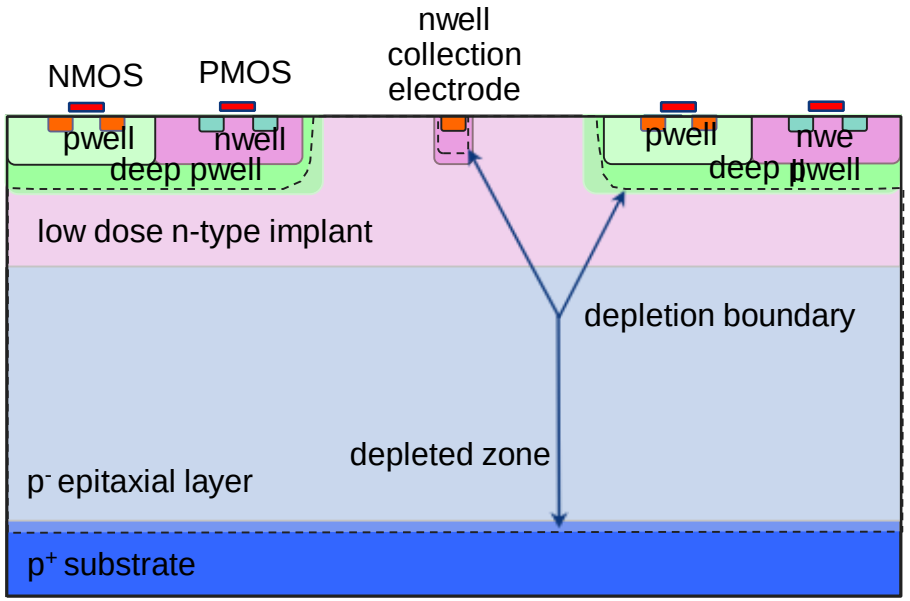
Large vs Small collection electrode





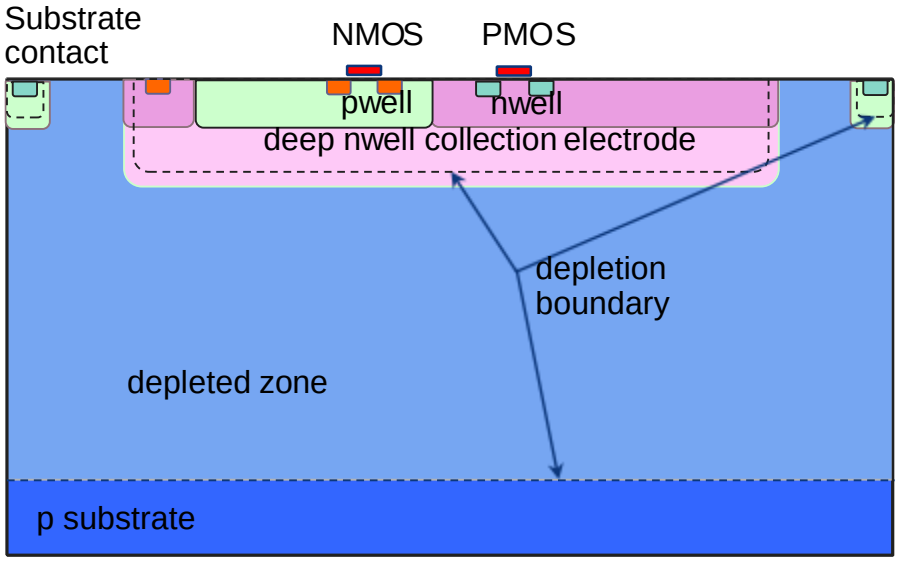
Large collection electrode (HV-CMOS)

- Large capacitance
- Higher power
- Electronics in the input well, signal coupling
- Practically uniform field
- Very high radiation tolerance

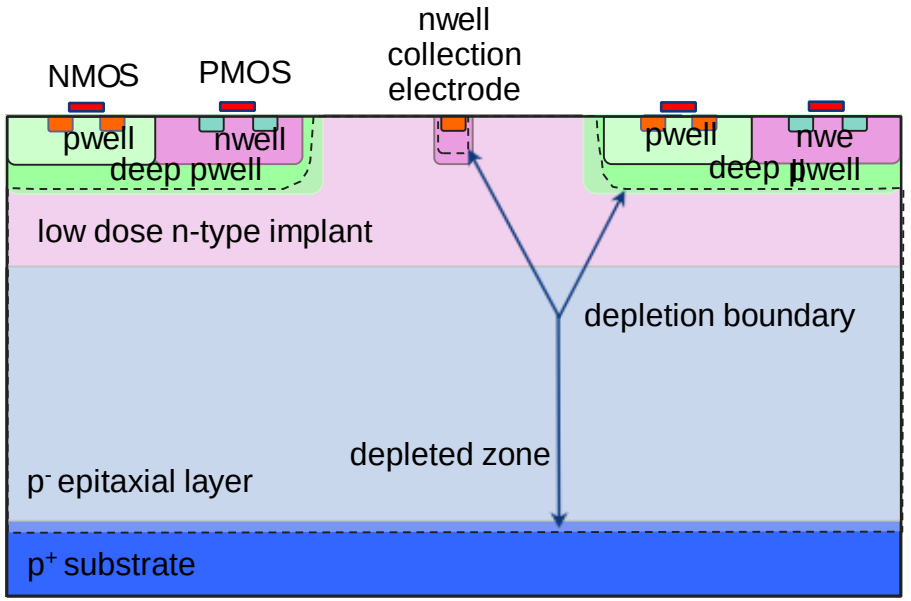
Small collection electrode (TJ)

- Small capacitance
- Lower power
- Less prone to coupling
- Process modification for full depletion and radiation tolerance increase

Large vs Small collection electrode



Large collection electrode (HV-CMOS)



Small collection electrode (TJ)

Power/Chip [mW]	TJ Asynch.	TJ Synch.	Large Electr. Synch.
Matrix Analog	238	238	1000
Matrix Digital	12	240	80
Total Expected	514	703	1305

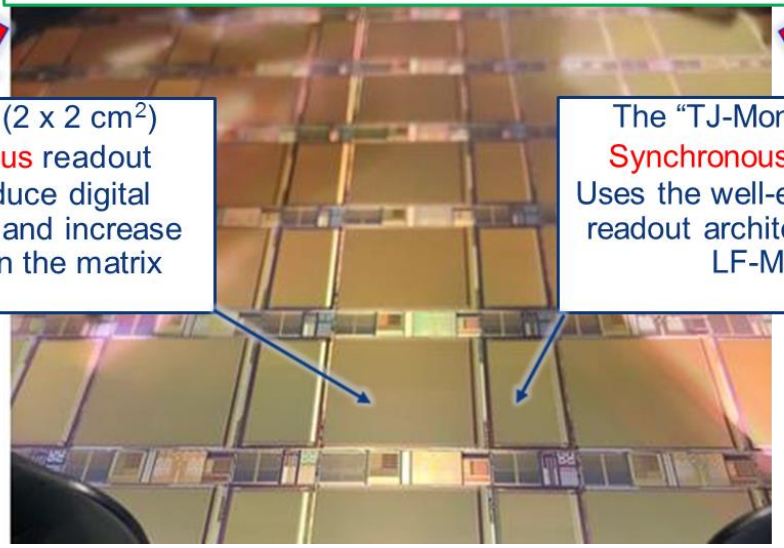
TJ 2017 submission

Measurement results show improved non-ionizing radiation tolerance for sensors manufactured using the modified process

⇩

Analog front-end optimized for timing, based on ALPIDE

Design of two large scale demonstrators to match ATLAS specifications for outer pixel layers
Collaboration CERN – Uni. Bonn



The "MALTA" chip (2 x 2 cm^2)
Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix

The "TJ-Monopix" chip (2 x 1 cm^2)
Synchronous readout architecture.
Uses the well-established column drain readout architecture (experience from LF-Monopix design)

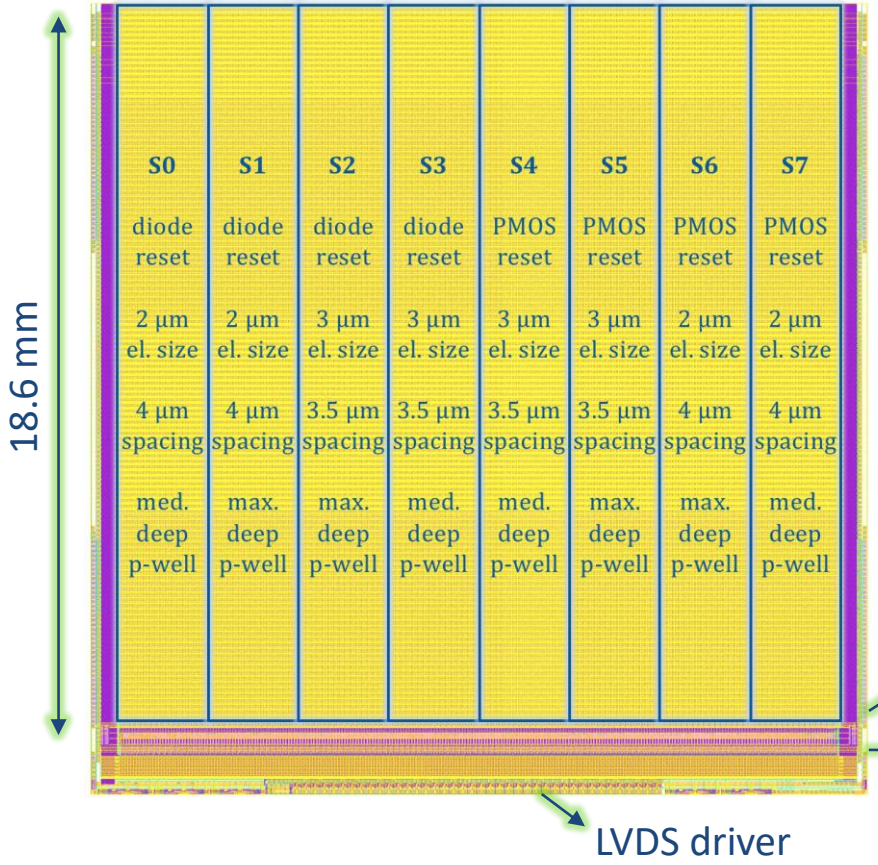
Talk on TJ-Monopix

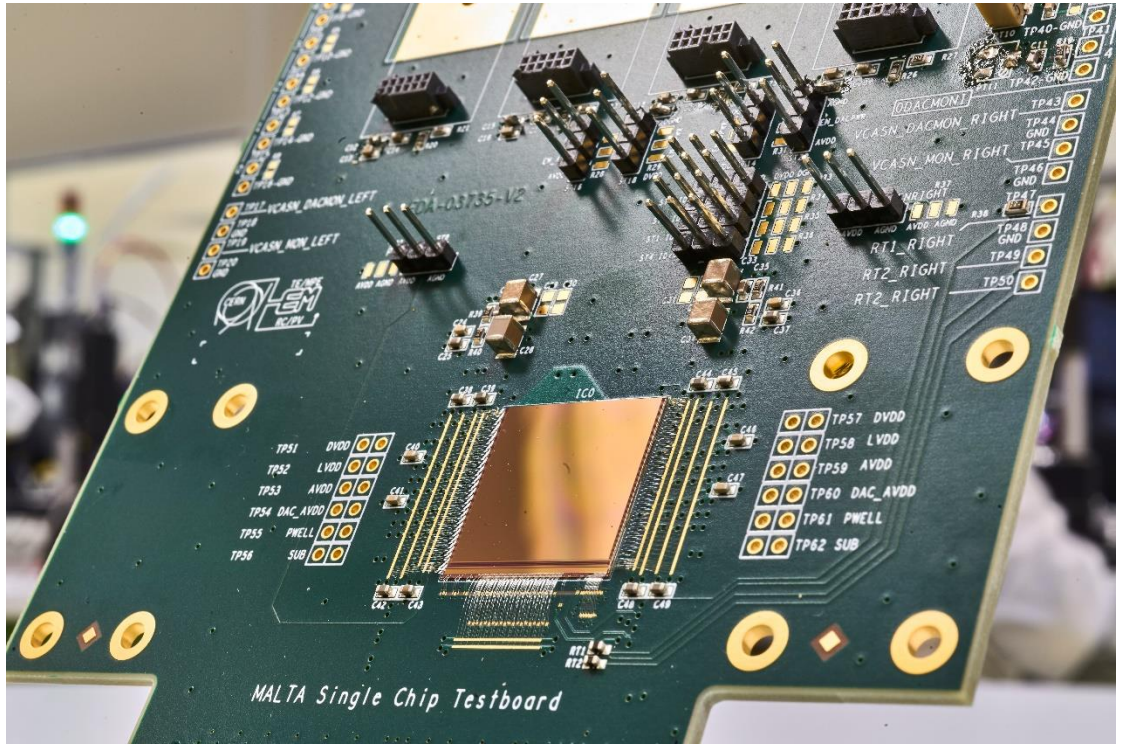
Thu 13/12 12:00 *I. D. Caicedo Sierra*

R&D status of the Monopix chips: Depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS Inner Tracker upgrade

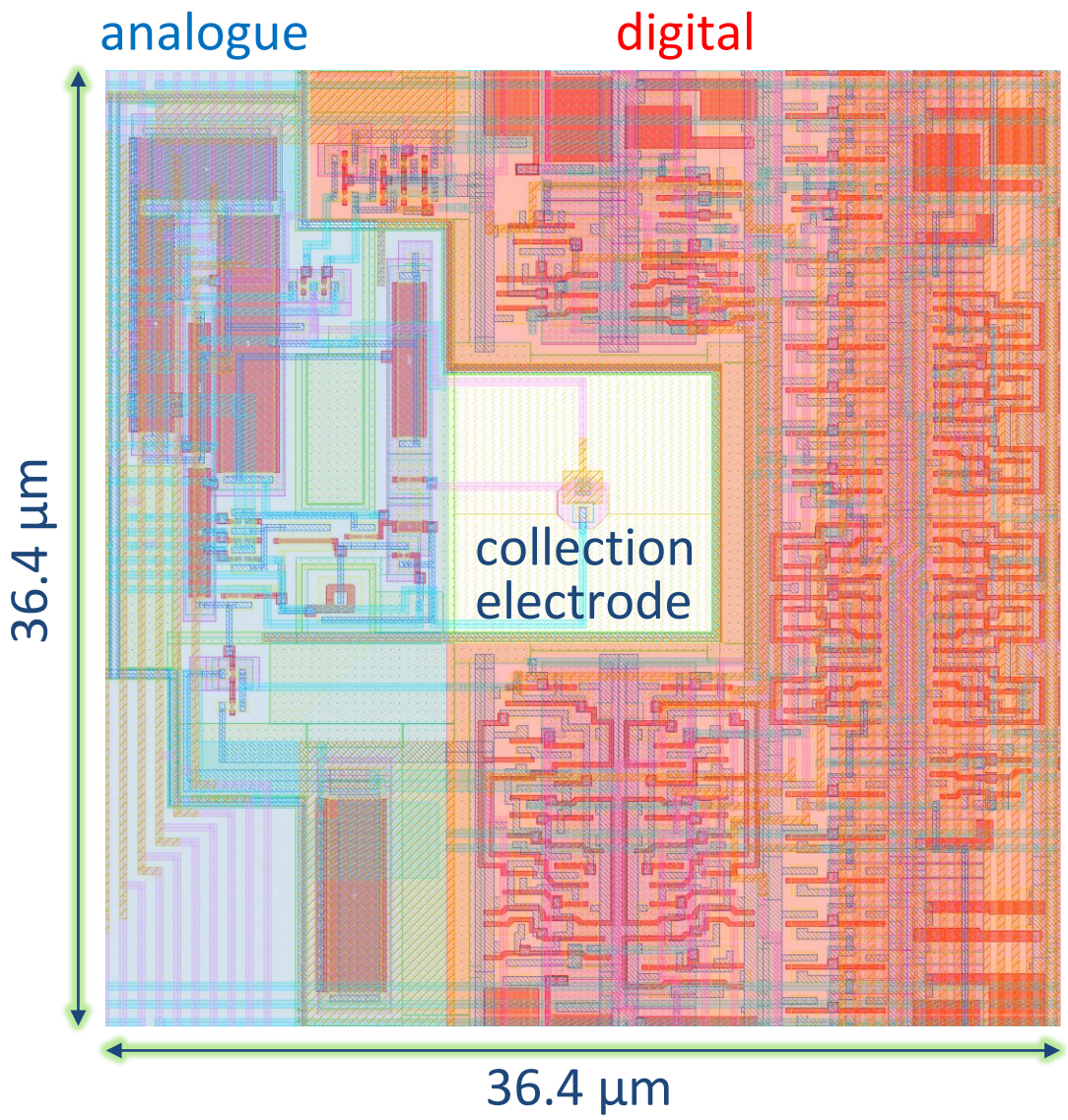
MALTA: Monolithic pixel detector from ALICE to ATLAS

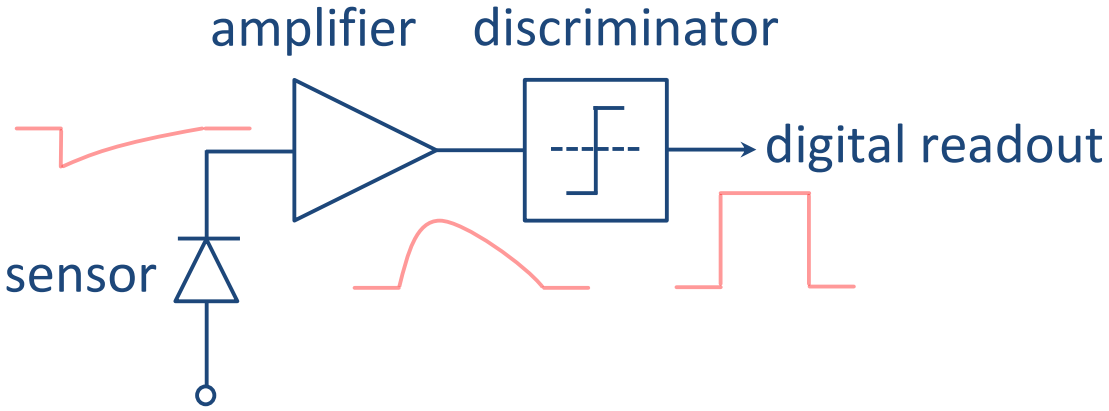
The 512x512 pixel - 8 sectors
The front-end is a development from the ALPIDE one.
Design based on a **low-power analogue front-end** and a novel **asynchronous architecture** to read out the pixel matrix





The MALTA pixel





- 2-3 um collection electrode → small input capacitance
- 3.4 – 4 um separation between electrode and electronics → low cross talk
- 1 uW/pixel analog power (75 mW/cm²)
- 10 mW/cm² digital power @ layer4

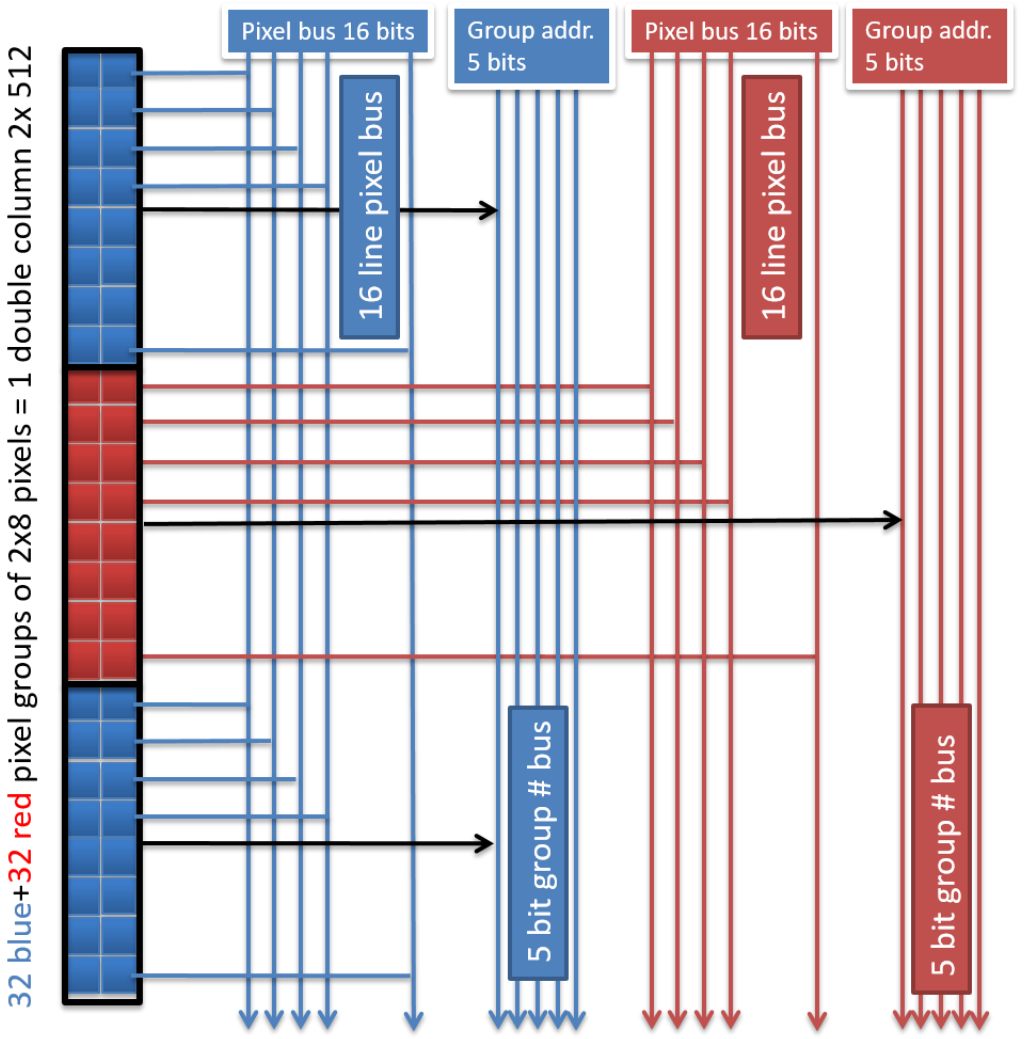
Sensor and analogue front-end (shaper-amplifier and discriminator) shielded from digital part to **minimise crosstalk**

Time walk information preserved

Digital readout architecture

- Front-end output injected into double-column digital readout logic
- Hits are stored using in-pixel flip-flops and transmitted asynchronously over high-speed buses to the end-of-column logic (digital periphery)
- **No clock distribution over the active matrix** – reduces power consumption!

- Double-column divided into groups of 2x8 pixels (“red” and “blue”)
- Buses shared by all groups of the same colour in the double-column, total of 64 groups
- Each hit is hence represented by a 40 bit word, **asynchronously transmitted via parallel LVDS drivers**



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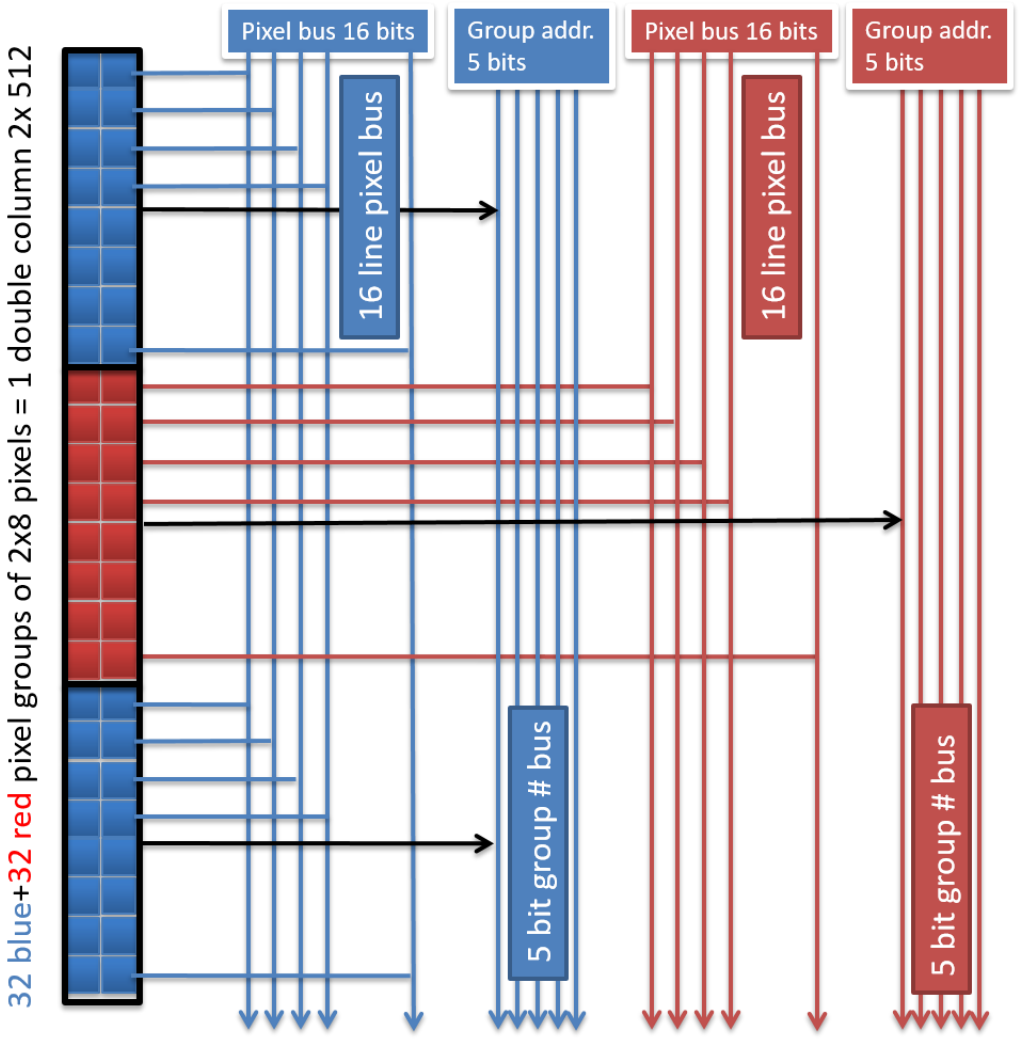
Power/Chip [mW]	TJ Asynchronous	TJ Synchronous
Matrix Analog	238	238
Matrix Digital	12	240
Total Expected	514	703

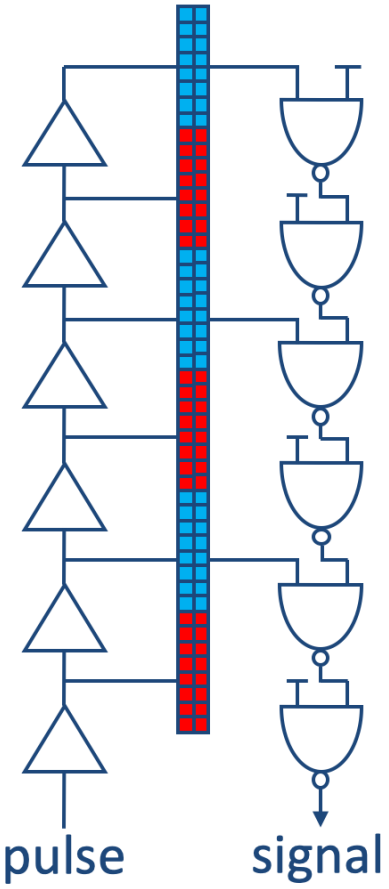
Factor 20 for matrix digital power

More than 25% of total power

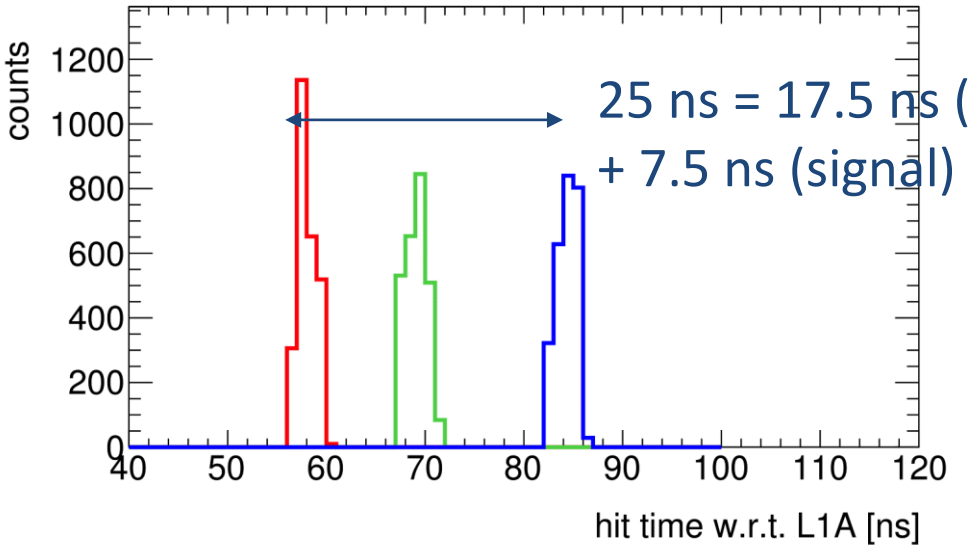


Asynchronous readout architecture

Hit signals from the pixels are buffered and arrive at the end-of-column with a maximum propagation delay of **~7.5 ns**

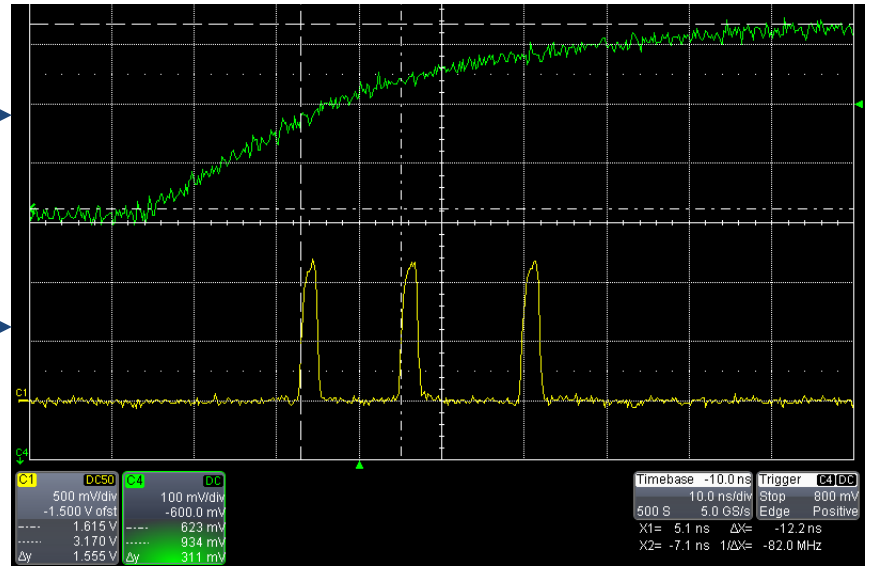


(measured by pulsing pixels on top, middle and bottom of the column)



analogue output of one pulsed pixel

reference signal



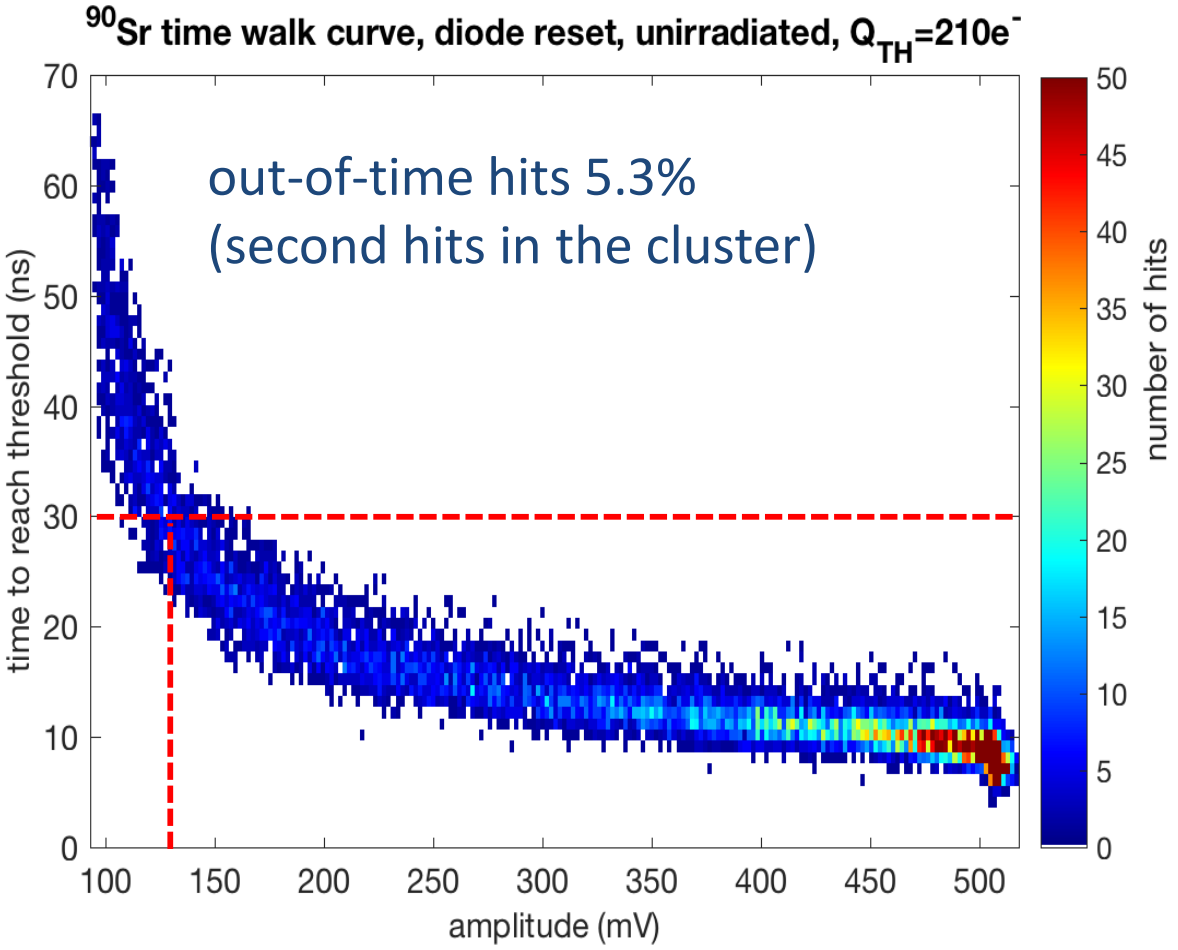
Analogue front-end timing measurements

	Outer Layer	Inner Layer
Required Time Res. $[ns]$	25	25
Particle Rate$[MHz/mm^2]$	1	30
Fluence $[n_{eq}/cm^2]$	10^{15}	10^{16}
Ion. Dose $[Mrad]$	50	1000

Time walk measurement performed with a ^{90}Sr source using special pixels to monitor the analogue output

With a threshold of 210 e^- the **in-time threshold** is **300 e^-** (20% of MIP charge)

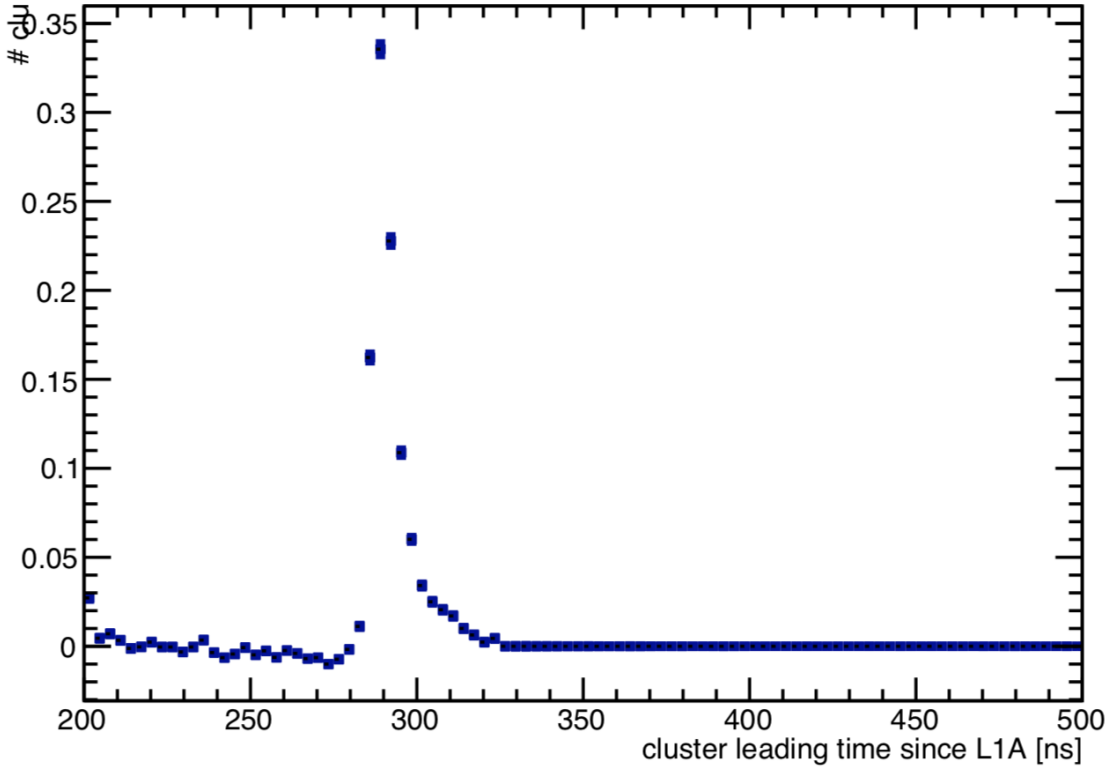
Out-of-time hits due to charge sharing (measurement done on a single pixel)



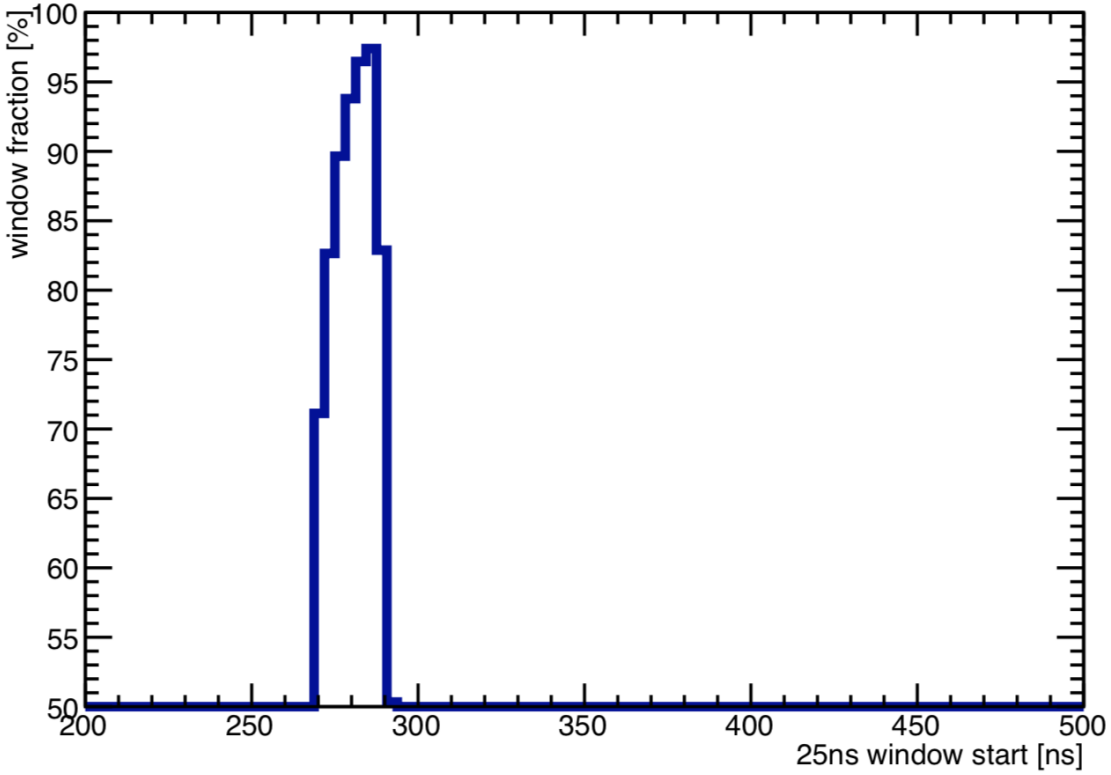
in-time threshold 130mV = 300 e^-

Front-end and readout timing measurements

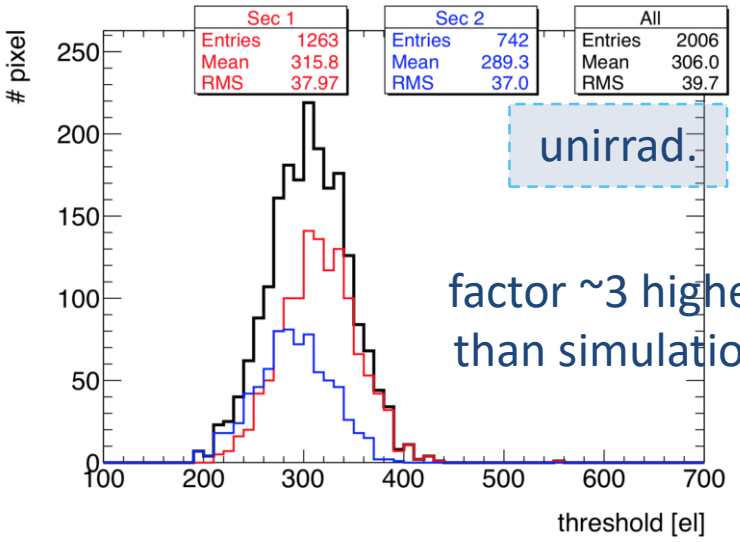
Time walk can also be obtained by measuring the delay of digital output signals with respect to a fast trigger (scintillator)

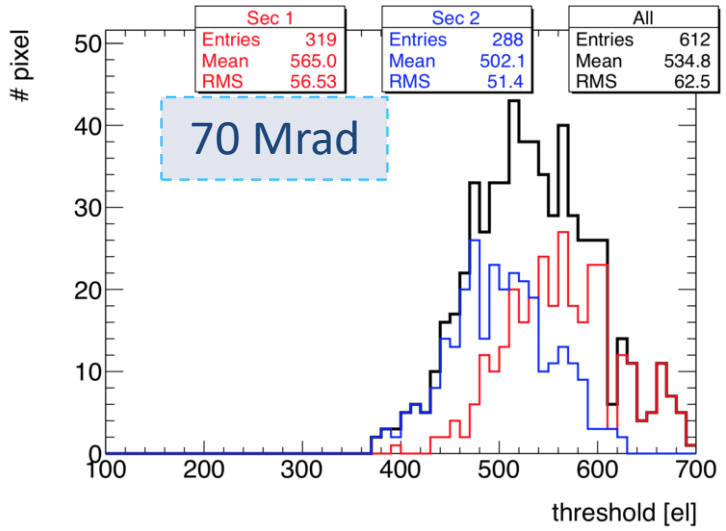


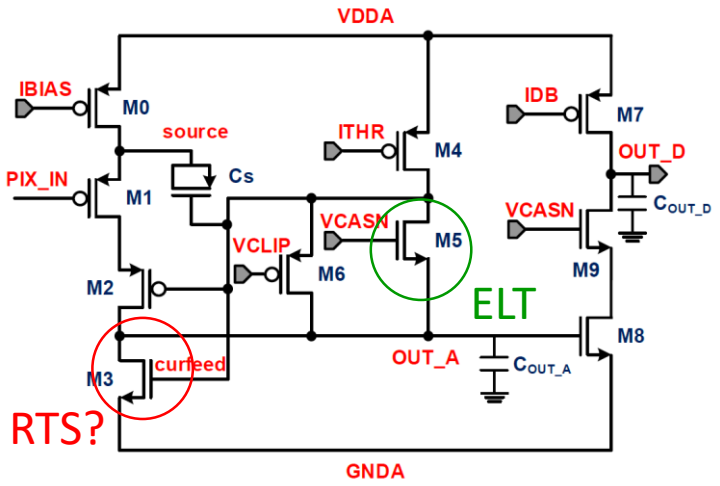
In-time efficiency for **leading signals** in clusters reaches **98%** with a 300 e^- threshold (no correction for the **7.5 ns** propagation delay down the column)

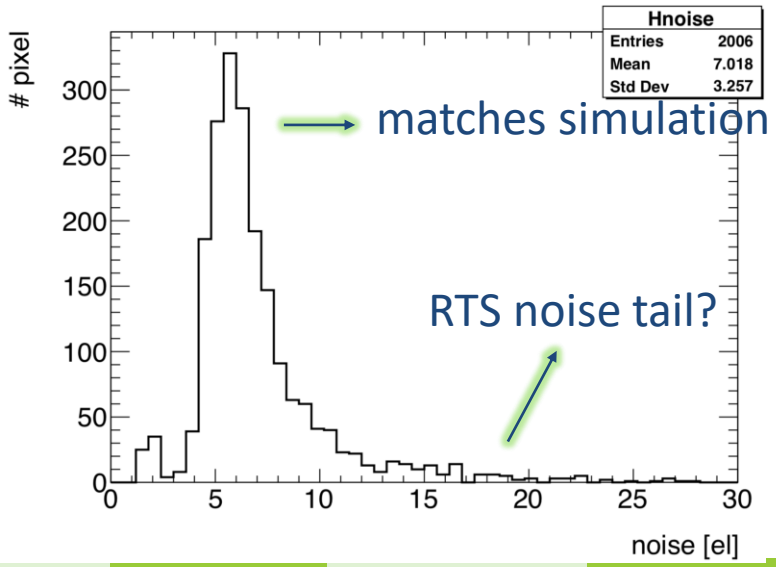


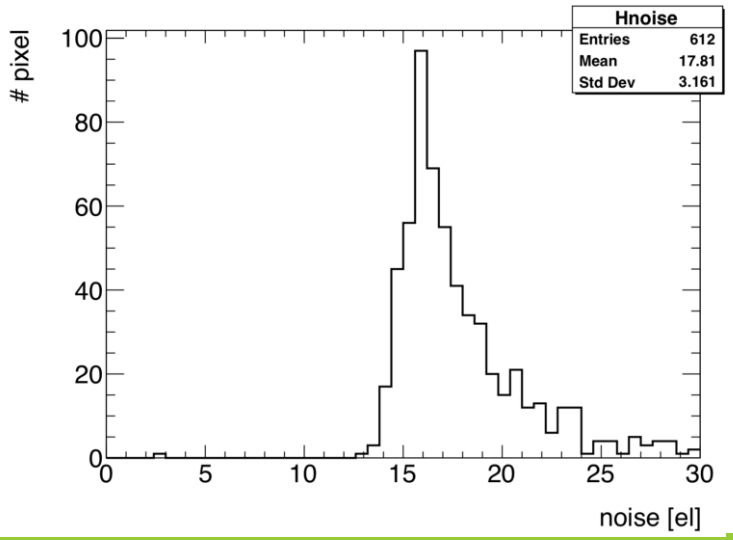
Thres. dispersion and noise before and after TID



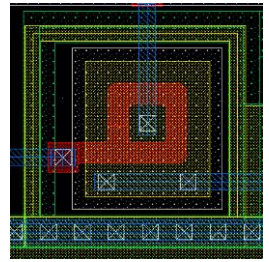








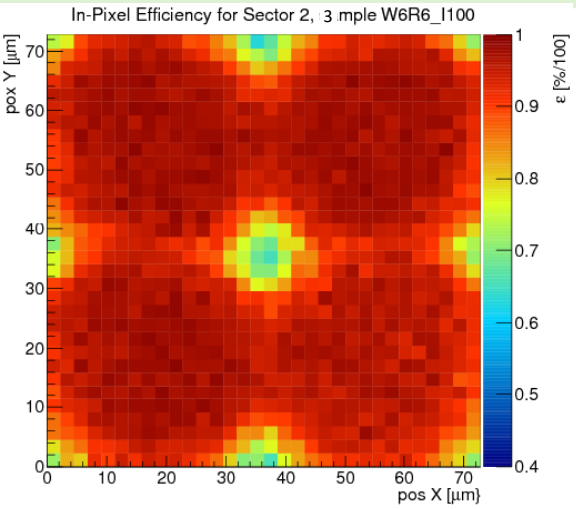
- Front-end still operational after 70 Mrad due to ELT in sensitive branch

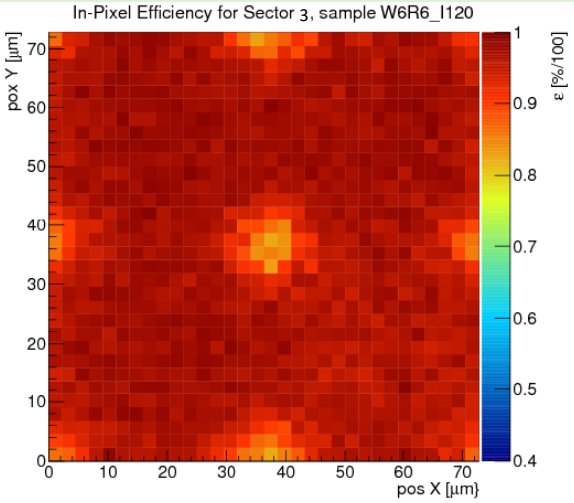


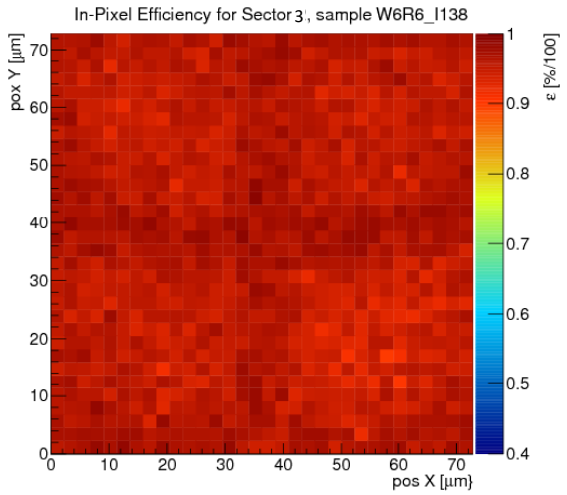
- Increase in threshold spread and noise under investigation

PIXEL 2018 - TAIPEI

Efficiency in testbeam before and after irradiation







Unirradiated: lowering the threshold gives full efficiency

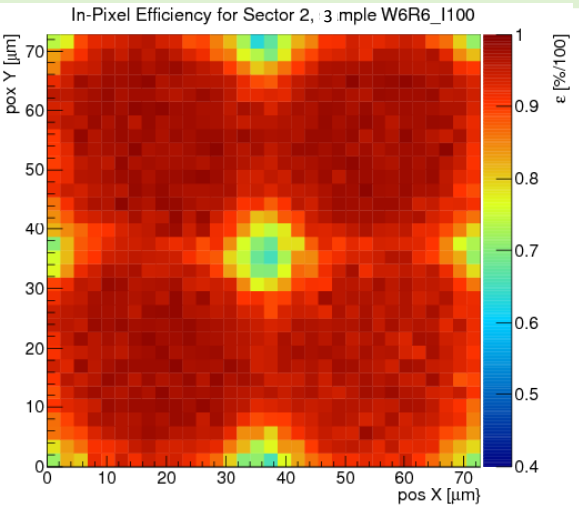
Decreasing threshold from ~600 e^- to ~250 e^- (unirrad.)

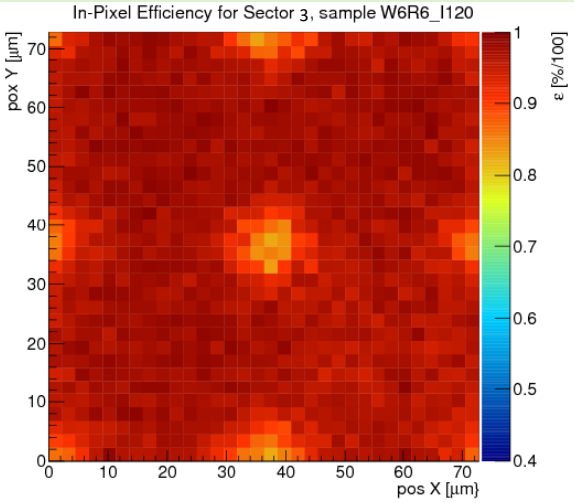
3 3

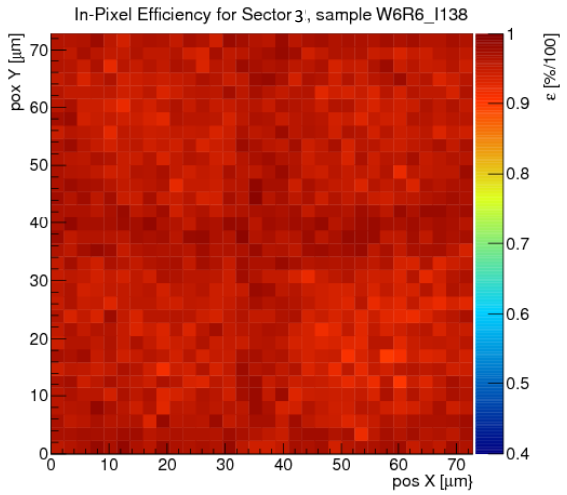
Cannot go lower with threshold because of RTS noise and masking issue

Solution for both under study.

Efficiency in testbeam before and after irradiation

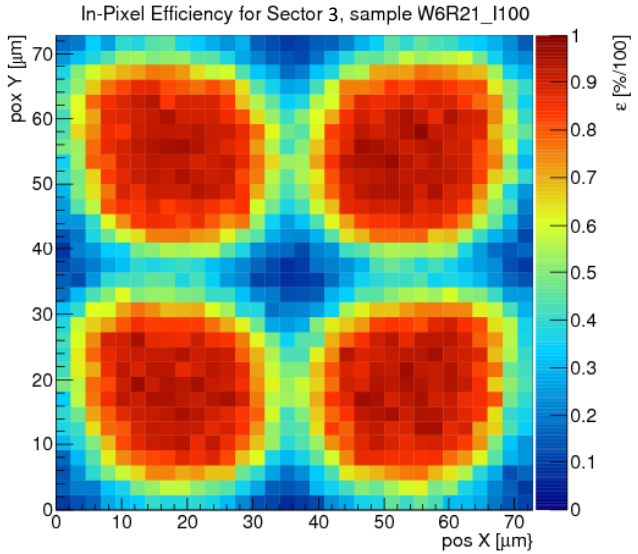


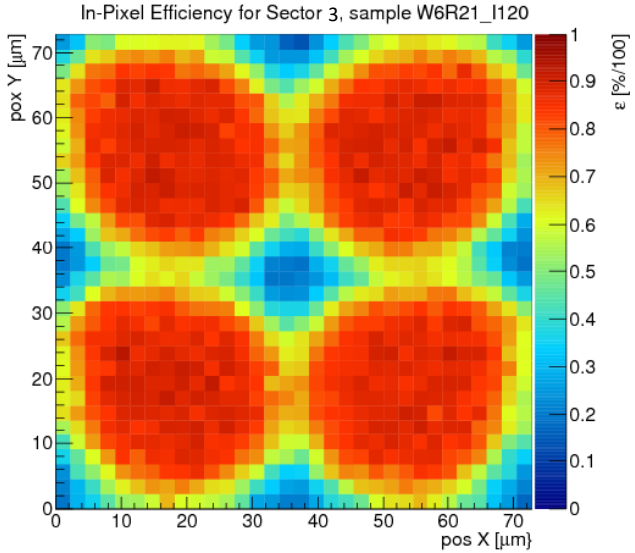




Unirradiated: lowering the threshold gives full efficiency

Decreasing threshold from ~600 e^- to ~250 e^- (unirrad.)/350 e^- (irrad.)





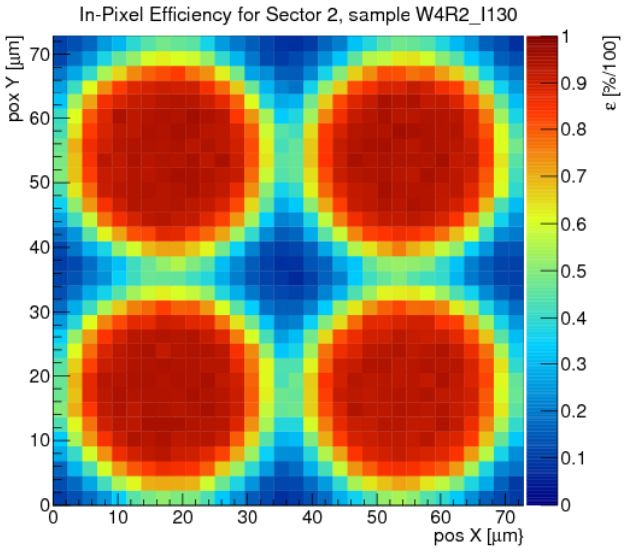
Could not reach lower threshold

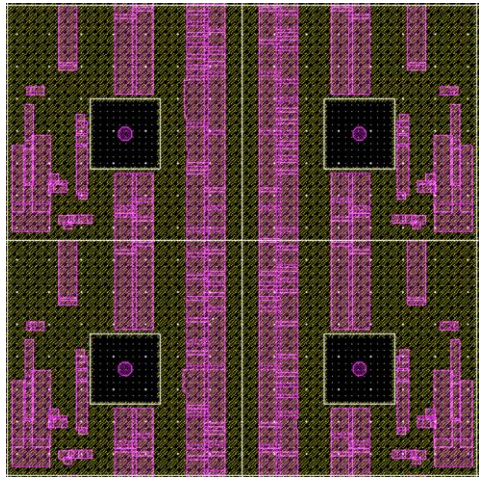
(RTS + MASKING ISSUE)

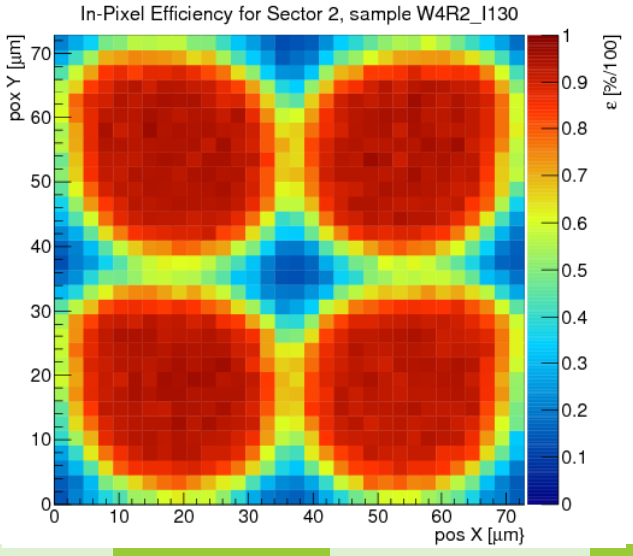
Neutron irradiated $5x10^{14}$ neq/cm^2

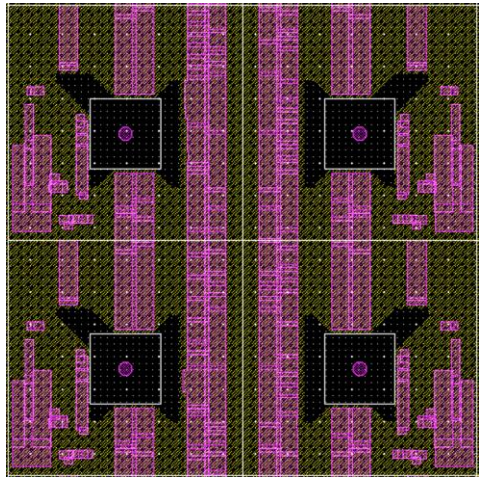
inefficiency in pixel corners due to low lateral electric field

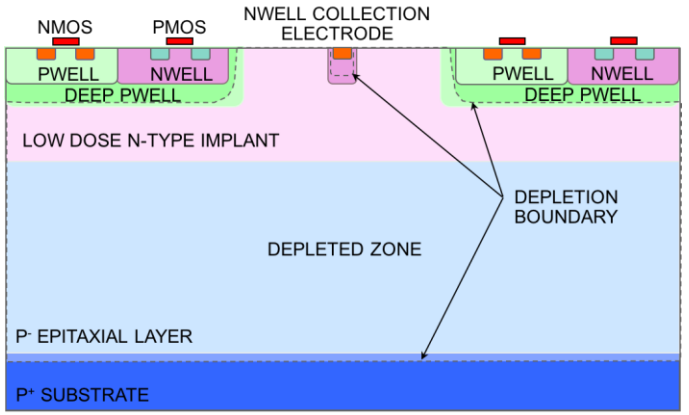
Efficiency vs. deep p-well coverage



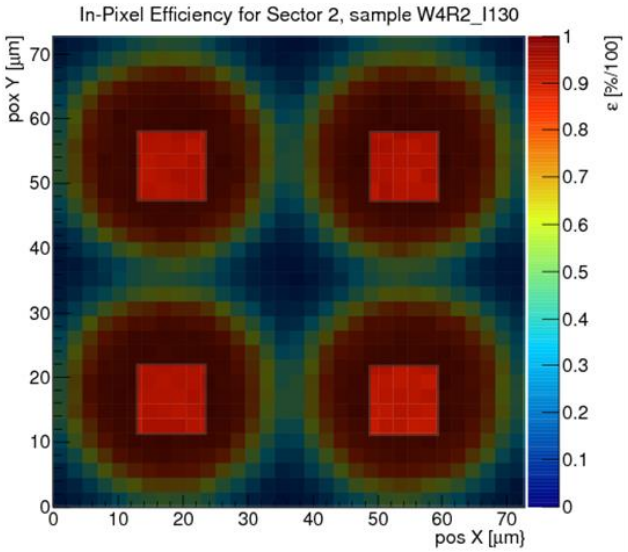


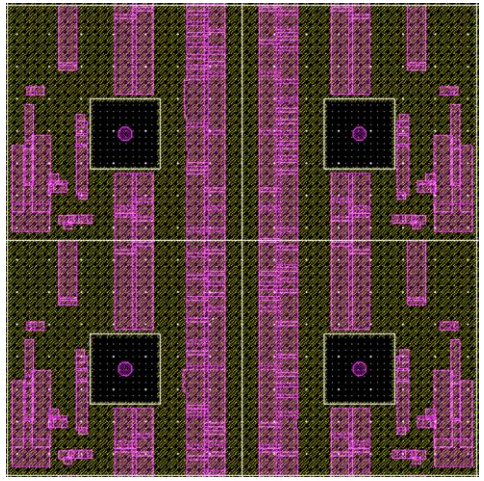


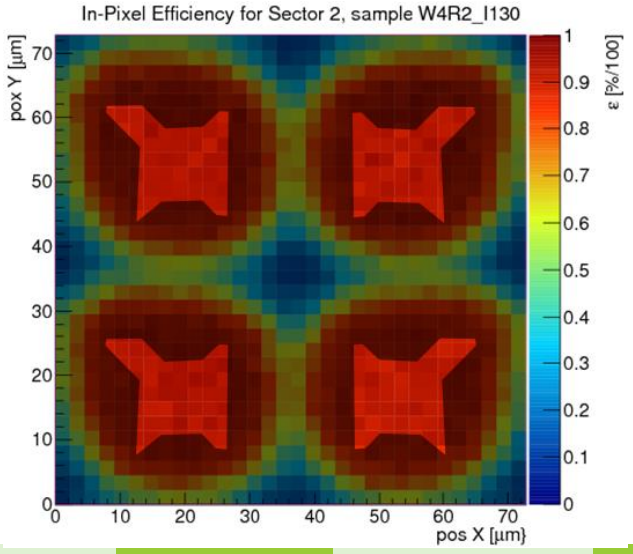


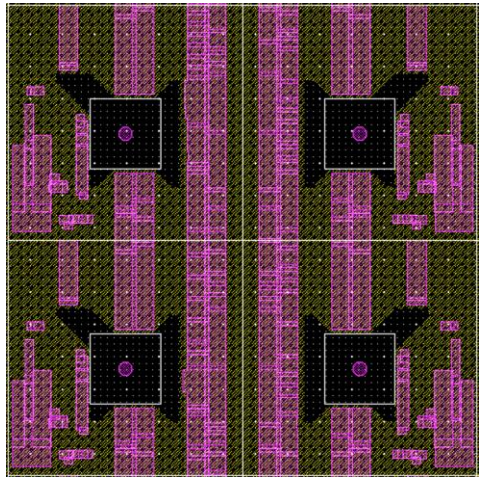


Efficiency vs. deep p-well coverage

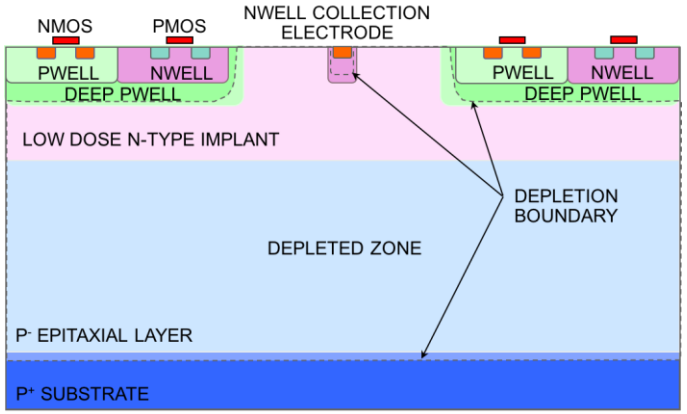








- Deep p-well only needed under n-wells of PMOS transistors
- In-pixel efficiency can be correlated to deep p-well coverage around the collection electrode
- Removed deep p-well results in higher overall efficiency due to higher lateral electric field



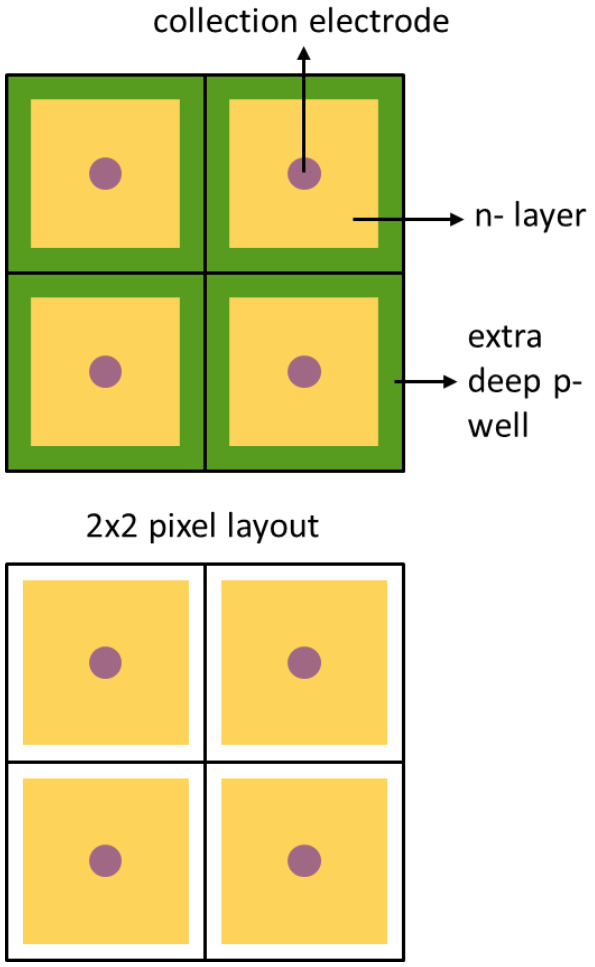
Pixel design improvements

Additional “extra-deep p-well” layer

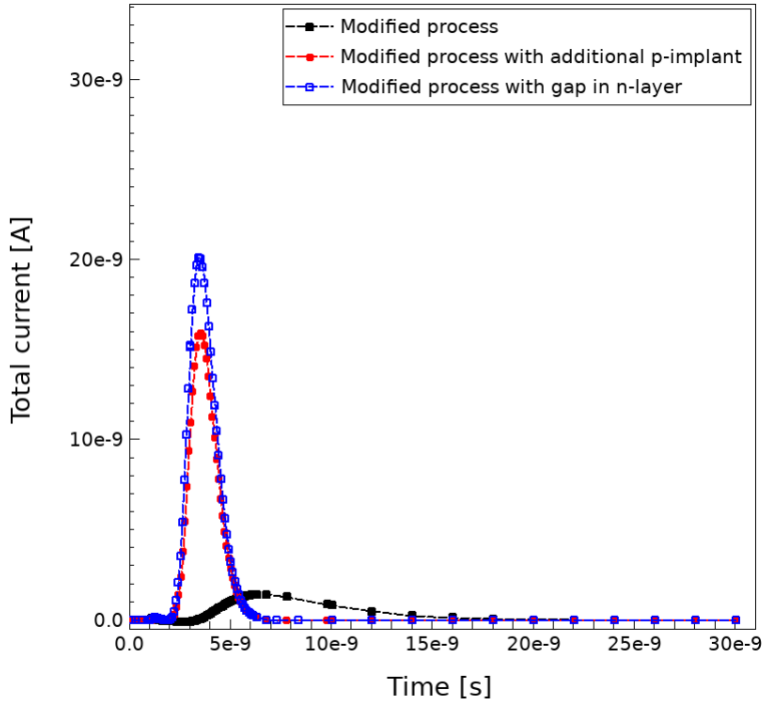
- Already known by TowerJazz: no process R&D needed

Gap in the n- layer

- requires only a change of the existing mask for the n-layer



After irradiation simulated current pulse



Magdalena Munker

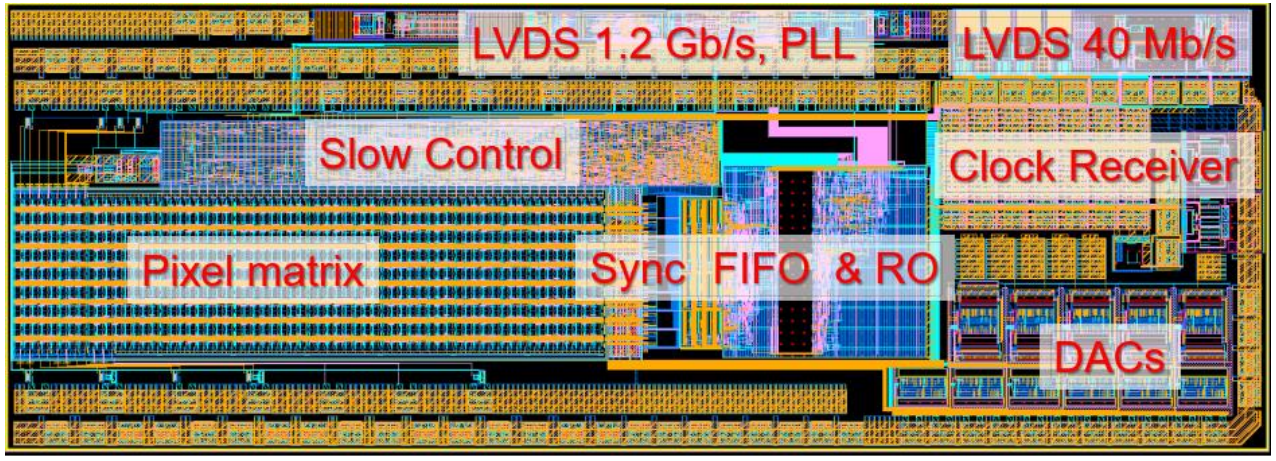
Talk on efficiency simulations

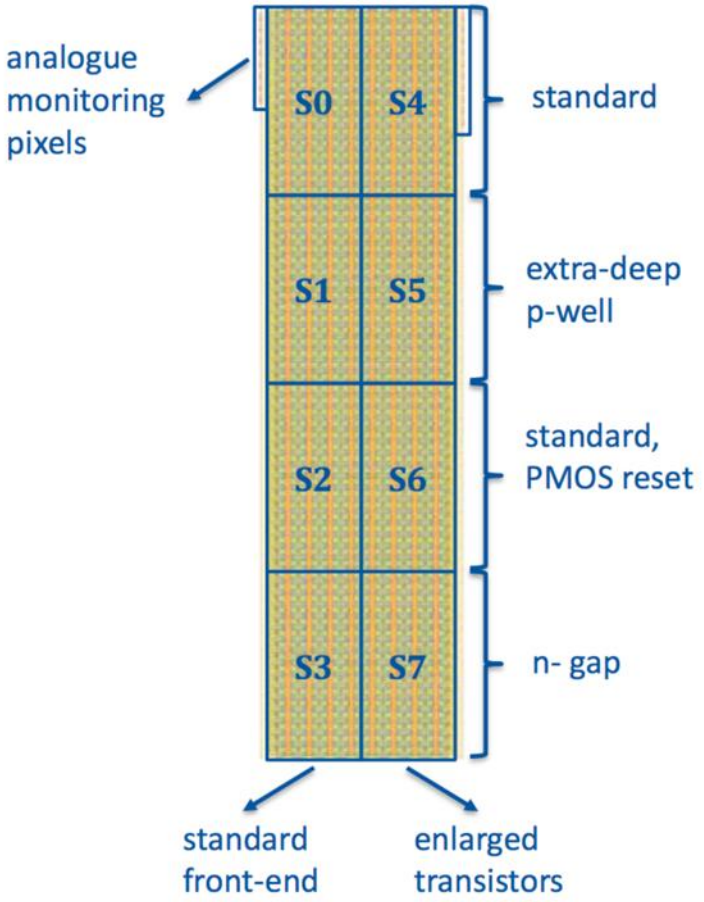
Mon 10/12 11:10 *Ruth Magdalena Munker*

Simulations of CMOS sensors with a small collection electrode improved for a faster charge-collection and increased radiation tolerance

Mini MALTA pixel matrix

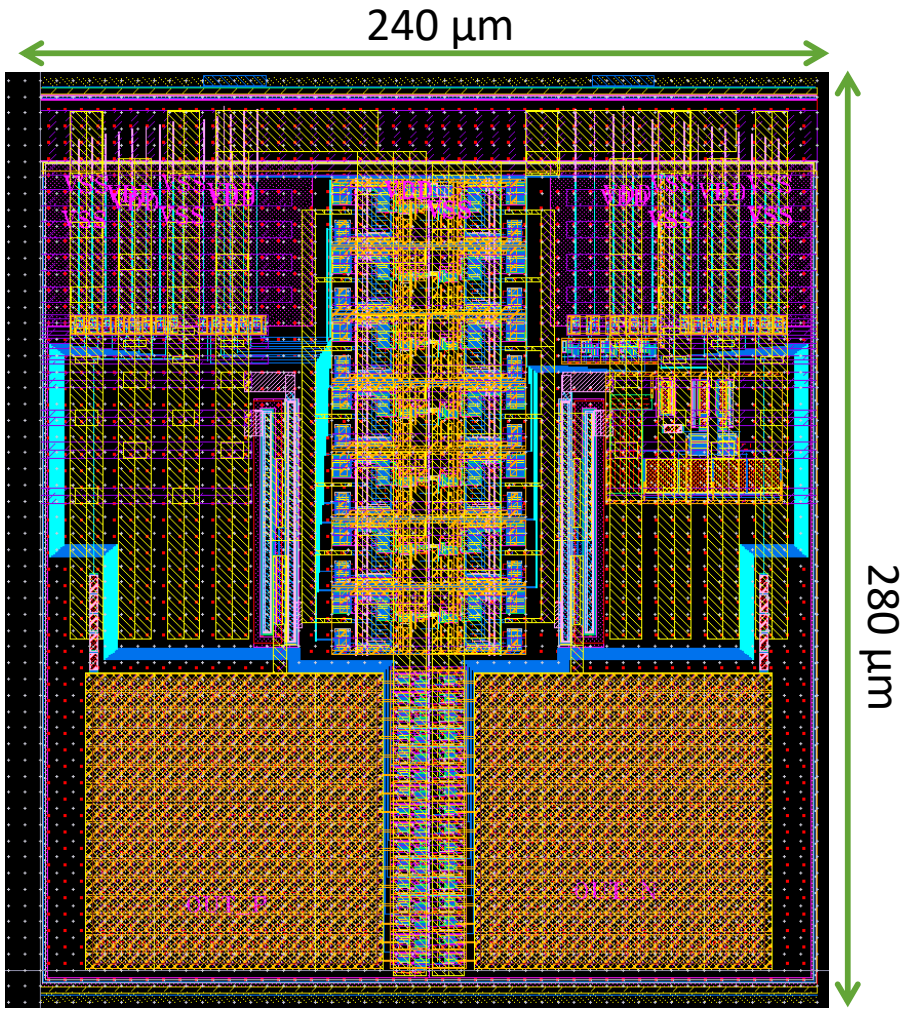
- Pixel size: 36.4 µm x 36.4 µm
- 64x16 pixel matrix includes 8 sectors with splits on analogue front-end design, reset mechanism and process





Mini MALTA with synchronization and fixes for improved chargecollection

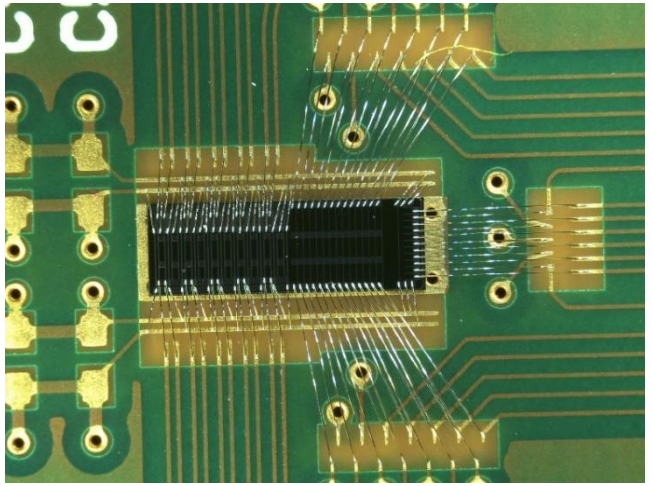
LAPA: pseudo-LVDS for the ATLAS Pixel Apparatus



5Gb/s

- 280 X 240µm^2 (2 pad pixel pitch)
- Tunable DC current (7x 0.8mA)
- Modular capacitive coupled pre-emphasis: 16 blocks driving 25fF each.
- Vcm feedback control at 0.8V.
- External 100 Ω differential termination
- 40 drivers integrated in MALTA (up to 2Gb/s)

Dedicated testchip



LAPA eye diagram

5Gb/s

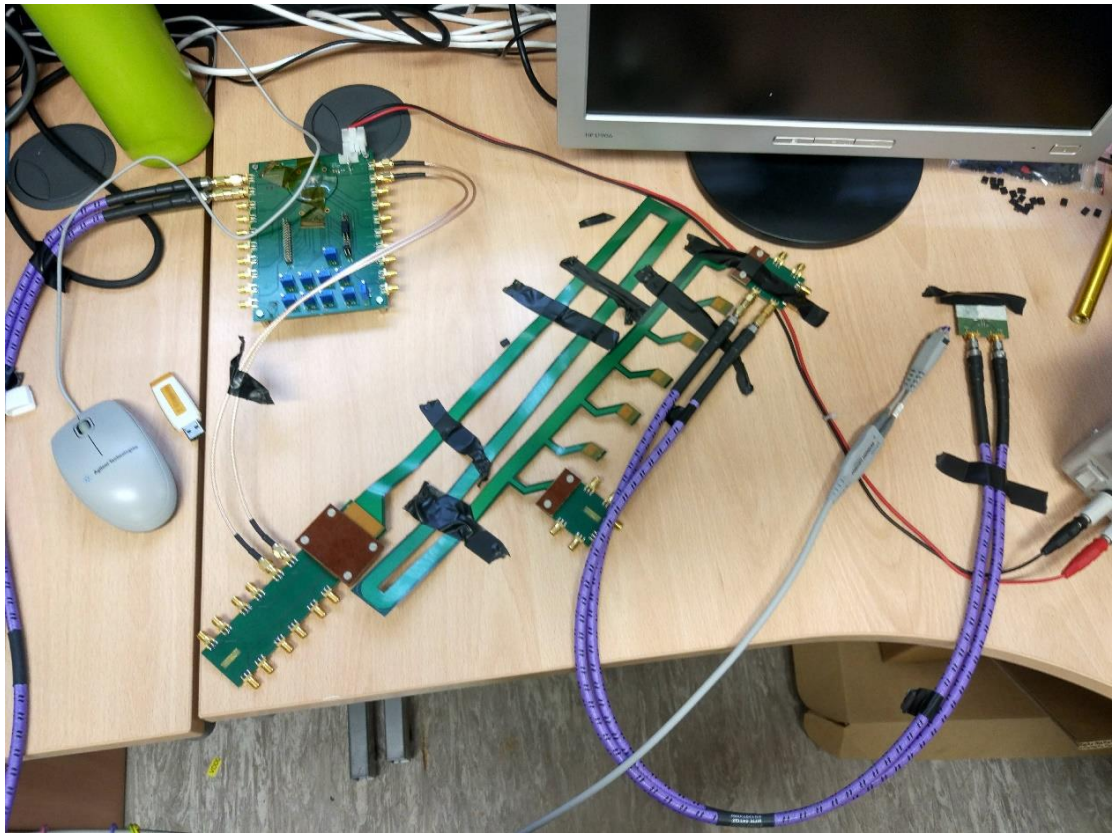
1.28Gb/s (ITk specification)

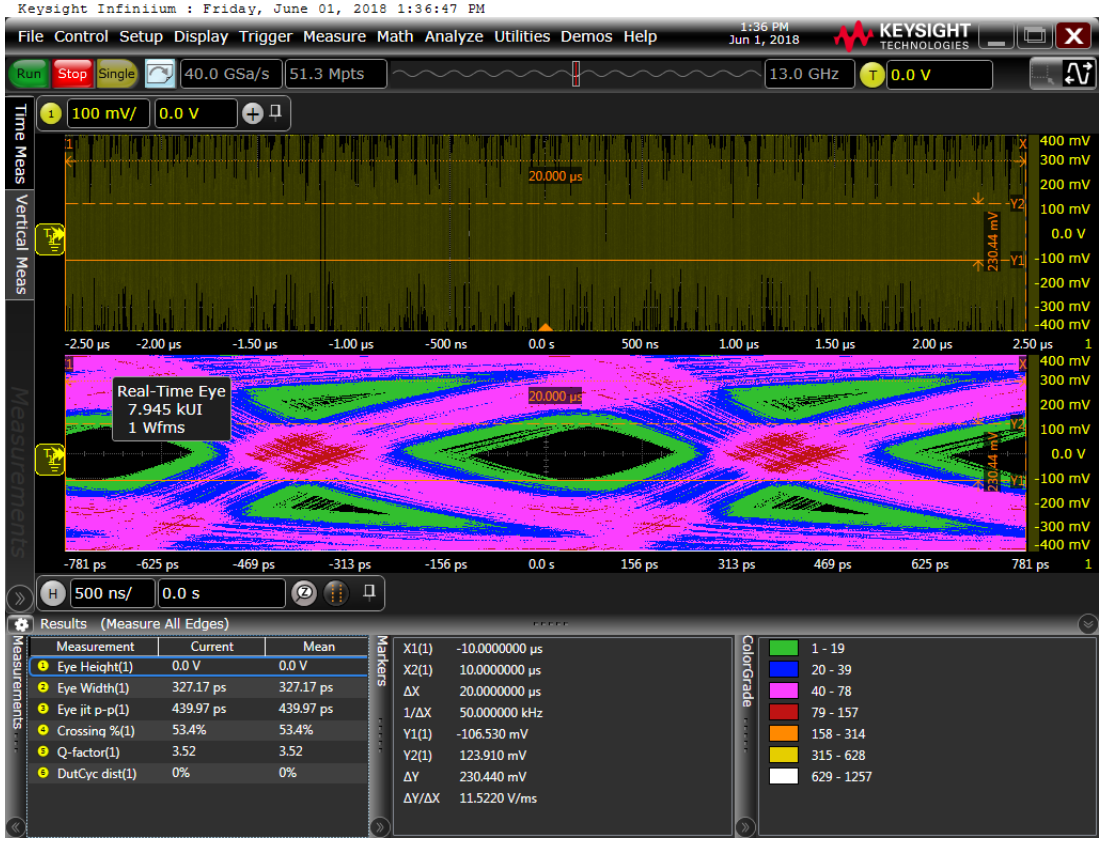
$Jitter_{p\text{-}p}$= 71ps

$Jitter_{p\text{-}p}$= 38ps

LAPA @1.28 Gbit/s on FLEX ITk prototype

Flex for data transmission out of the ITk system (length~5m)

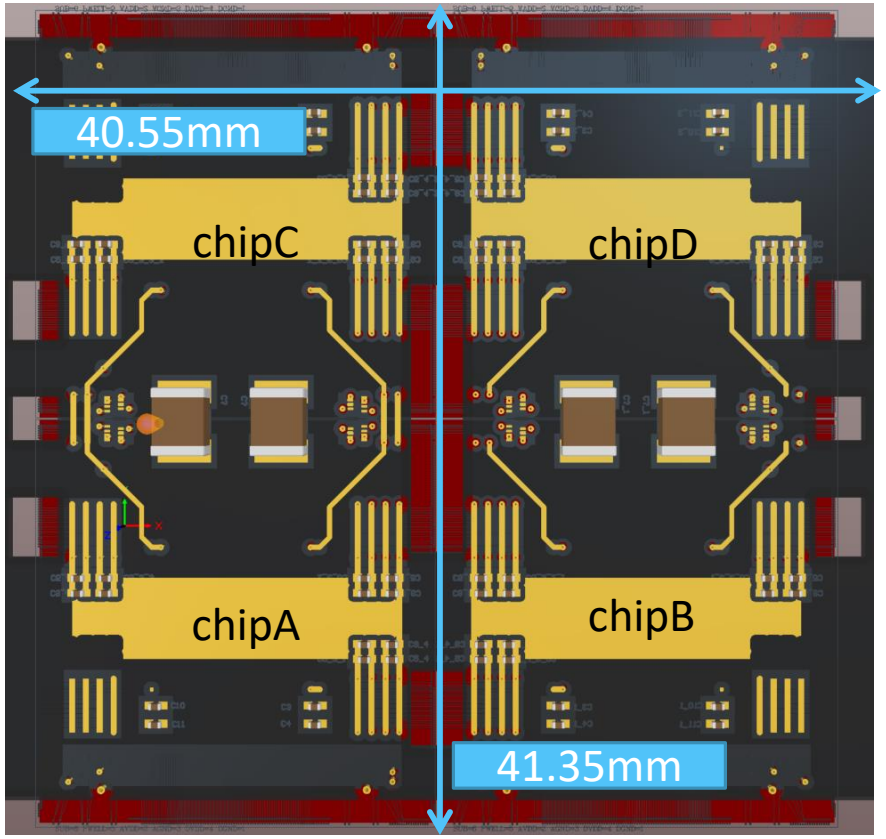




CMOS Quad-Module design

The ATLAS ITk sensors will be organized in quad modules.
In the case of the hybrid pixel, one sensor of around 4x4 cm^2 will be bonded to four 2x2 cm^2 front-end chips

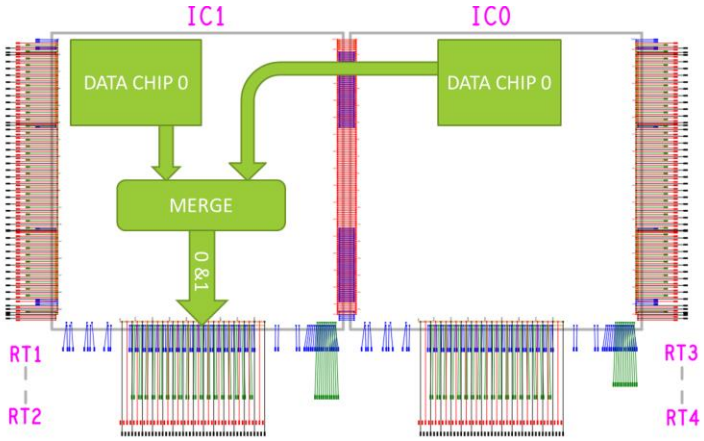
MALTA is the first large scale monolithic chip that allow build a compatible Quad-Module, assembling four detectors in a single FLEX



Under design

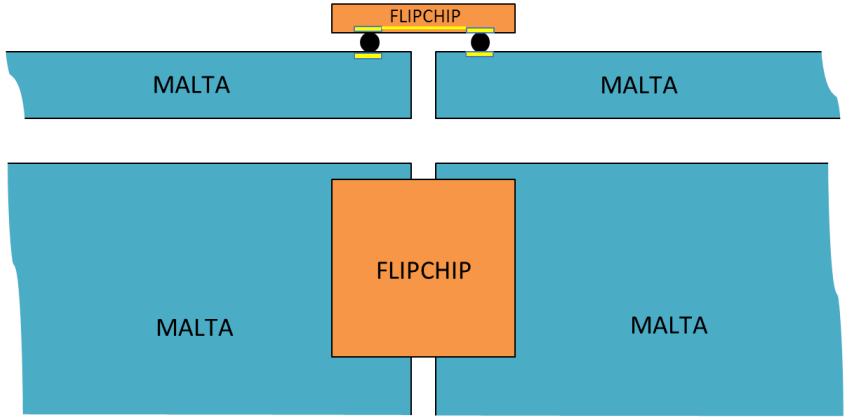
Parallel R&D on MALTA

Chip to Chip communication



MALTA can transmit power and data asynchronously to a neighboring chip (via CMOS pad), merging the data of multiple pixel matrix in just one parallel output

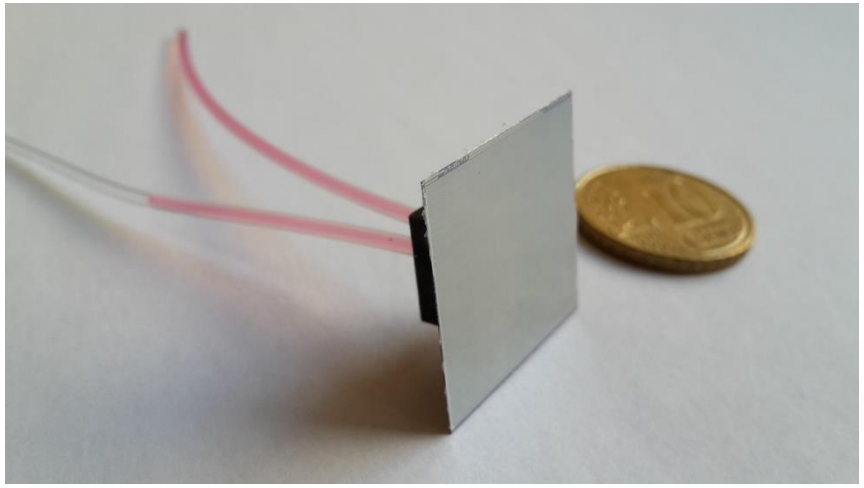
Flip chip connection

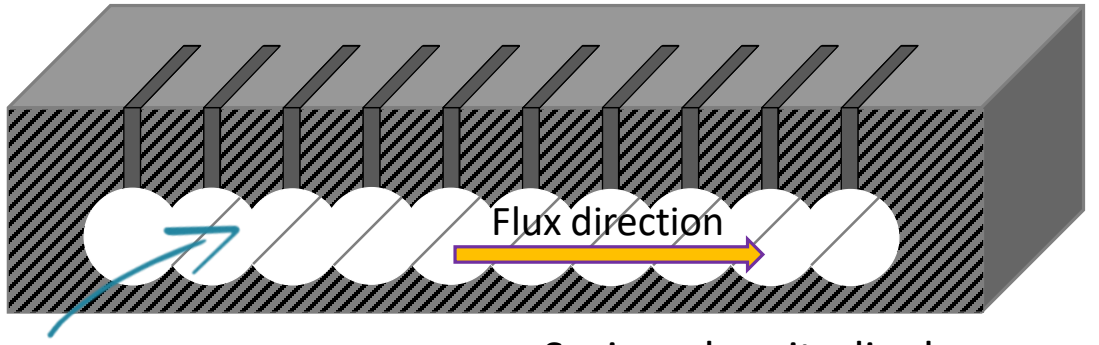


Connection between neighboring chips using flip chip

- Better for assembling
- Allow additional electronics in the flipchip

Buried channels cooling





(Ø 35 µm, length ≈ 1 cm)

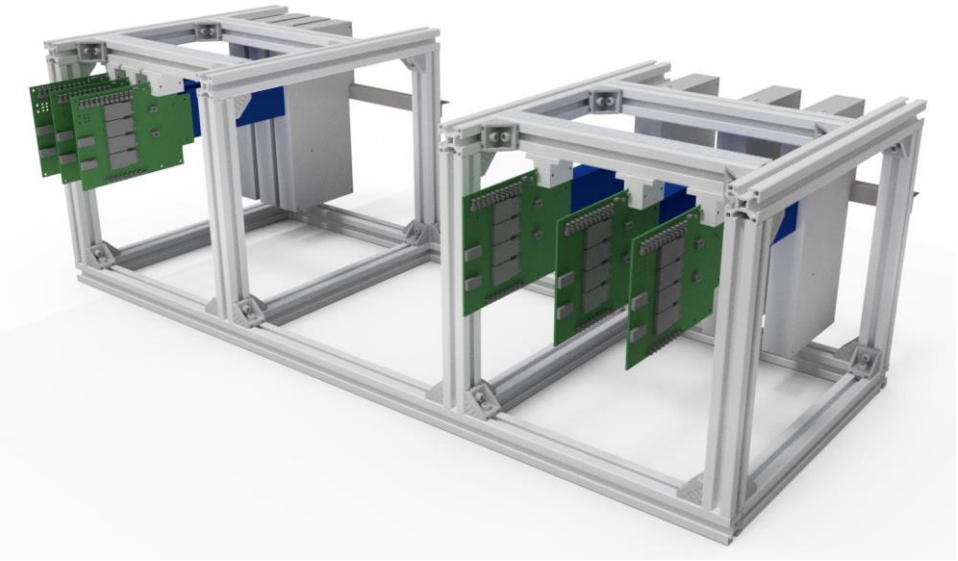
Sezione longitudinale

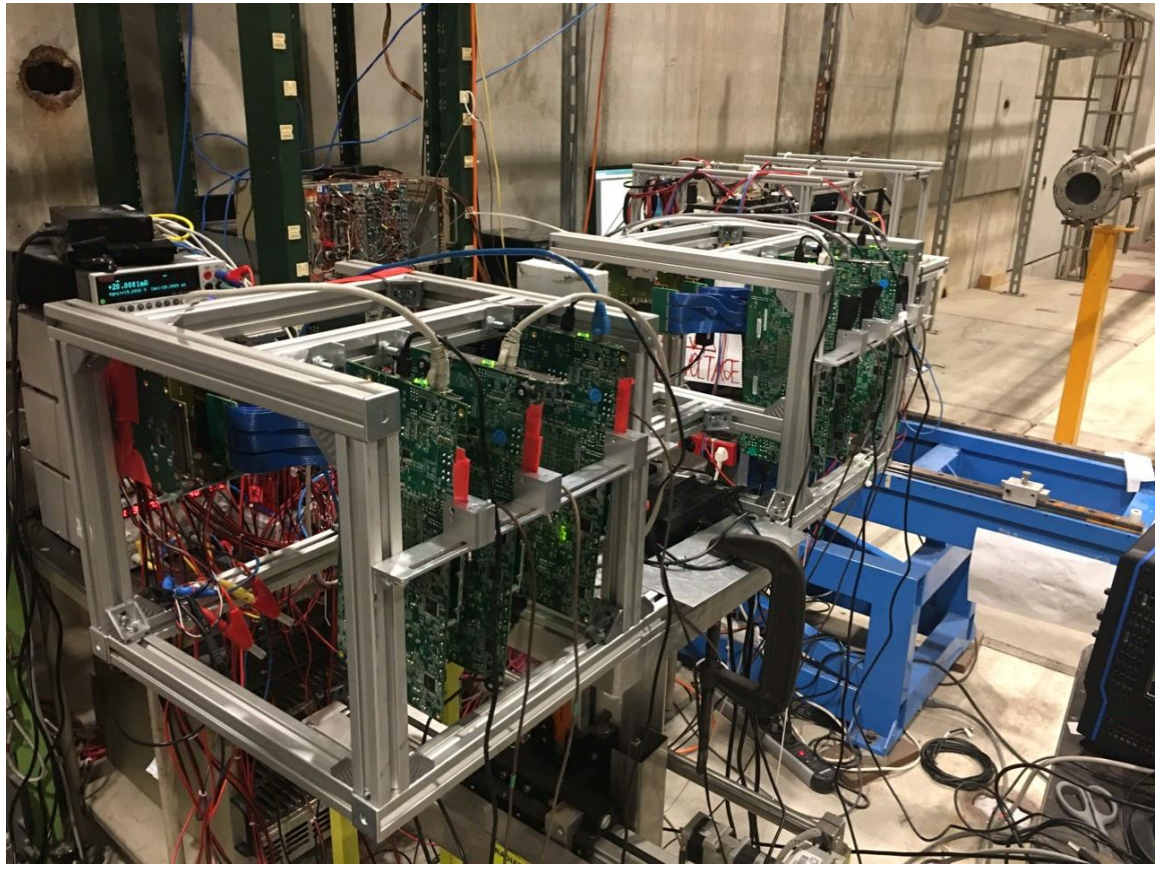
DOI: 10.1109/ITHERM.2012.6231493

J. Bronuzzi, A. Mapelli, R. Callegari, P. Riedler

Malta Telescope

6 MALTA chip-based planes
2 Scintillators
4um resolution





Conclusions

The MALTA CMOS pixel sensor was developed in view of the ATLAS High-Luminosity upgrade.

The large pixel matrix implements a fast, low-power analogue front-end and a novel asynchronous readout architecture.

The chip has been extensively characterised in lab measurements and testbeam, and shows promising results in terms of front-end performance and readout capability, but needs further improvement:

The small collection electrode sensor suffers from degraded efficiency in the pixel corners after irradiation to 10^{15}neq/cm^2, and this is being addressed by means of improvements in the process (see M. Munker's presentation), and also in the front end design to obtain a lower threshold.

An LVDS driver has been designed and tested to transmit the data to the ITk readout system, up to 5Gb/s.

The MALTA chip allows to build the first prototype of a monolithic module, compatible with the hybrid equivalent for the ITk system.

Several R&D on monolithic pixel sensors are in progress using the MALTA chip, such as buried channels cooling and chip to chip data communication.

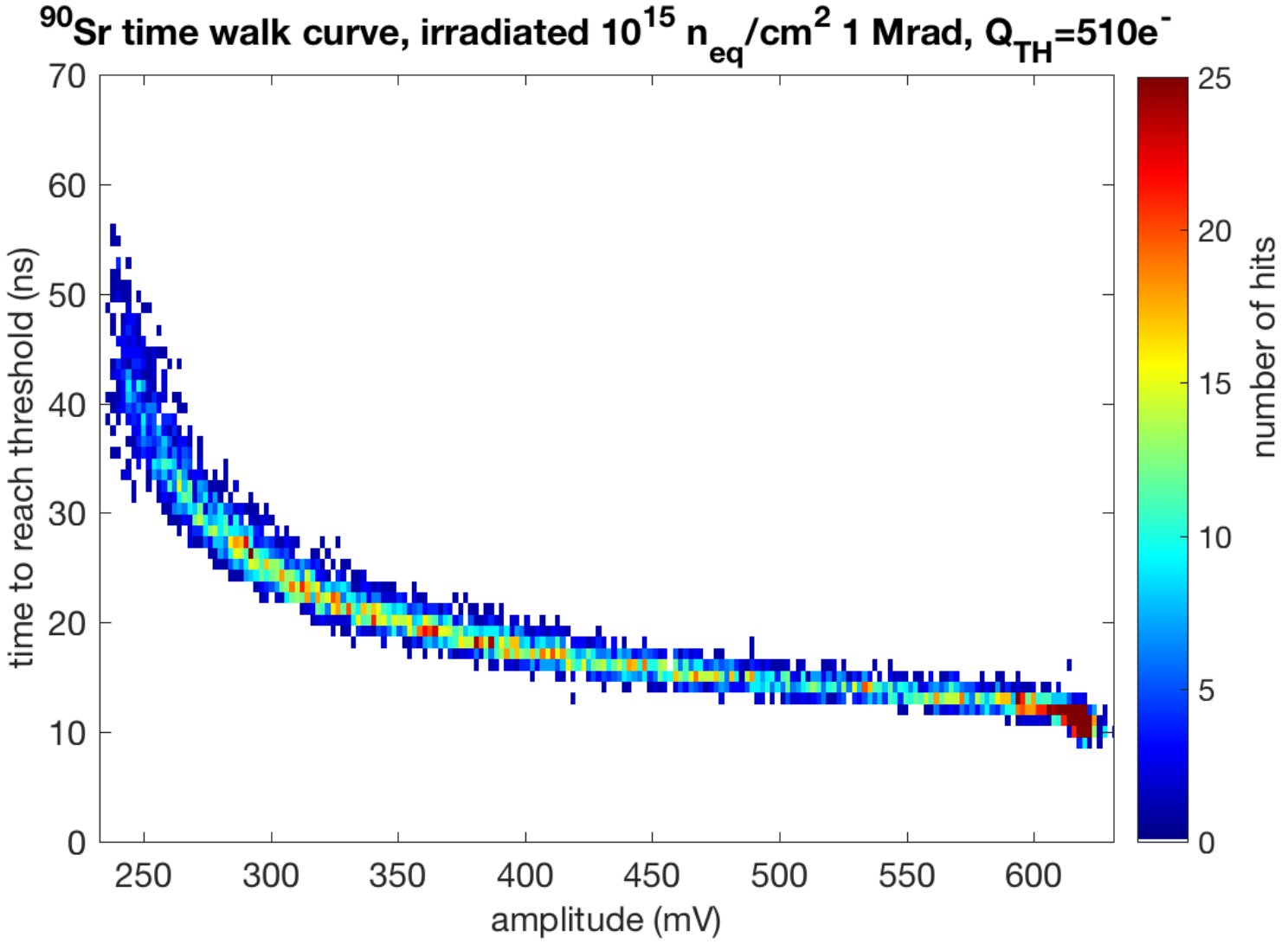
Thank you for the attention

Question time!

Backup slides

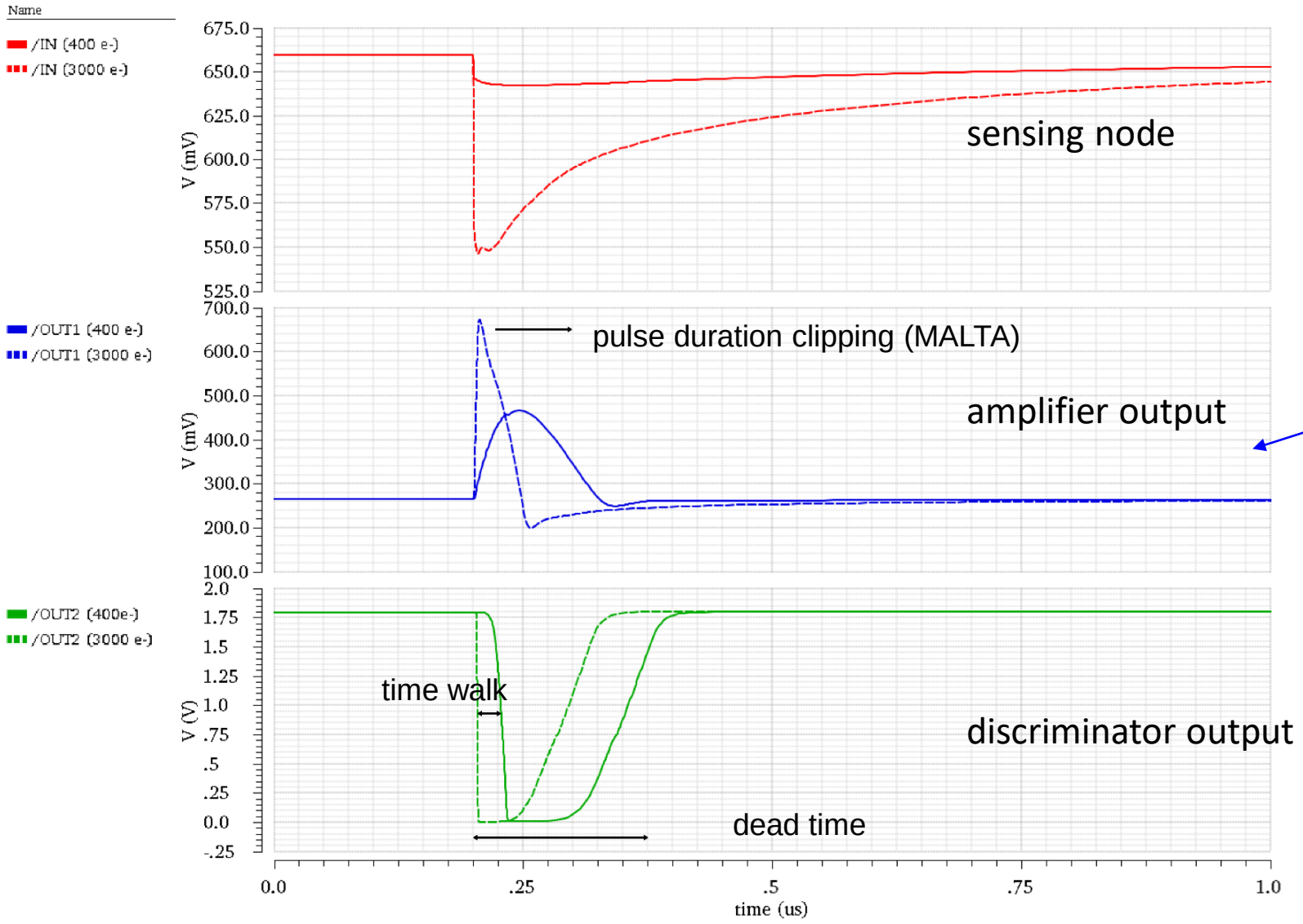
Time walk after irradiation

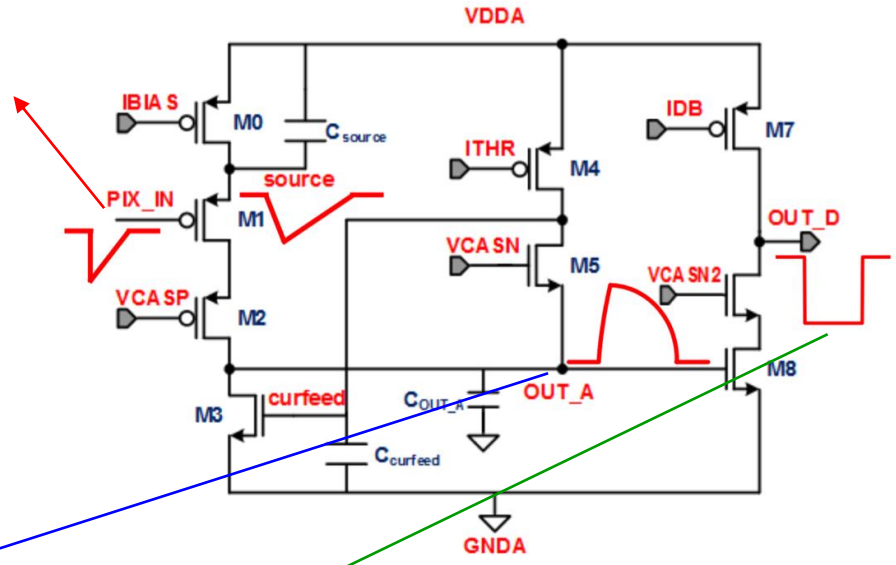
Little change in front-end signal and timing after irradiation (somewhat more charge sharing)



Front-end optimization (simulation)

*I. Berdalovic et al 2018 JINST **13** C01023*

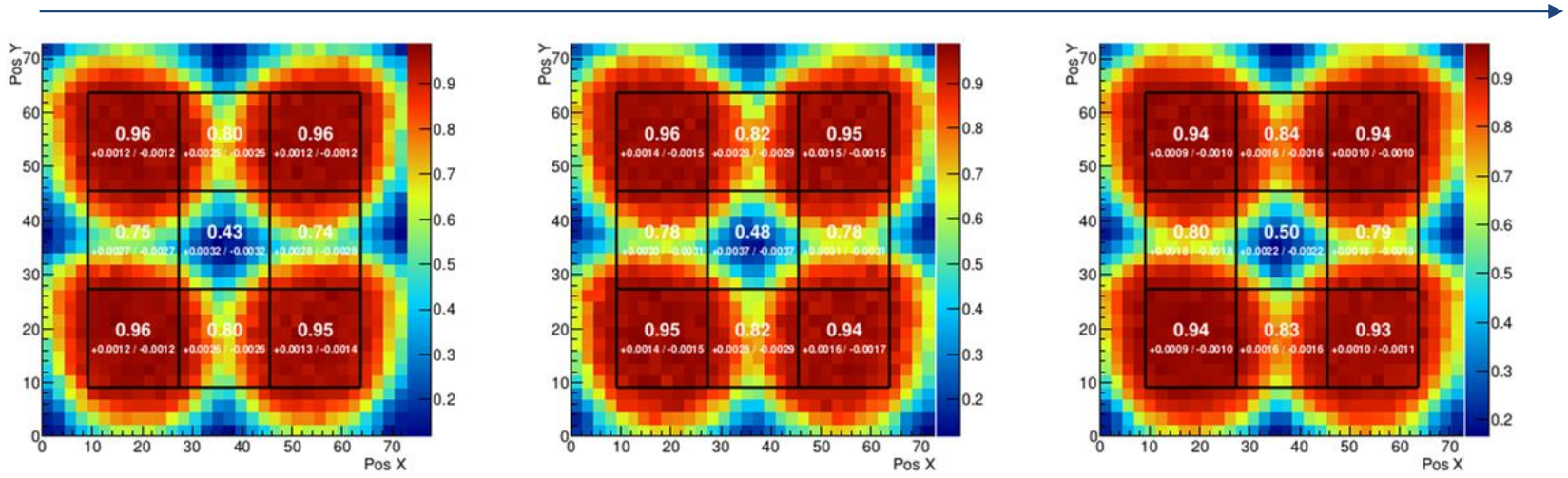




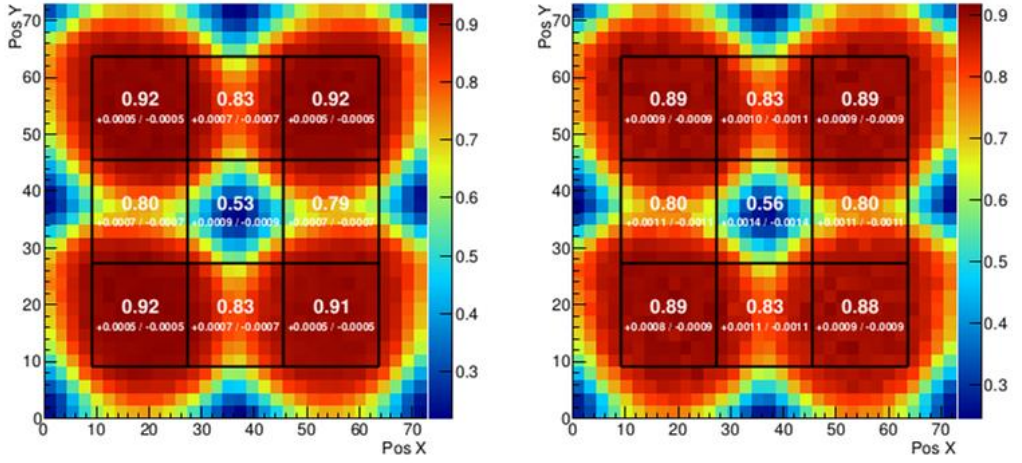
P_{analog} = 0.9 µW

Charge threshold Q_{th}	300 e
Equivalent Noise Charge	7.1 e
Channel-to-channel RMS	10.2 e

Efficiency after irradiation to 10^{15} n_{eq}/cm^2



(a) (b) (c)



(d) (e)

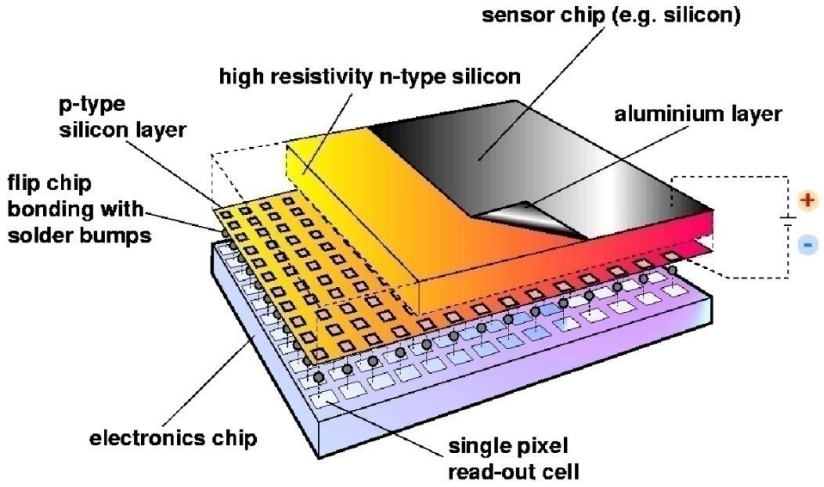
Decreasing threshold from ~450 e^- to ~350 e^-

Artifact: pixel center efficiency decreases at low thresholds due to noise issues

Silicon Pixel Detector

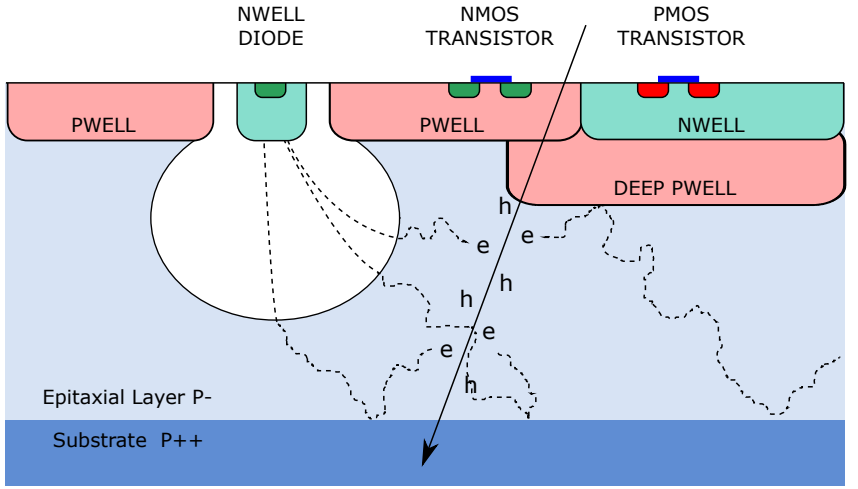
Hybrid

- Used in current LHC detectors
- Optimized silicon sensor for radiation hardness
- Dedicated front-end electronics bonded to the sensor
- Thick modules
- Complex and costly assembly due to fine-pitch bump bonding



Monolithic

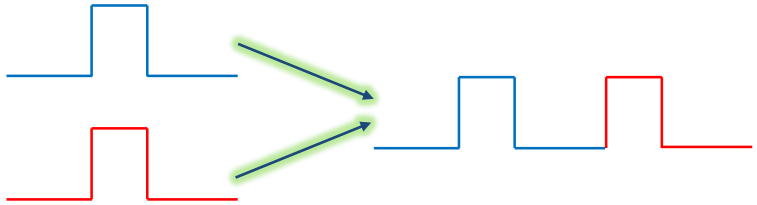
- Promising technology for future detectors
- Single chip integrate electronic and sensor
- Radiation hardness limitation
- Lower material budget
- Large number of available vendors



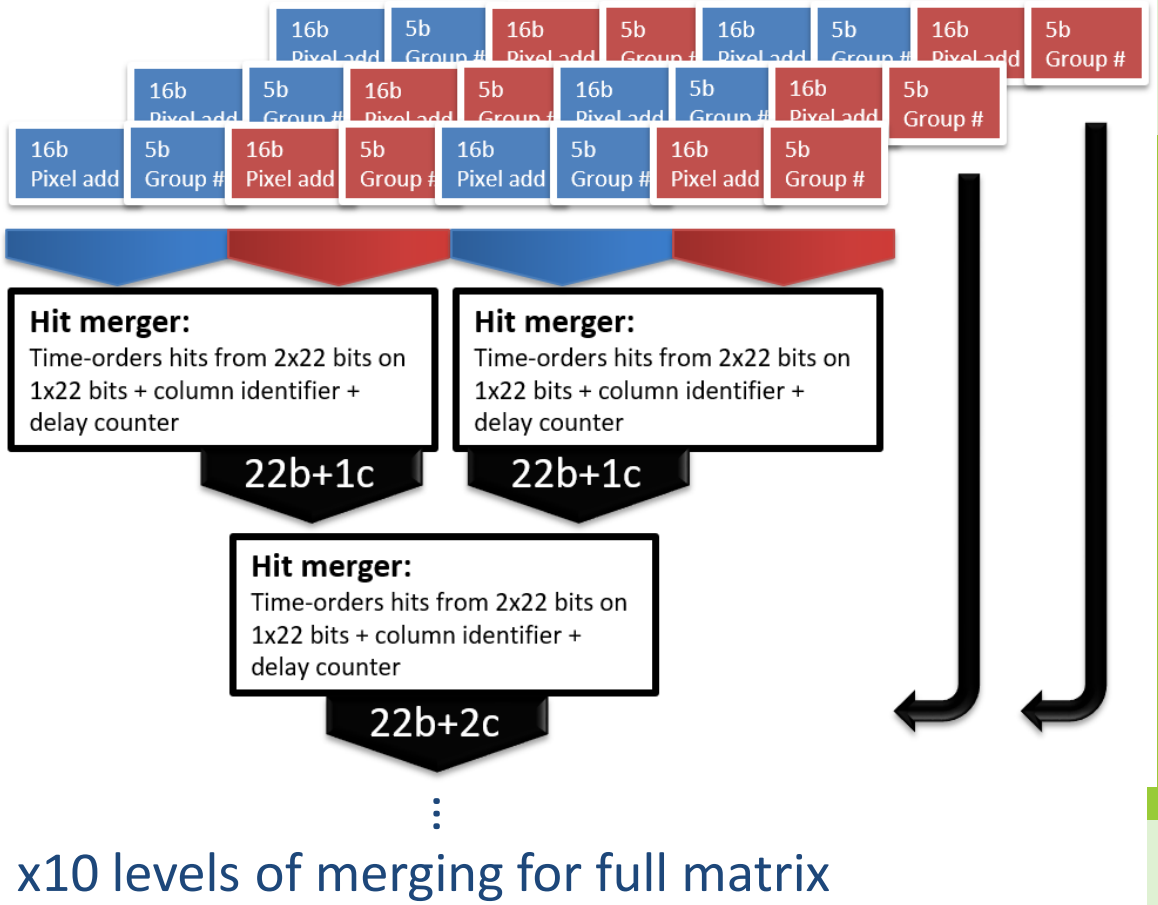
MALTA periphery logic

The MALTA periphery implements a fully **asynchronou**
signals coming from groups with different colour

In the case of simultaneous signals on two buses the l
the other is delayed

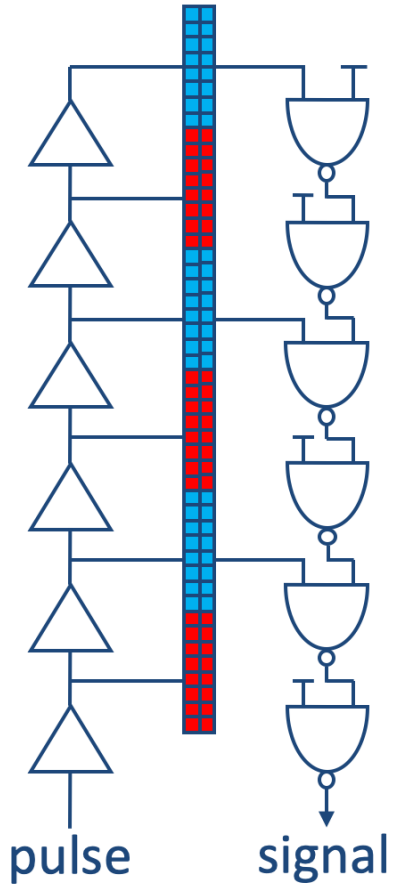


Merging is repeated for all the double-columns in a bi
column address bit in each step, until all outputs are r
bus

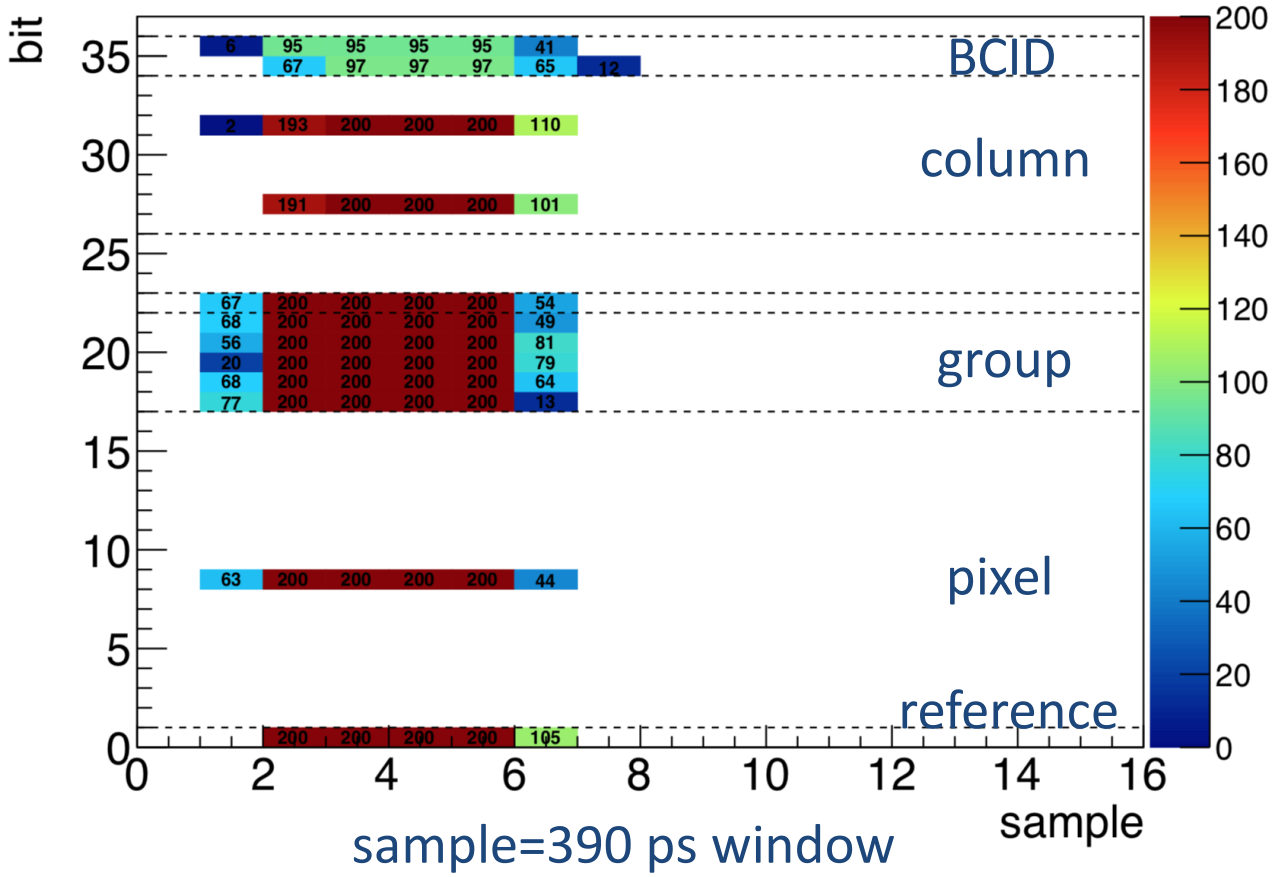


Asynchronous readout – measurements

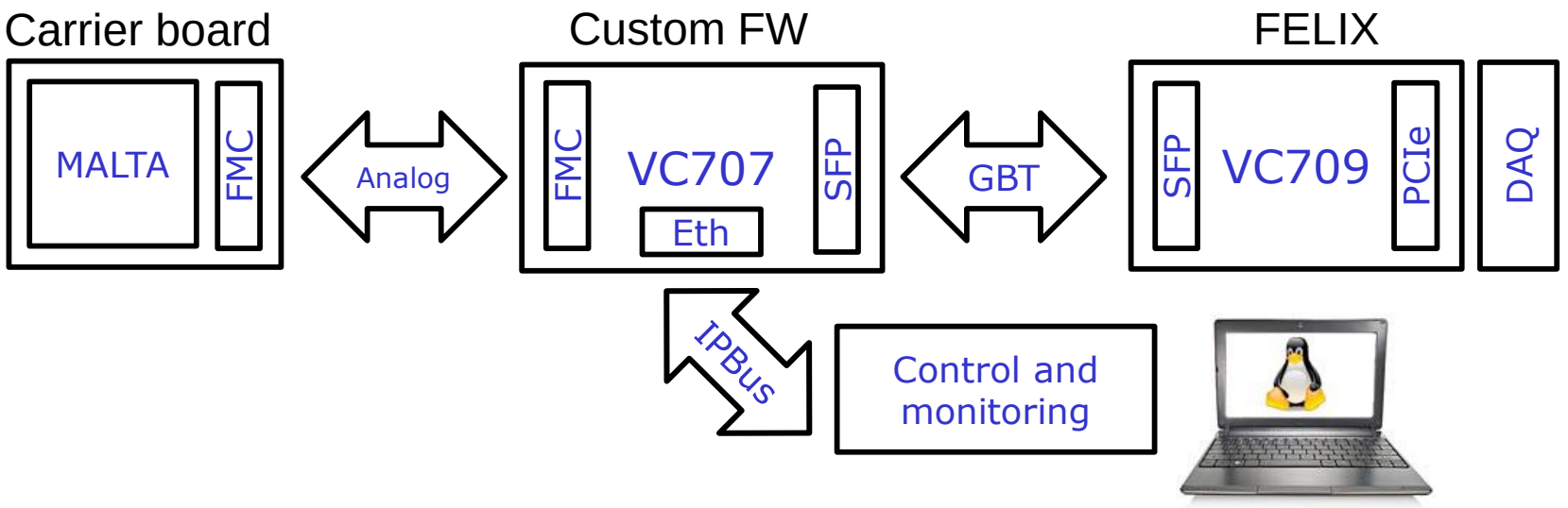
Parallel data bus requires **delay uniformity**: al
at the reference signal



(pulsing a pixel 200 times and oversampling the output signals to check the timing alignment)



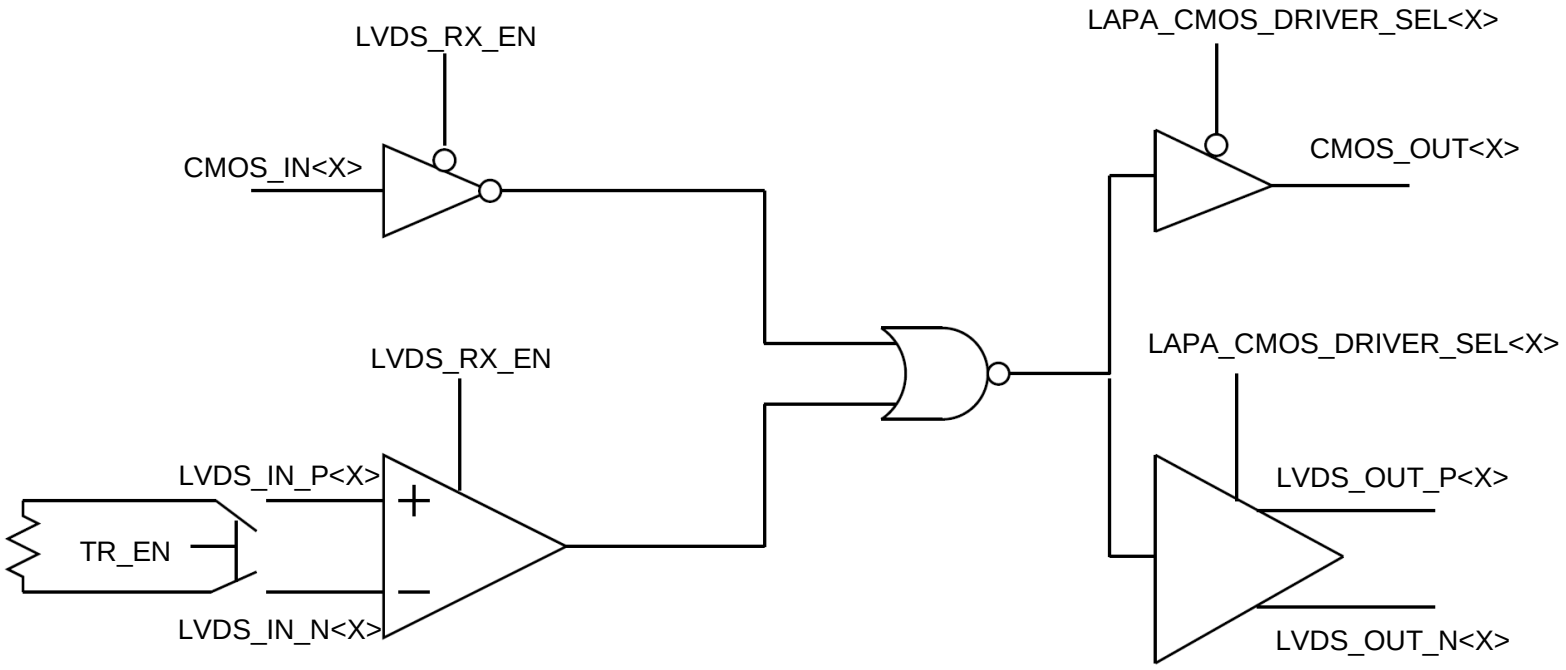
MALTA Read-out system



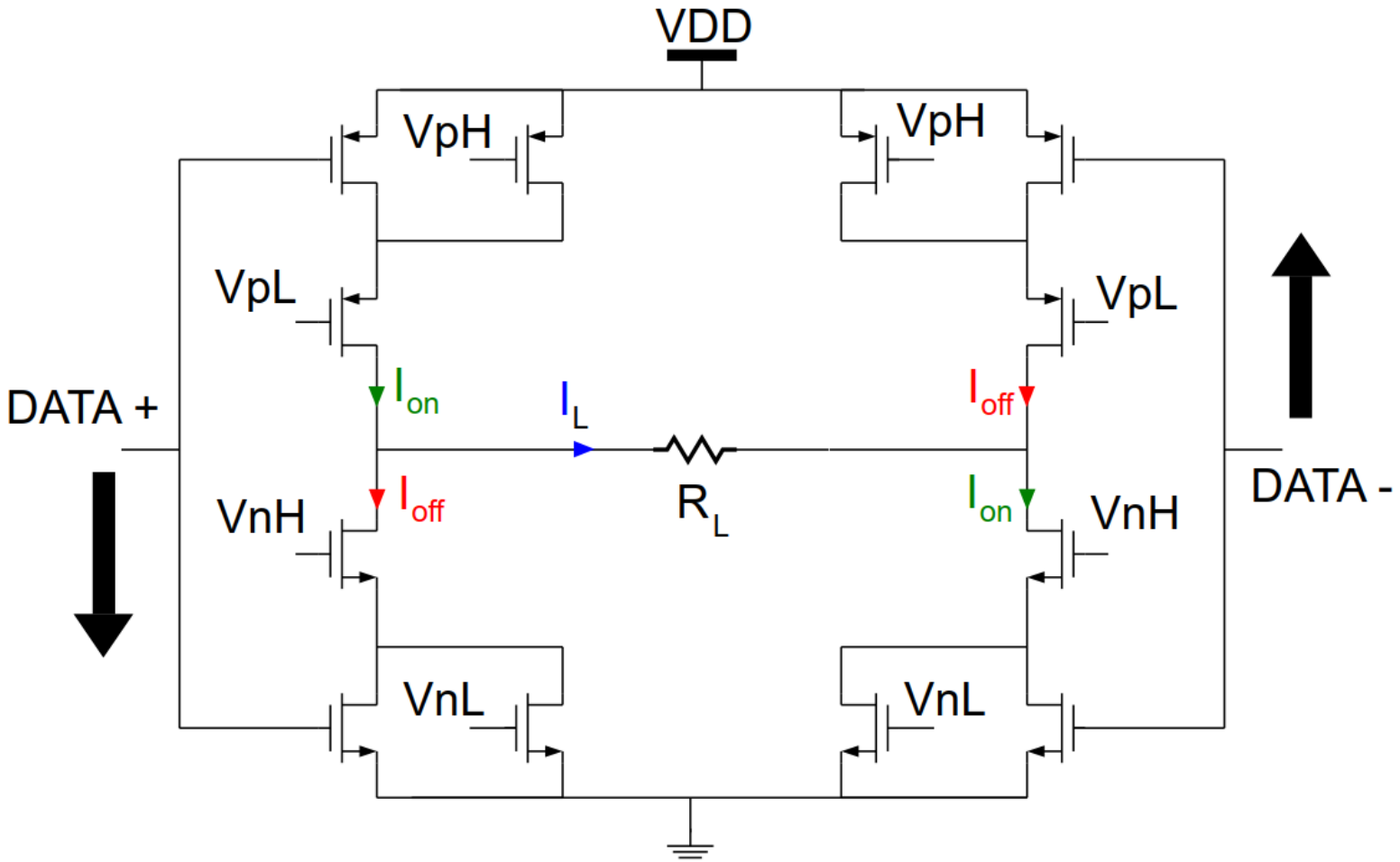
- Carrier board for two MALTA chips with FMC interface
- Asynchronous oversampling on Xilinx VC707 board
- Slow read-out through IPbus ethernet to Linux PC running SLC6
- Fast read-out through GBT optical link with FELIX + ITK SW

R. Cardella, V. Dao, C. Marin Tobon, E.J.Schioppa, B. Schlager, L. Simon Argemi, C. Solans Sanchez

LAPA Single Channel Schema

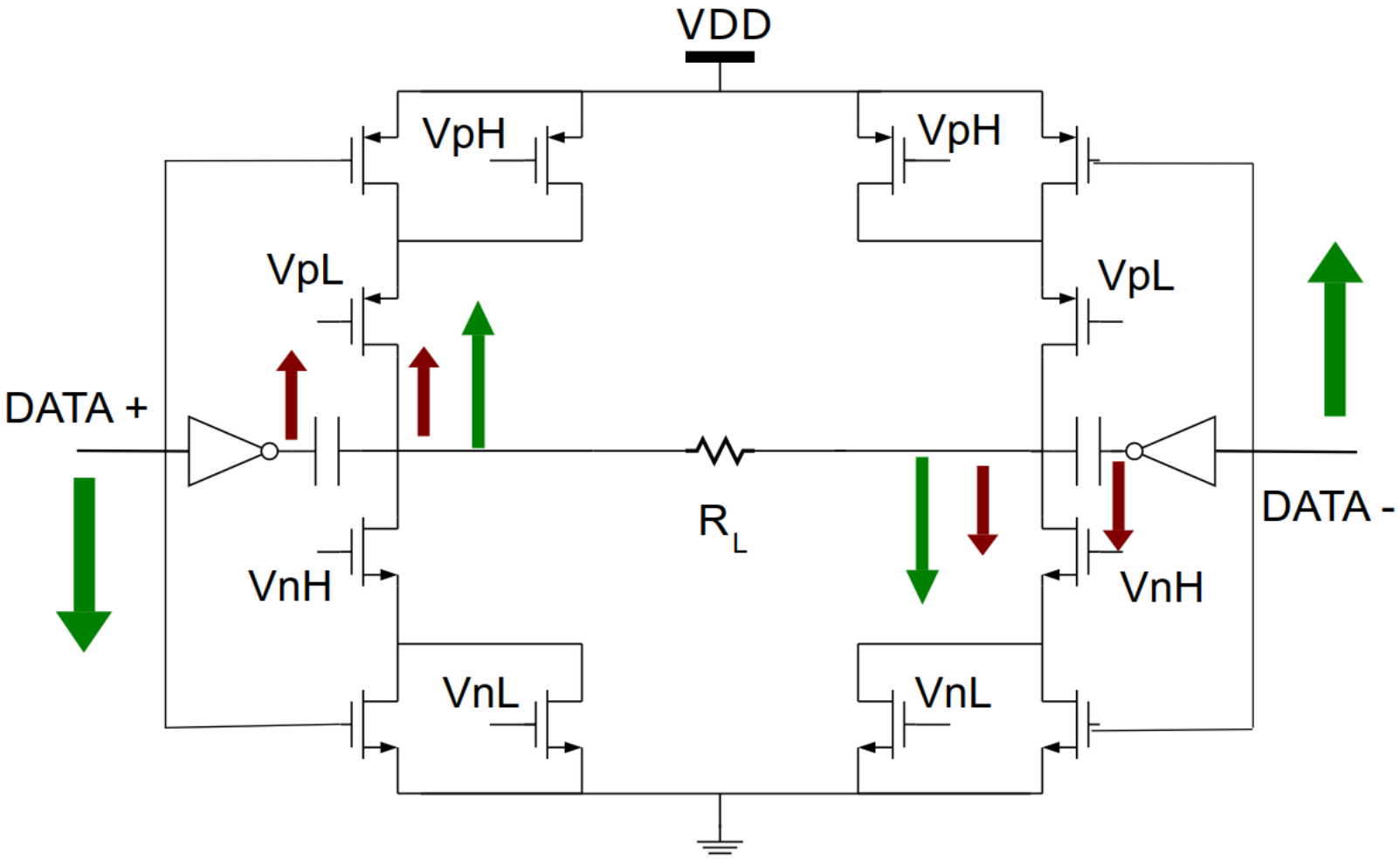


LAPA H-BRIDGE



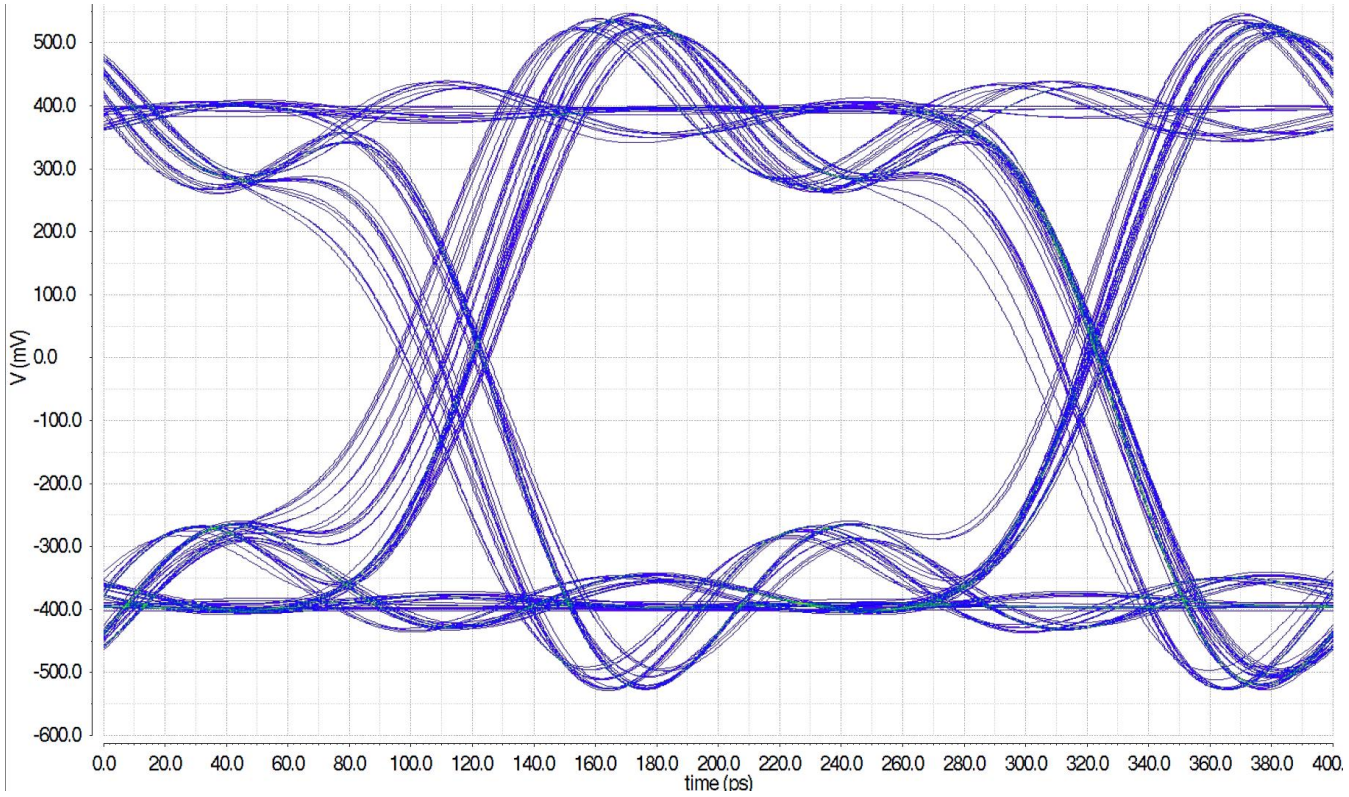
7 HBRIDGE blocks of 0.8mA - max: total 6mA

LAPA-PRE-EMPHASIS



16 BLOCKS driving 25fF coupled with the output pad

LAPA TESTCHIP SIMULATION



2.5GHz LVDS IN – LVDS OUT. 100Ω termination. 1pF load.

Simulated jitter=45ps

Preliminary power consumption

Expected static power consumption

Static	Current [mA]	Power [mW]
5 Hbridge	4	7.2
7 Hbridge	5.2	10

Measurements on test chip

Static+Dynamic 1.28Gb/s	Current [mA]	Power [mW]
5 Hbridge	6	10.8
7 Hbridge	8	14.4