



Study of efficiency and noise of fine pitch planar pixel detector for ATLAS ITk upgrade

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13th Dec 2019

Introduction

<u>High Luminosity LHC (HL-LHC)</u>

- Start around 2026- with new crab cavity in the interaction region.
- Target : \sqrt{s} =14TeV L=5x10³⁴ $\int Ldt$ =3000fb⁻¹
- Physics program focus the precise measurement of the Higgs coupling (e.g. $Y_{\tau},\,Y_{b}$ and $\lambda_{\rm HHH})$ and BSM searches.
- Tracking detector is key element
 - To keep B/ τ -tagging performance up to μ =200 pileup in an event.
 - Mitigation for the pileup effect for MET calculation can be done by tracking from primary vertex.

• Development of middle-outer pixel layer

- Planar type Pixel detector (For ATLAS phase II upgrade : ITK pixel)
- n+-in-p sensor with Pixel size : 50um x 50um (or 25um x 100um)
- Radiation tolerance : up to $3x10^{15} n_{eq}/cm^2$

Sensor performance of 50um x 50um planar pixel detector is presented.

Bias structure and efficiency loss

- For n+-in-p sensor, negative bias to backside and ground at all pixels.
- Need to set all pixels to ground potential for testing I-V property before Bump bonding. (Bias structure)
 - Bias rail & bias resistor (BR)
 - Punch through (PT)
- Two important feature
 - Higher noise observed for pixels with BR structure.
 - Typical Efficiency drop at under bias structure observed. к





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Available Read out ASICs

- For sensor performance evaluation, used FE-I4, FE65p2 and RD53A.
- FE65p2 is small prototype ASIC for RD53A and have lower noise than FE-I4.

	FE-I4 (2012)	FE65p2 (2016)	RD53A (Nov. 2017)
ASIC demention	17mm	3mm 4mm	20mm 11.8mm
CMOS process	130nm	65nm	65nm
Pixel size	50um x 250um (25um x 500um)	50um x 50um (25um x 100um)	50um x 50um (25um x 100um)
Pixel matrix	336 x 80	64 x 64	400 x 192
Max data output rate	160Mbps	160Mbps	1.28Gbps x 4
stable threshold (typical threshold)	~1500 e⁻ (2000-3000 e⁻)	500 e ⁻ (700 e ⁻)	500 e ⁻ (1000-1500e ⁻)

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4

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6th sensor mask by HPK/KEK



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Irradiation Facility in Japan

- CYRIC@Tohoku Univ. is a irradiation facility with 70MeV proton beam (~1μA).
 - This allows 5-6 pixel module with back Al plain at the same time(3% E loss/pixel).
 - Operated at -15° C temprature with dry N₂ gas.
- Programmable X-Y stage and "push-pull" mechanism are implemented to the machine.
 - choose one or a few target samples in max 15 pre-installed samples.
- Scanning over full pixel range during irradiation.
- Actual Fluence difference relative to the target fluence is within ~10%.



Testbeam at CERN SPS H6A/B

- To evaluate efficiency in pixel, performed testbeam before/after irradiation.
 - CERN H6 beam line
 - 120GeV pion beam
 - 7 testbeams in 2016-2018 at CERN (and Fermilab)
 - Typical CERN TB
 - 6 layer of telescope
 - 3-5um pointing resolution
 - DUTs are in the cooling box







Noise increase by Biasing structure

- Higher noise in the pixel with BR observed
 - Depends on the FE circuit

First 65nm CMOS analog FE

testing chip (FE65p2)

~36e

- FE65p2:90e RD53A:215e effect
- Under investigation with chip designer.

0.12

0.1

0.08

0.06

0.04

0.02

~80e

No BR

100

Depends on resistivity of poly-si and capacitance between poly-si/Al

~100e

w/ BR

120

140

100



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40

60

Noise [e]

400

350

300

250

200

150 100

50

0

Number of Pixels

No BR

20

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200

(RD53A)

~230e

w/BR

400

300

bias

STD N⁺

STD N⁺

Large N⁺

500

Large N⁺ no bias

NoiseDist(N⁺ size)

- Compared top Al size

• Smaller Al have smaller noise

Affected by Capacitance between Poly-si and Al







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p+

- SiO2 thickness comparison
 - Compared SiO2 thickness btw Poly-si and Al
 - Thicker SiO2 have smaller noise
 - <u>Compared SiO2 thickness btw Poly-si and n+</u>
 - No visible difference

Affected by Capacitance between Poly-si and Al



12



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Poly-si resistivity comparison

– <u>Compare 0.67ΜΩ, 2ΜΩ, 6ΜΩ</u>

Larger resistivity have smaller noise

Highly affected by poli-si resistivity



NoiseDist(Poly-Si resistor)





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- Noise is affected by poly-si resistivity and capacitor btw polysi and Al
 - Tested Smaller top Al & thicker SiO2 & higher poly-si resistivity
 - Indeed the condition is the best, resistivity is highest contribution



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Poly-si resistivity after Irradiation

- Measurement done using TEG with the same poly-si resister pattern.
 - Compared various sheet resister target wafers.
 - Tested 0.6M Ω , 2M Ω , 4M Ω , 6M Ω
 - Can achieve >5MΩ









Noise measurement after irradiation

• For default type :

- Compared before and after irradiation

 Smaller noise after irradiation due to high resistivity after 3x10¹⁵n_{eq}/cm² irradiation



NoiseDist





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Efficiency loss due to charge sharing

- Charge sharing effect
 - After proton irradiation, about 8k electron-hole pair created by ionizing loss of MIP particle in 150um thick sensor.
 - At the corner of pixel, charge is splitting to 4 pixels (2ke each).
 - Efficiency loss occur if the comparator threshold of readout ASIC is >2ke.
 - In case of 50um x 250um pixel efficiency loss are ~1% to overall efficiency @ 2400e.
- Finer pixel size (50um x 50um)
 - expected to 5 times larger effect than 50um x 250um pixels.
 - Lower noise ASICs than FE-I4 helped to improve efficiency i.e. FE65p2 and/or RD53A
 - No visible efficiency drop for FE65p2 but there was issue for the absolute value of efficiency



Tested RD53A modules





K.Nakamura et. al. NIM A: doi.org/10.1016/j.nima.2018.09.015

Efficiency results (non-irrad)

- Results with 2000e thresholds.
 - Efficiency is over 99% for all types.
 - Still checking the proper mask has been applied.
 - No visible efficiency drop at the corner of pixel.
 - 20V is already enough voltage to have 99% efficiency.



Efficiency result (irrad 3x10¹⁵n_{eq}/cm²)

- Efficiency results of HV scan 200-800V have been evaluated.
 - Analyzed both 1500e and 2400e threshold data for different types.
 - All types have over 98% efficiency at 600V.
 - 1500e threshold results have over 99% efficiency.
 - Small n+ w/ BR have low efficiency at 200V



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Conclusion and plan

- Conclusion
 - Develop optimized sensor structure for HL-LHC ATLAS phase-II upgrade.
 - New sensor mask compatible to the RD53A ASIC has been developed.
 - Pixel with Biasing structure have larger noise.
 - Larger resistivity and smaller capacitance btw poly-si/Al improve this.
 - Best design have 150e increase by BR.
 - Efficiency results
 - Non-irrad sample have over 99% efficiency
 - Irrad module have over 98 % efficiency for both w/ and w/o BR.

Satisfied ATLAS ITK-pixel requirements

- Plan
 - Understanding the source of noise with Spice Simulation of RD53A ASIC with resister between input pads.
 - Quad sensor production as the final design of ATLAS ITk modules.

Contributer

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- Check only DIFF FE
 - Measured by threshold scan by YARR
 - -20V bias supplied.
 - Compered with and w/o Bias structure
 - No BR~ 80e, With BR~ 230e (increase 215e)
 - <u>Compared n+ size</u>
 - No major difference for both w/ and w/o BR.





NoiseDist(N⁺ size)

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Equivalent circuit



Equivalent circuit



Location of efficiency drop

 In case of small n+ size, Efficiency drop at the corner which wide bias rail located. (3x10¹⁵ irrad @800V)





Efficiency loss per pixel (FE-I4)



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Results : irrad 3x10¹⁵n_{eq}/cm² (FE65p2)

- Projection of In-pixel efficiency
 - For both 25x100um and 50x50um pixel size, efficiency loss at the pixel boundary at 600V are consistent to Zero. For 25x100um w/ bias str at 400V(left blue) E_{loss}=0.90±0.05%.
 - 200V 25x100um w/ bias str is also shown(left red).



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Flip chipping development

Development of Lead-free(SnAg) Bumpbonding (Since 2012)

- No Flux used 1.
 - confirmed flux improve connection, though

No backside compensation 2.

- Improvement of Vacuum chuck jig to hold and flatten the ASIC/Sensor...(jig size ~ FE-I4 area)
- Special UBM (key element: cannot tell *3*. much...)
- **Hydrogen plasma reflow** to remove surface **Final unit** 4.
- Thin sensor/Thin ASIC : 150um/150um
 - Established Bumpbonding method in the beginning of 2016.
 - Quite stable quality for both single and four ASICs. 100% yield for last one year (>100 chips are bumpbonded.)



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Optimization of Bias structure

Very first module HPK produced have critical efficiency loss at the inter pixel region.



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Optimization of Bias structure



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Charge sharing v.s. threshold 2016Aug Th3000e HV=1000V





2016Nov with 2200e HV=917V



Th3000e – Th2200e



Bias rail to GND v.s. floating

- We took testbeam data with floating Bias rail long time.
- For the ASIC point of view, amplifier should have low noise with bias rail to GND. (by Maurice.)







Bias rail to GND v.s. floating

- We took testbeam data with floating Bias rail long time.
- For the ASIC point of view, amplifier should have low noise with bias rail to GND.

Field to make efficiency drop by BR is milder in case BR floating?



