RADIATION-INDUCED EFFECTS ON DATA INTEGRITY AND -LINK STABILITY OF RD53A

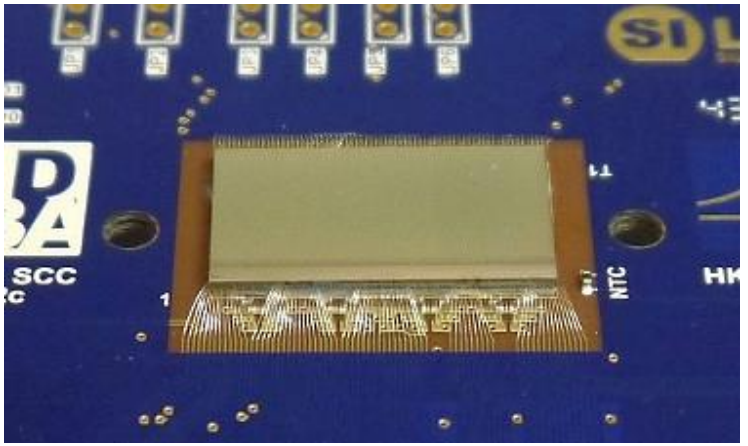
PIXEL 2018, TAIPEI

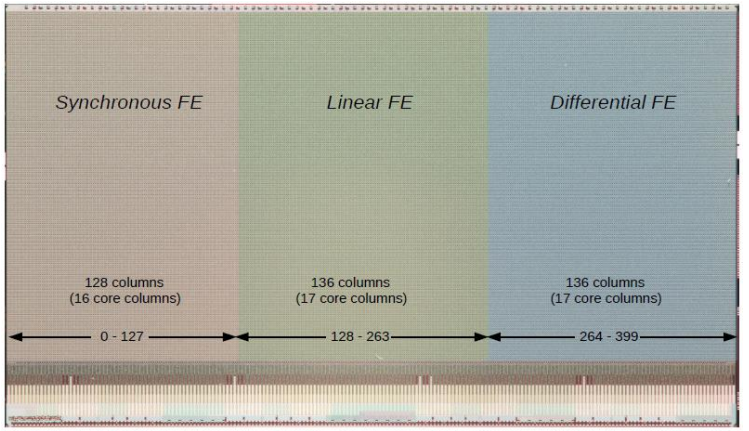
M. VOGT* ON BEHALF OF THE RD53 COLLABORATION

*PHYSIKALISCHES INSTITUT, UNIVERSITÄT BONN

INTRODUCTION - RD53A

- The **RD53 collaboration** is a common effort, shared between ATLAS and CMS
- Goal: Development of designs and methods for a hybrid pixel detector readout chip in a 65 nm technology
- **RD53A** is the first large (=half) scale demonstrator, produced in 2017, available for testing since 12.2017
- Features of RD53A
  - Three different analog frontend designs and two memory architectures for comparison
  - Fast data link to the readout system
    - Aurora protocol
    - Several configurable data rate options: 1x 640 Mb/s … 4x 1.28 Gb/s
  - Designed to withstand **at least 500 Mrad**





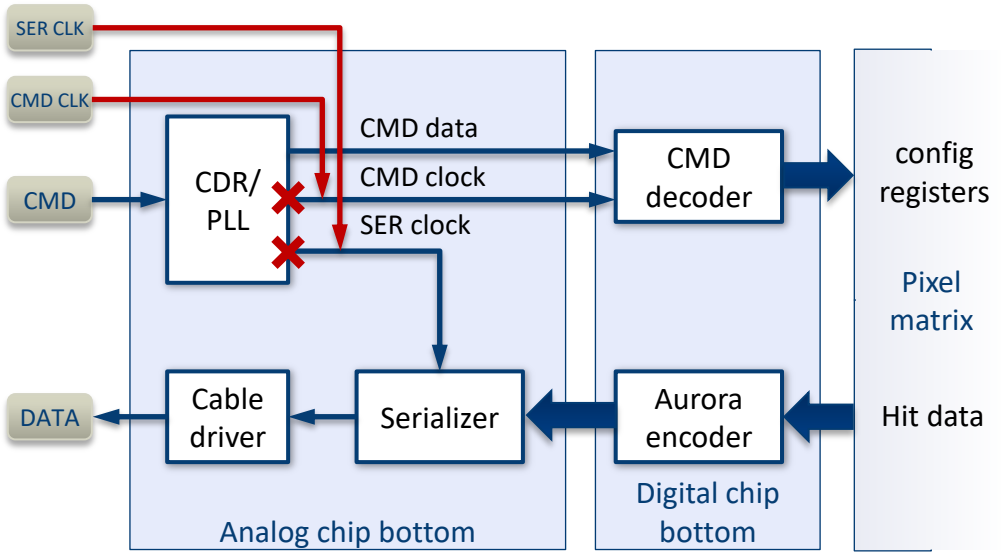
INTRODUCTION

- Motivation
  - Radiation effects in 65 nm CMOS have been modeled and studied for prototypes
    - Transistor level simulation model, using **worst case bias conditions**
    - **DRAD test chip** to study radiation effects on digital standard cells in 65 nm, agrees with models
  - In RD53, most of the previous irradiation campaigns focused on the analog front end performance
    → The digital performance of the prototype chip RD53A has to be studied, as RD53B is being designed
- Main focus of this campaign
  - **Data link stability and signal integrity**, as a function of V_{DDD}, f_{ref} and TID
- **600 Mrad** in multiple steps
  - Dose rate: 4.5 Mrad/h for the first 20 Mrad, then **6 Mrad/h**
  - During irradiation: The chip is cooled and operated with a monitor script (digital scan, threshold scan, temperature, power consumption)
  - At each TID step: Time consuming and detailed measurements like full shmoo scan and eye diagrams

INTRODUCTION - CDR BYPASS MODE

- Default operation mode: CDR/PLL block generates
  - **Command clock:** Recovered from the command data stream
  - **Serializer:** Multiplied (1,2,4,8) command clock
- In order to observe only the digital logic behavior, the chip was operated in **CDR-bypass** mode
  - Clocks have to be **provided externally**
  - **Generated by the FPGA PLL** of the readout system
    - CMD_CLK → **160** ± 20 MHz
    - SER_CLK → **640*** ± 80 MHz
      *(the chip was operated in 640 Mbit/s mode)

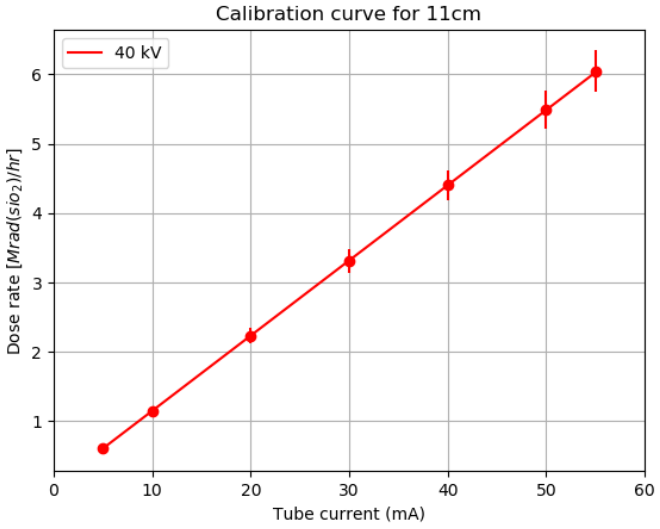
Fixed factor
(1, 2, **4***, 8)



Setup

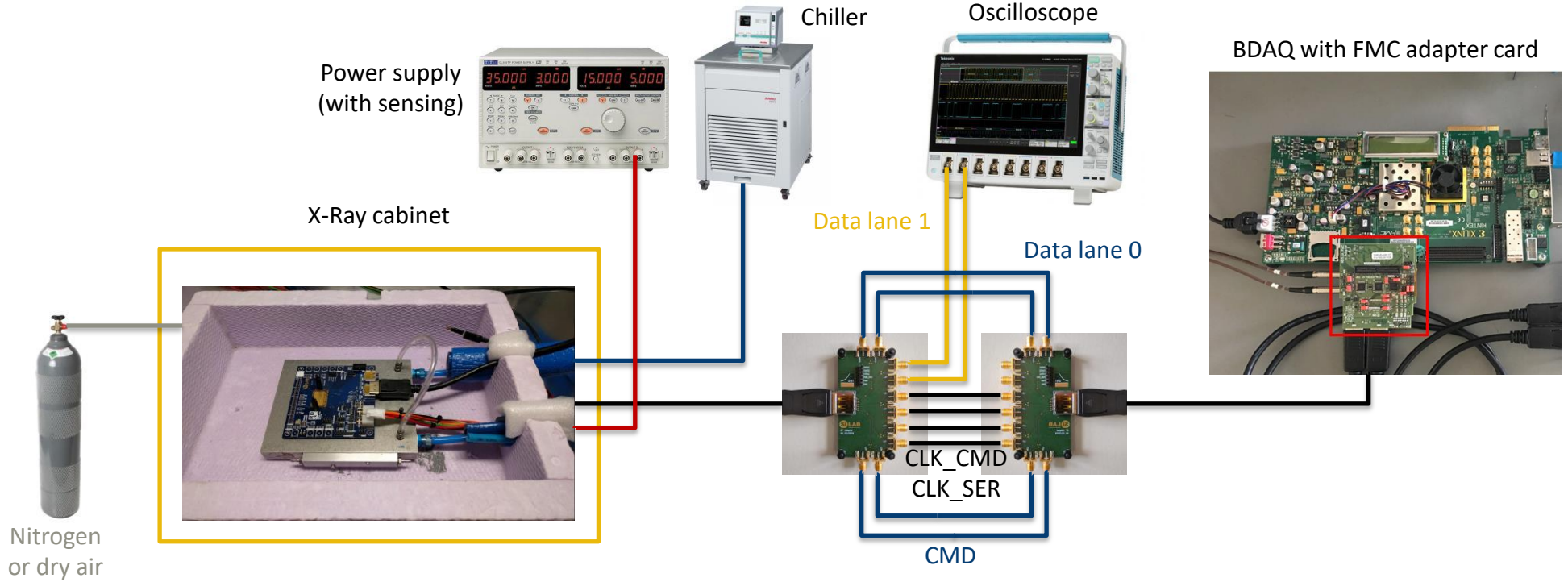
X-RAY SETUP

- X-ray cabinet
  - Tungsten target X-ray tube: 60 kV, 58 mA max
  - **Up to ~6 Mrad/h** at a beam spot diameter, suitable for RD53A (3 cm)



X-ray cabinet

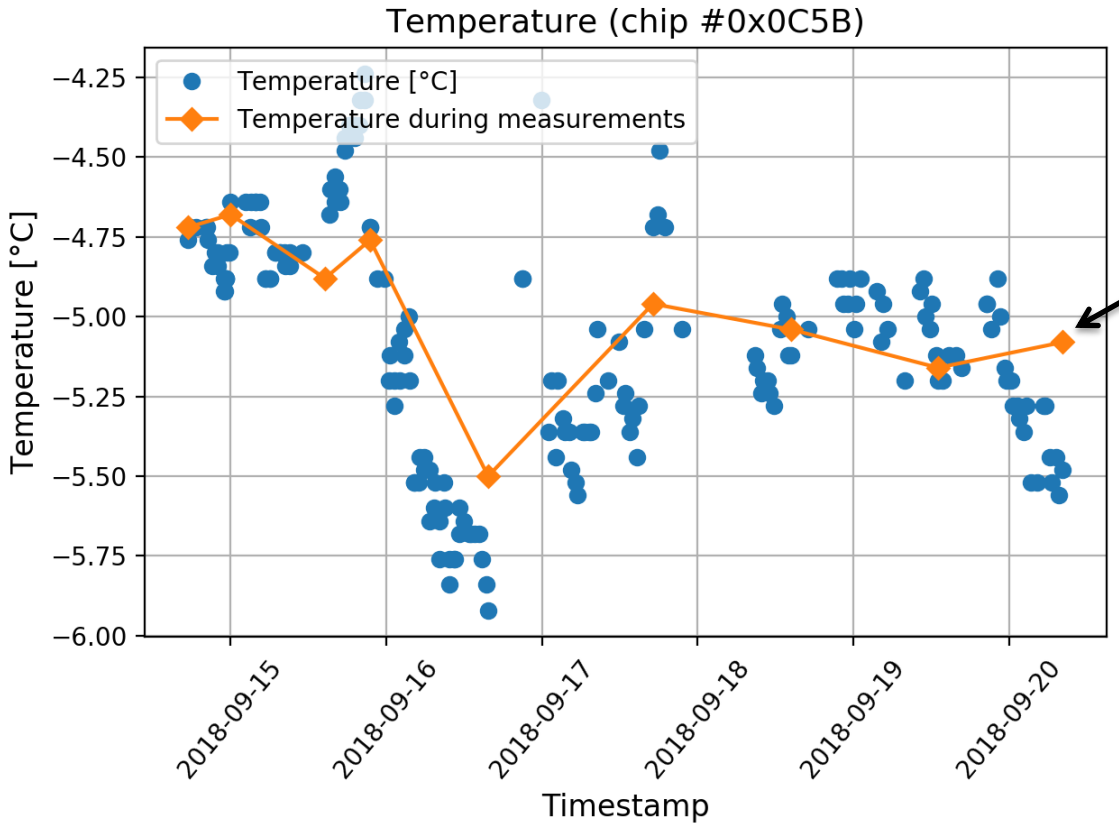
X-RAY SETUP



- The chip was operated in **direct powering mode:** Fixed V_{DDA}, variable V_{DDD}
- Data lane 0: DAQ, monitoring of the **serial data link status** (errors, sync losses)
- Data lane 1: Various data link parameters (**amplitude, eye opening, jitter**) were measured

TEMPERATURE CONTROL

- Temperature of the cooling plate set to $-5\ °C$
- Monitored close to the chip: Fluctuation of $\pm 0.8\ °C$ during the campaign

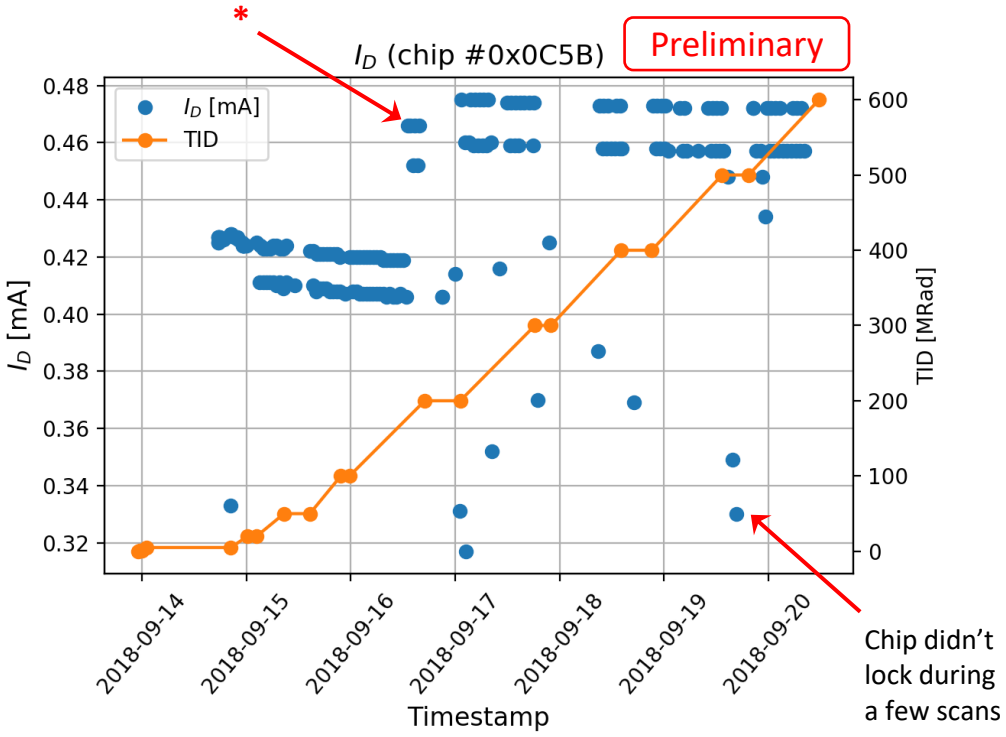


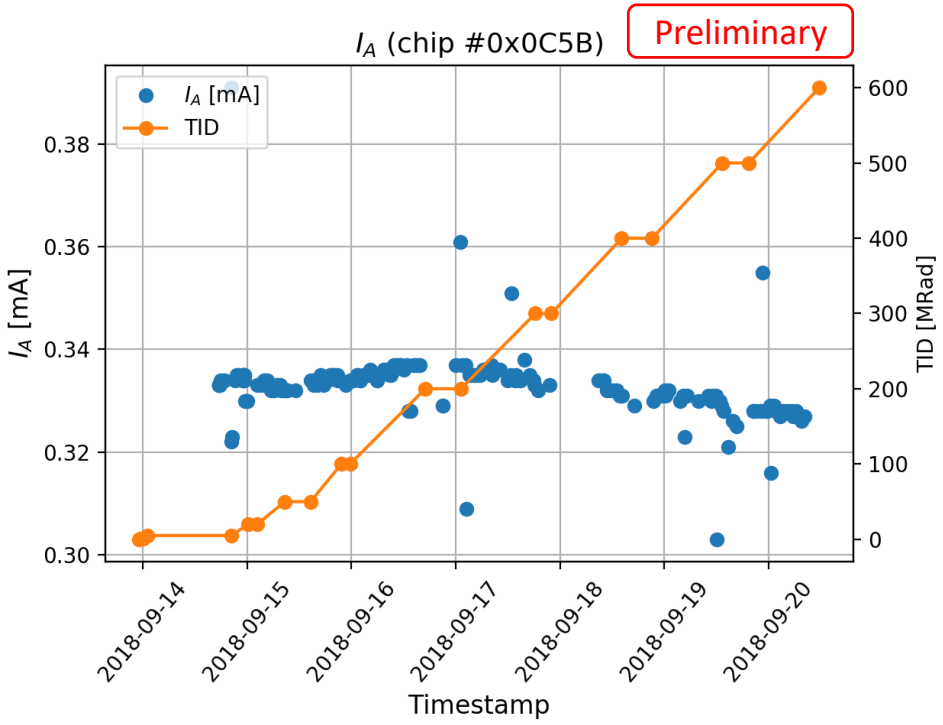
Measurements were performed at these temperatures

Results: Power and I_{ref}

CURRENT CONSUMPTION

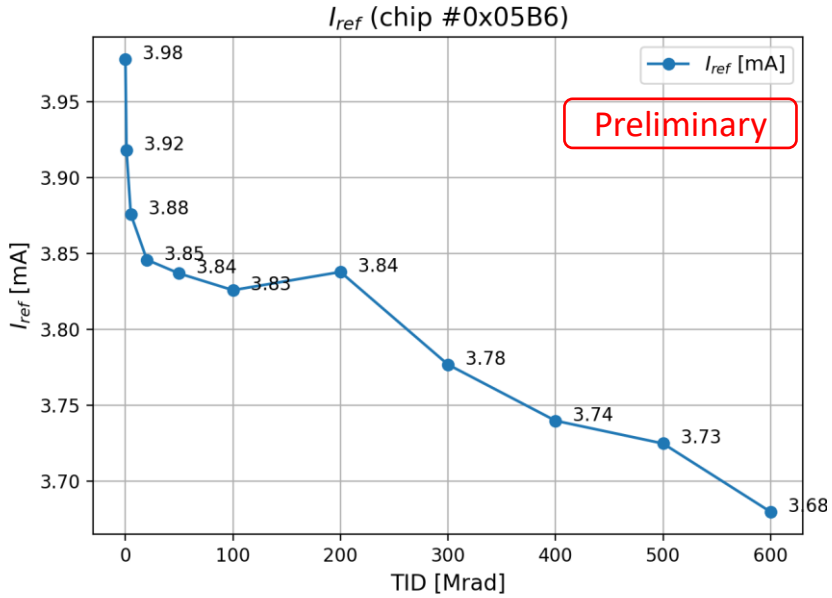
- Starting from 200 Mrad*, we enabled the clock to the complete pixel matrix
  → Increased digital power, slope barely affected
  → Slope for analog power changed





REFERENCE CURRENT

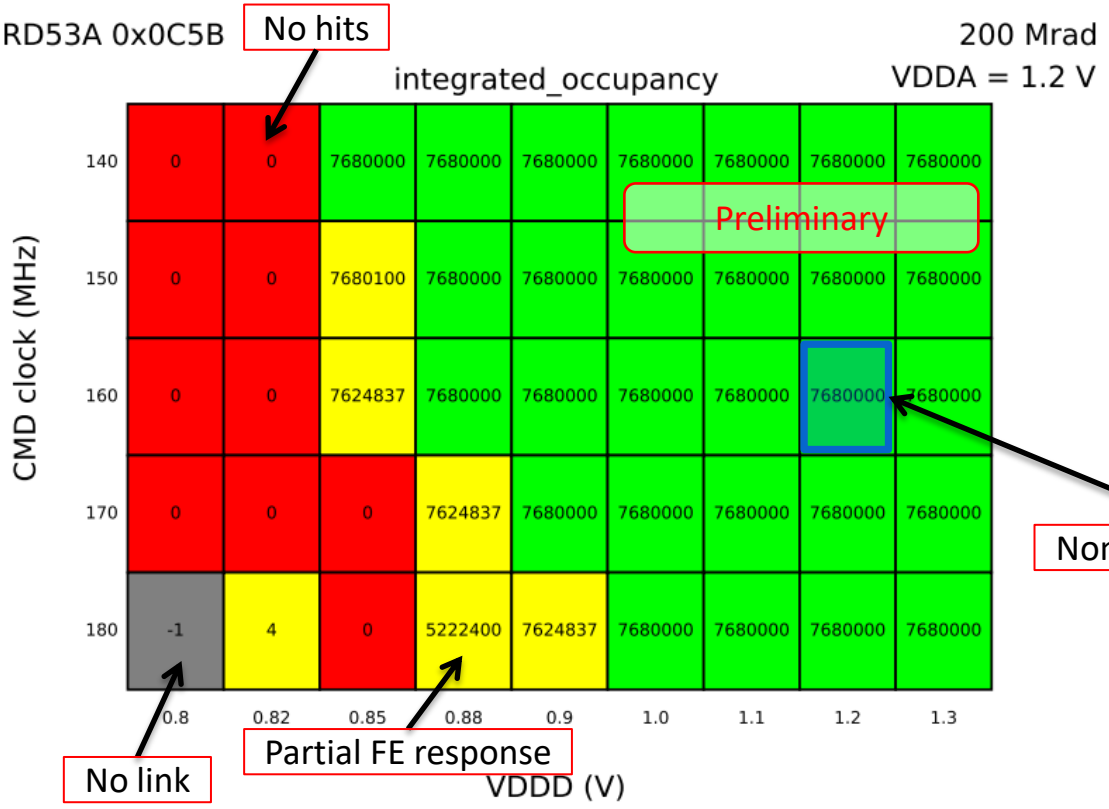
- RD53A uses a bandgap voltage reference and an **internal voltage divider** to generate its main reference current
  - Nominal value of $\boldsymbol{I_{ref} = 4\ \mu A}$ was trimmed before the irradiation
- During the campaign, I_{ref} **decreased by ~7.5%**
  - Caused by the **temperature-stable, but radiation sensitive** divider (poly silicon + diffusion resistor)
  - For RD53B, external resistors will be used instead



Results: Digital

DIGITAL SCANS – SHMOO PLOTS

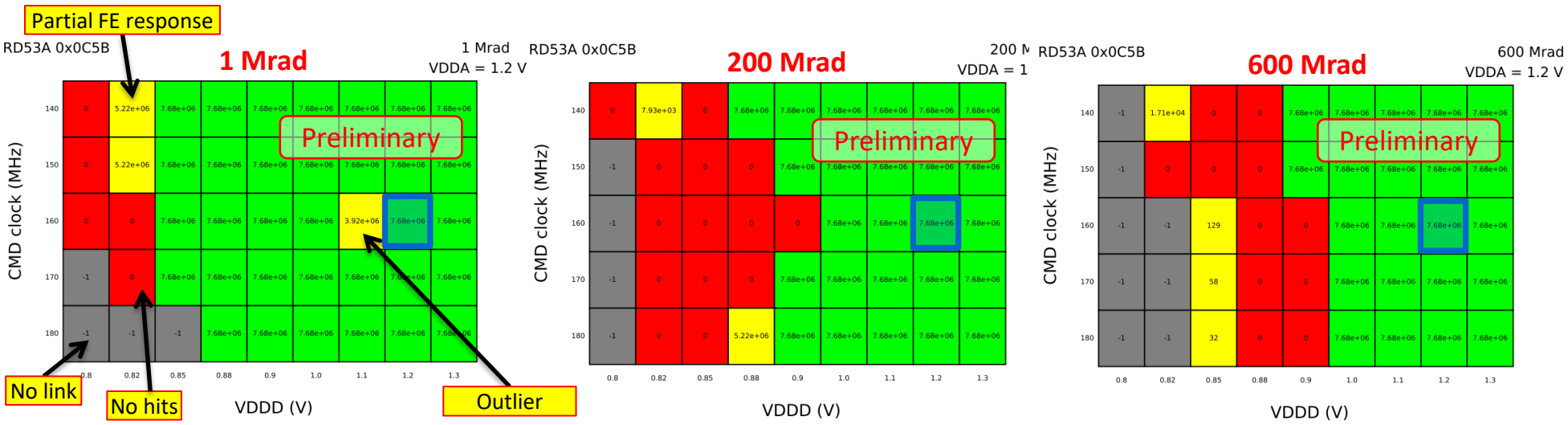
- Question: How large are the **margins** in terms of digital supply voltage and reference frequency?
- Method: **Digital scans within a parameter space** (V_{DDD}: $0.8 - 1.3\ V$, f: $140 - 180\ MHz$) with 100 injections into every pixel → Expectation: 7.68e6 hits



How to read the **shmoo plots**?

- **Grey**: No link → scan failed
- **Red**: No hits → Link established, but no FE response
- **Yellow**: Only partial FE response
- **Green**: Expected FE response

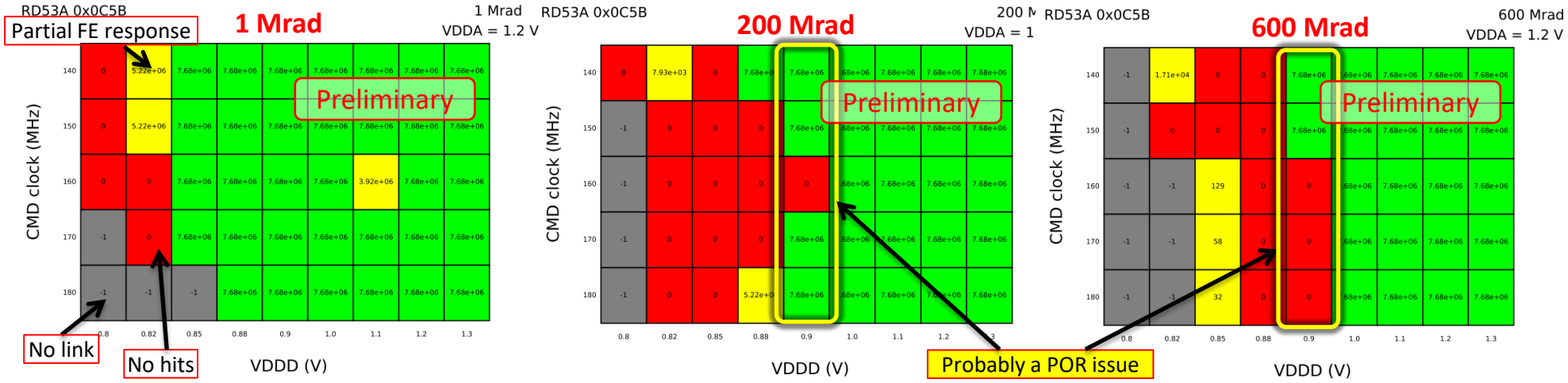
DIGITAL SCANS – SHMOO PLOTS

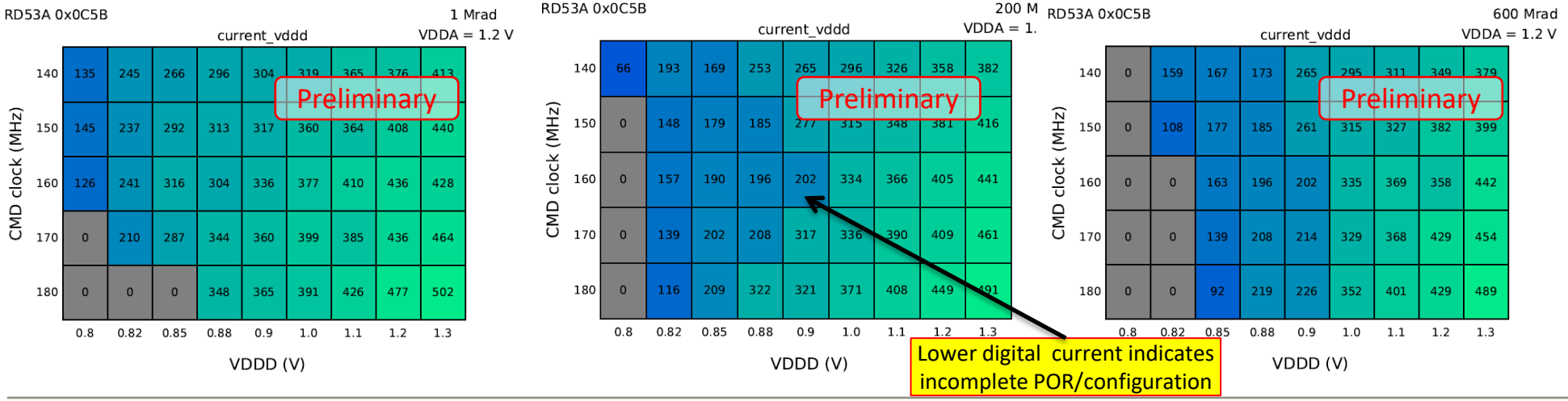


- With increasing dose
  - fewer combinations of operating condition are working
  - the margin decreases

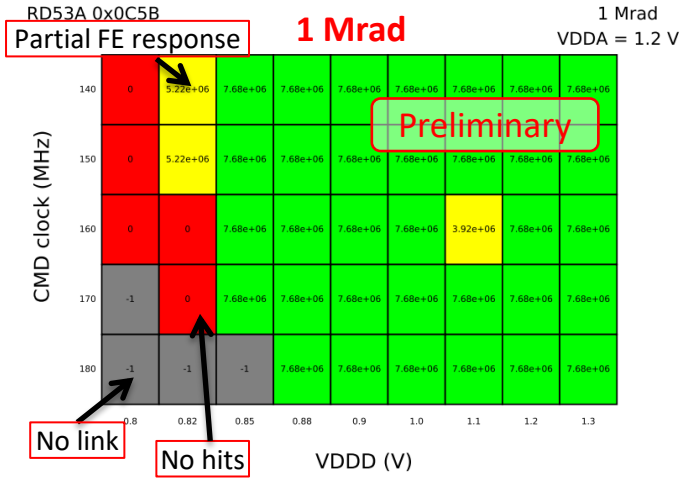
DIGITAL SCANS – SHMOO PLOTS

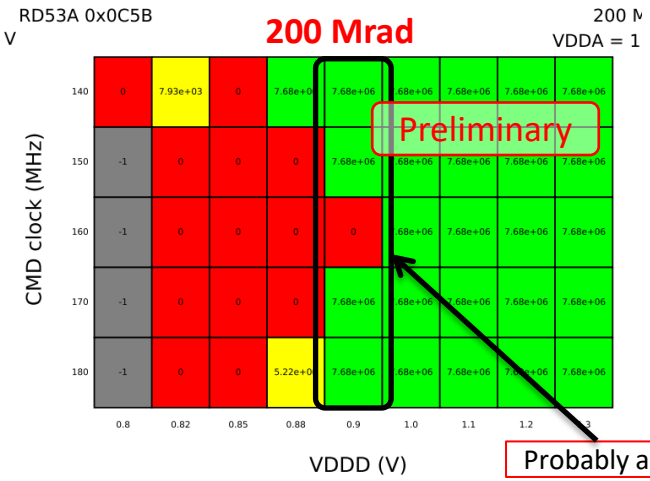
- The digital logic is supposed to work at 0.9 V after 200 Mrad (according to simlations)

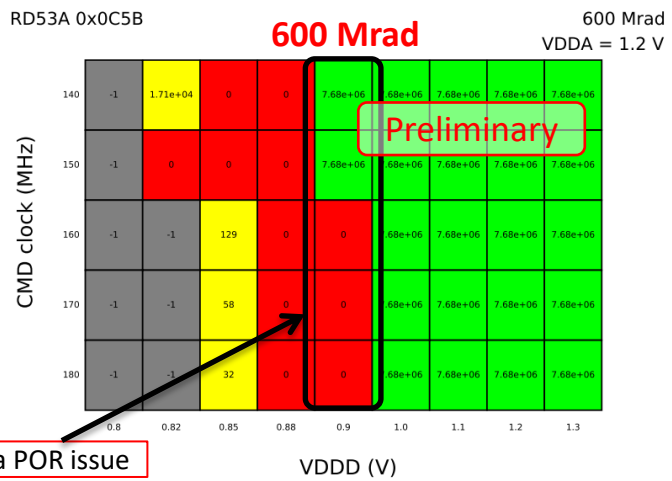




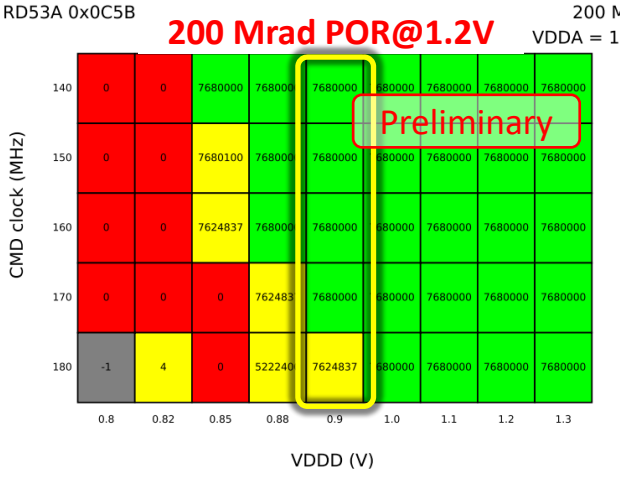
DIGITAL SCANS – SHMOO PLOTS

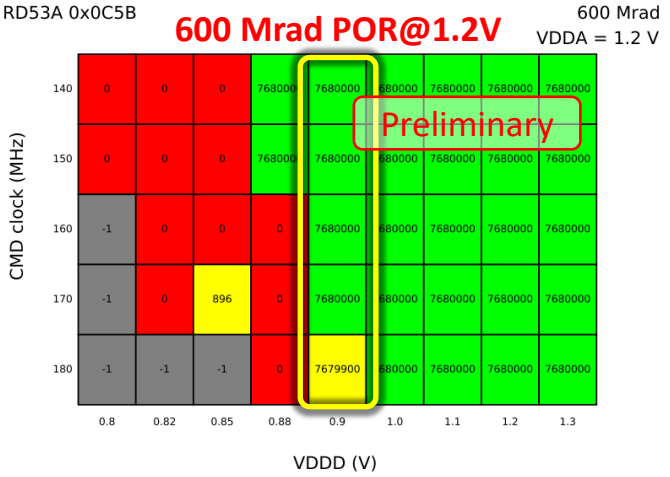






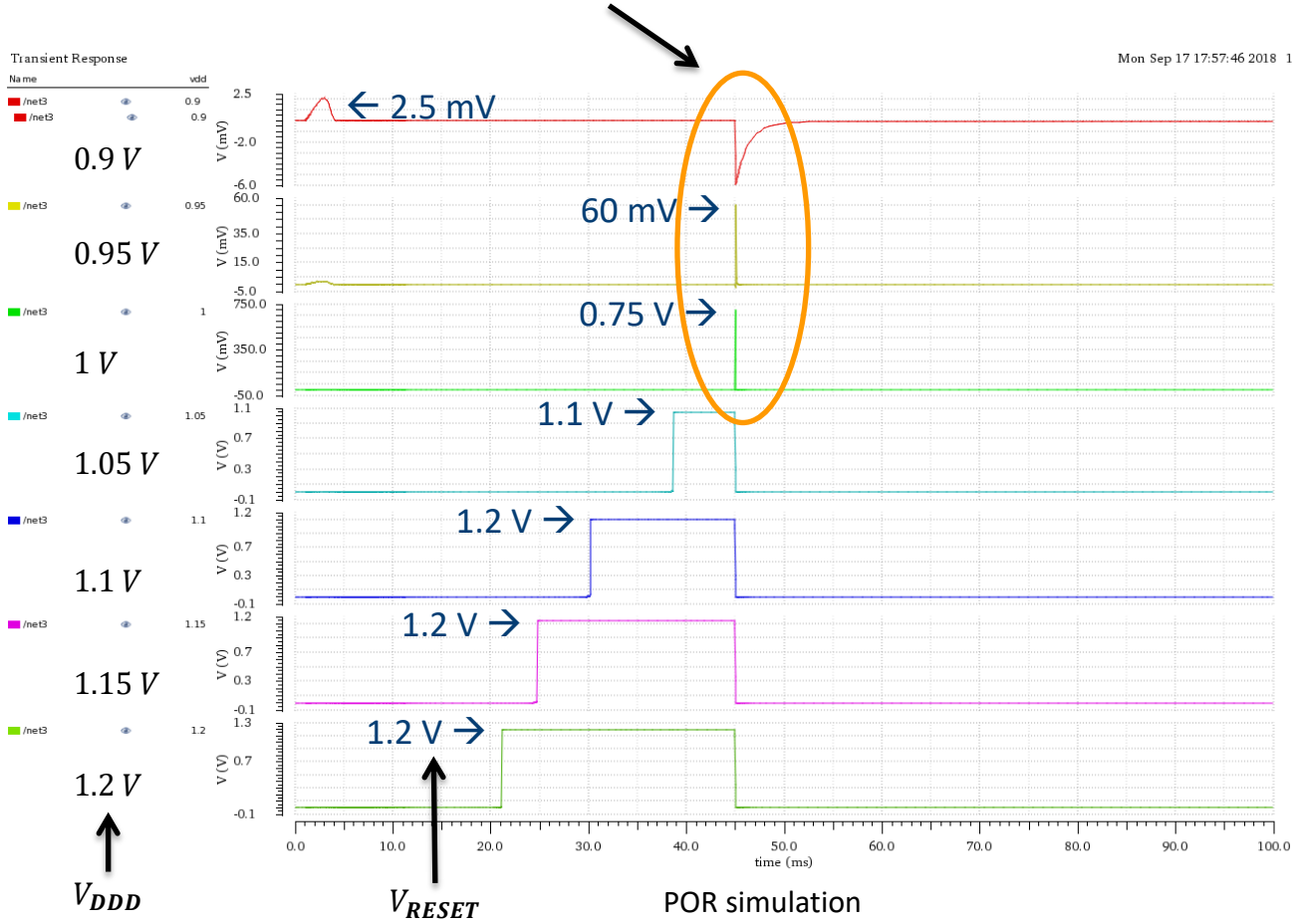
- Additional scan introduced with different reset conditions
- POR is more reliable, when the chip is first powered (and reset) at 1.2 V, before lowering V_{DDD}





POWER-ON RESET

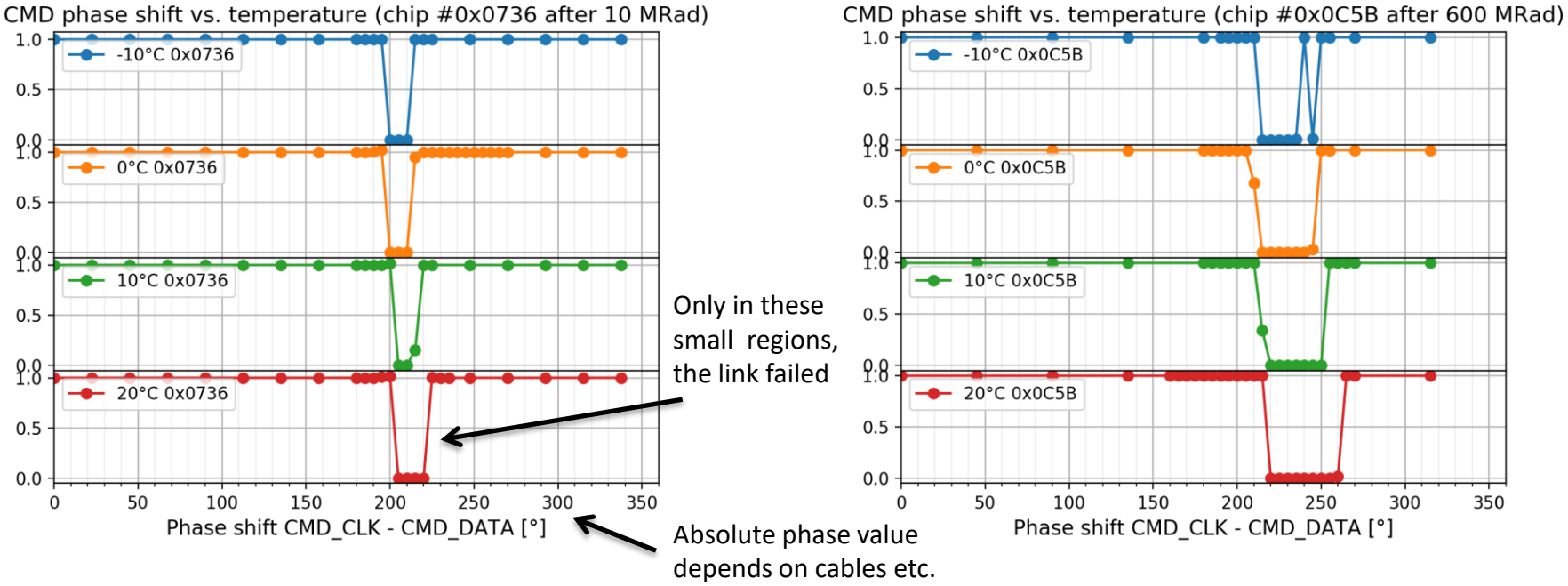
- The POR circuit was **designed using the analog corner** ($V_{min} = 1.08\ V$)
- With $V_{DDD} \leq 1\ V$, the reset signal is only a short pulse, which is **insufficient to reset the logic reliably**



POR simulation

COMMAND/DATA PHASE SHIFT

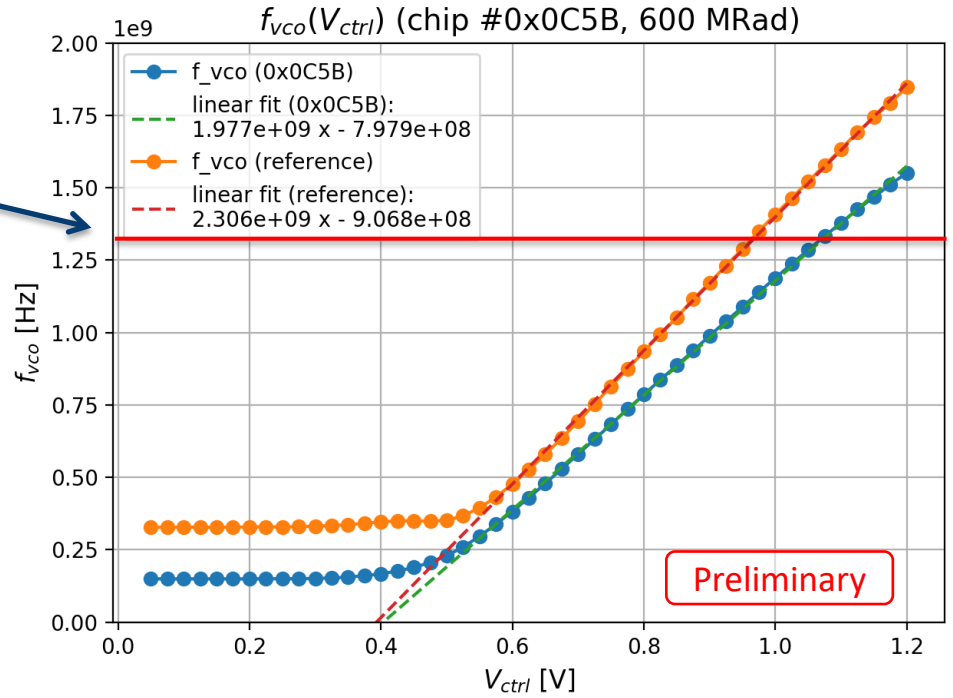
- **In CDR bypass mode**, the **phase** between command clock and data is critical
- Measurement with a controllable external two channel clock generator after the campaign:
  Ch1: FPGA (CMD data), Ch2: CMD clock to the chip. Phase between channels was varied
- The **setup- and hold timing** changes with temperature and dose
  - **Hold time** (distance between data transition and clock edge) **increases** by $\sim 0.5°/°C \; = \; 8.7\; ps/°C$
  - The critical **phase region increases** from ~20° at 10 Mrad to ~45° at 600 Mrad



PLL: VCO TUNING RANGE

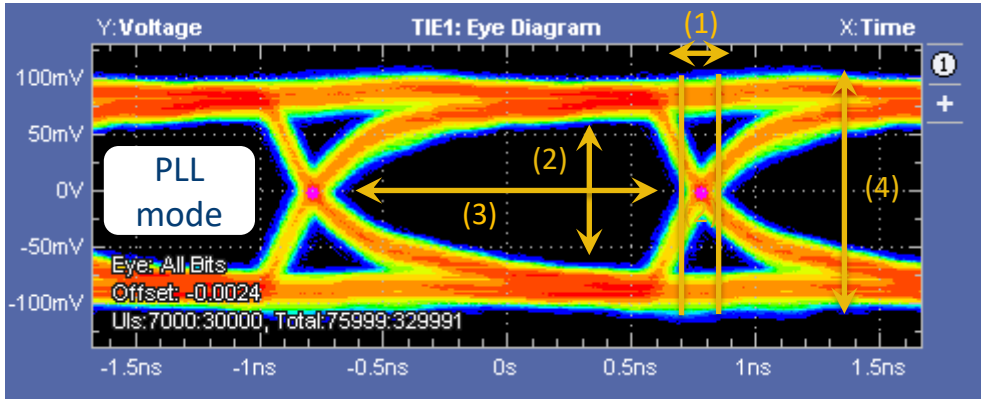
- In the default operation mode of the chip, a **CDR/PLL block** locks to the CMD clock and provides several clocks, derived from the internal VCO
- Measurement of the **VCO gain curve**
  - V_{ctrl} is scanned from 25 mV to 1.2 V, while the frequency is measured
  - Compared to a non-irradiated chip, the **VCO gain decreased** and the **frequency range shifted** slightly

Nominal VCO operating frequency: 1.28 GHz

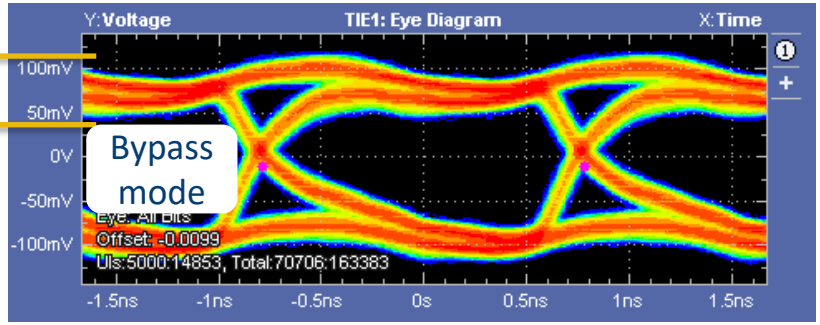


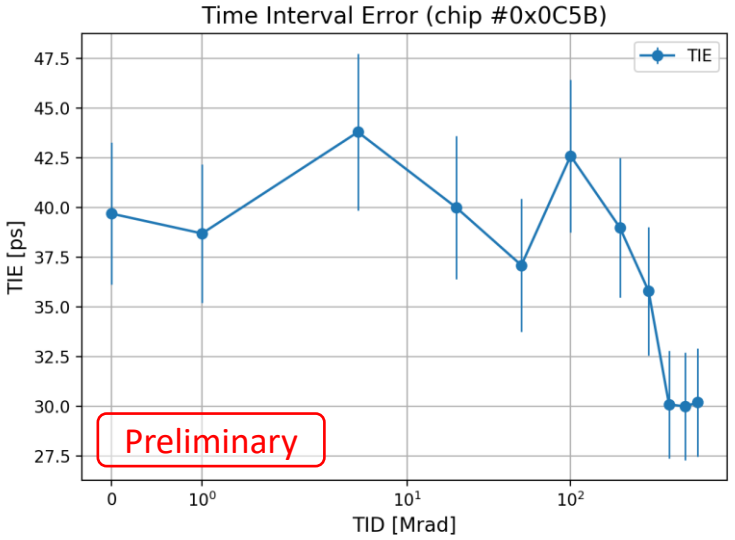
EYE DIAGRAMS

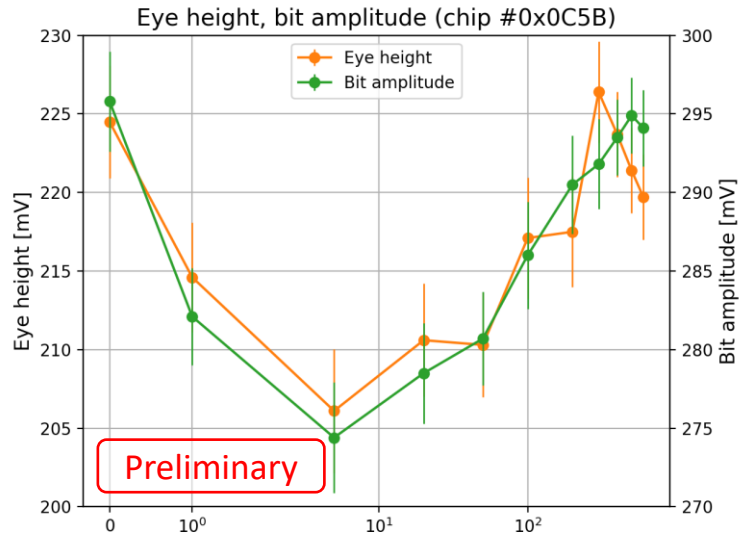
- Most interesting values from the eye diagrams
  - Time Interval Error: RMS of the total jitter (1)
  - Eye width(2), height (3): Define the eye opening, bit amplitude(4)
- **Cross-coupling** of SER_CLK can be seen on the data line: $\sim 50\ mV_{pp}$(4) in bypass mode – no issue for the data link



Cross talk in bypass mode (4)

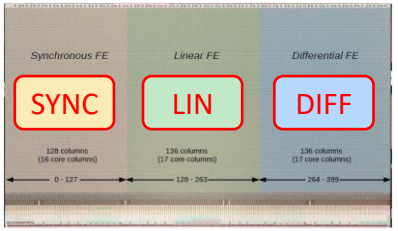






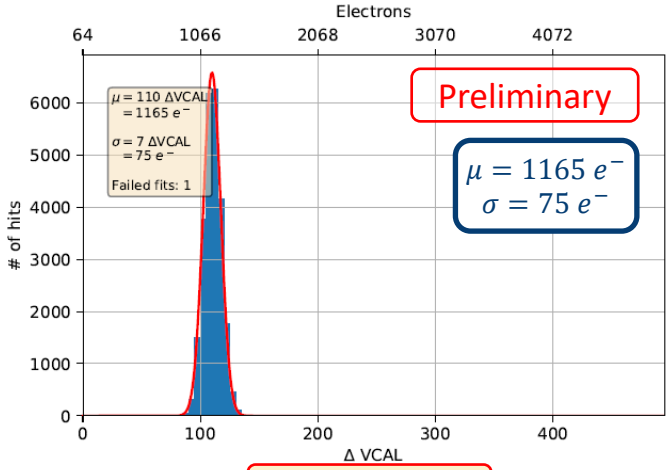
Results: Analog Front Ends

THRESHOLD



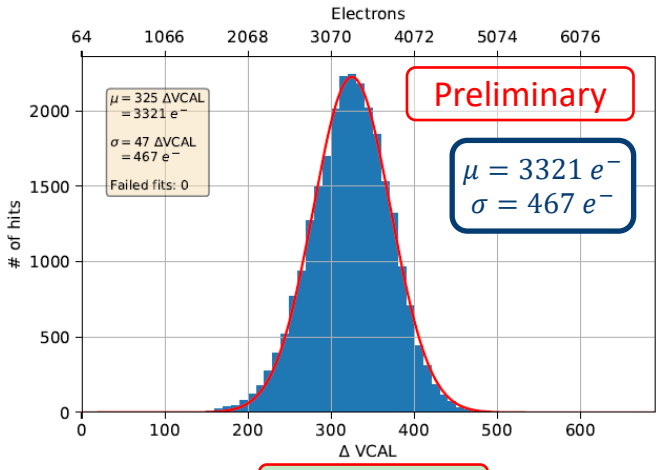
RD53A preliminary | 0 Mrad SYNC | Chip S/N: 0x0C5E

Threshold distribution for enabled pixels



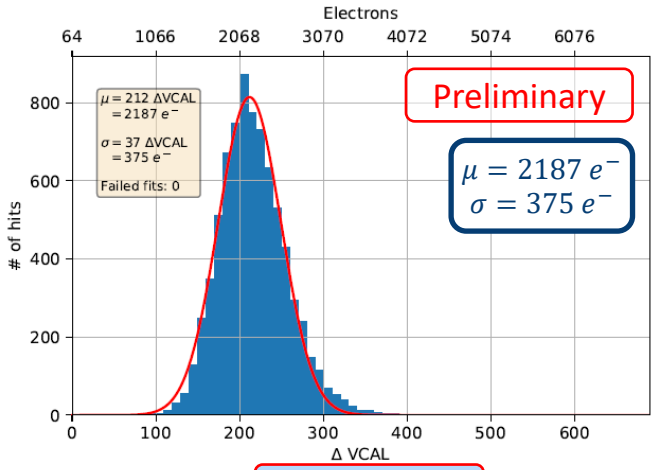
RD53A preliminary | 0 Mrad LIN | Chip S/N: 0x0C5E

Threshold distribution for enabled pixels



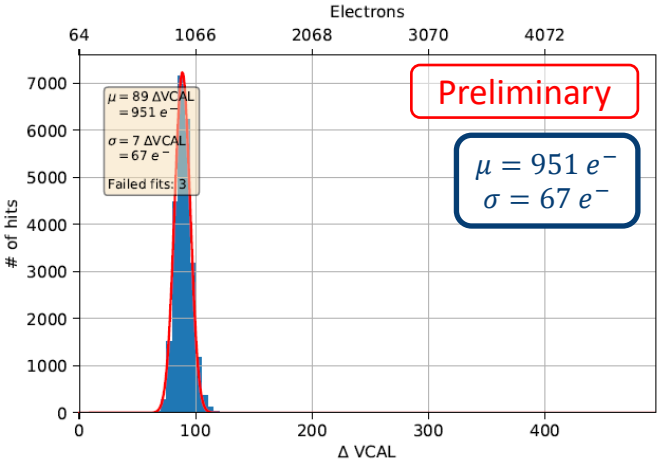
RD53A preliminary | 0 Mrad DIFF | Chip S/N: 0x0C5B

Threshold distribution for enabled pixels



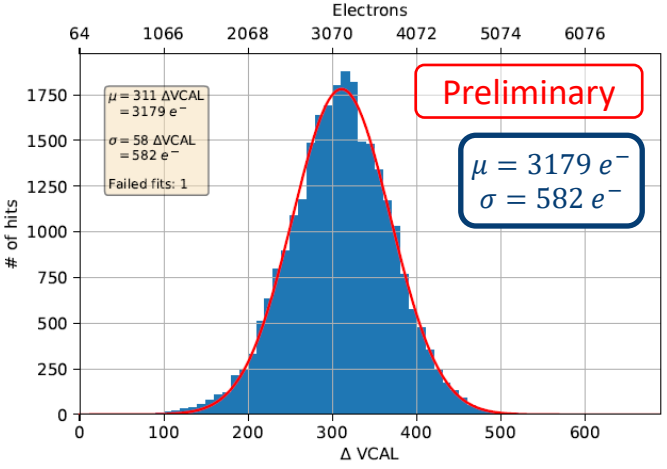
RD53A preliminary | 600 Mrad SYNC | Chip S/N: 0x0C5E

Threshold distribution for enabled pixels



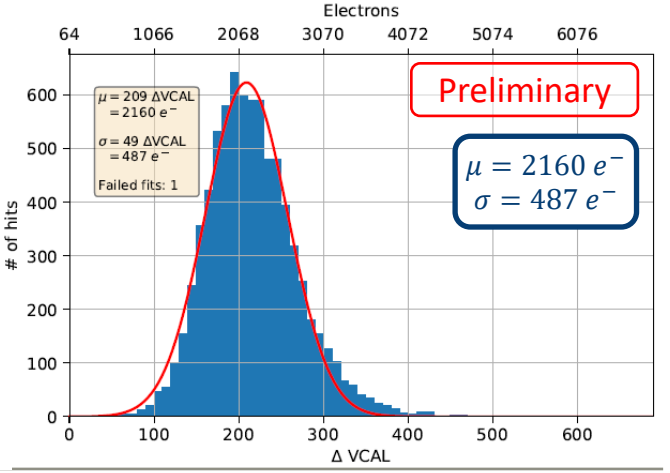
RD53A preliminary | 600 Mrad LIN | Chip S/N: 0x0C5B

Threshold distribution for enabled pixels

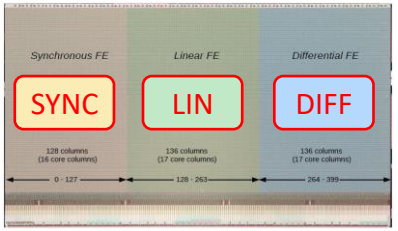


RD53A preliminary | 600 Mrad DIFF | Chip S/N: 0x0C5B

Threshold distribution for enabled pixels

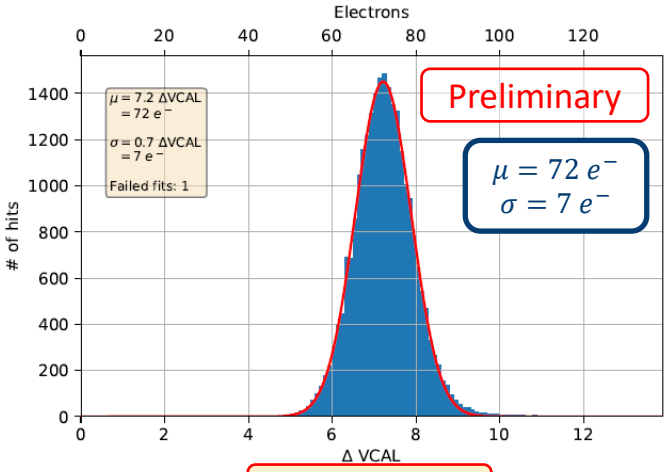


NOISE



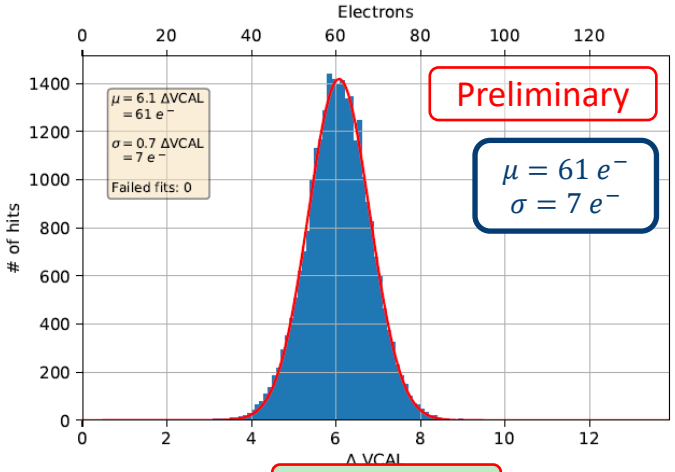
RD53A preliminary | 0 Mrad SYNC | Chip S/N: 0x0C5

Noise distribution for enabled pixels



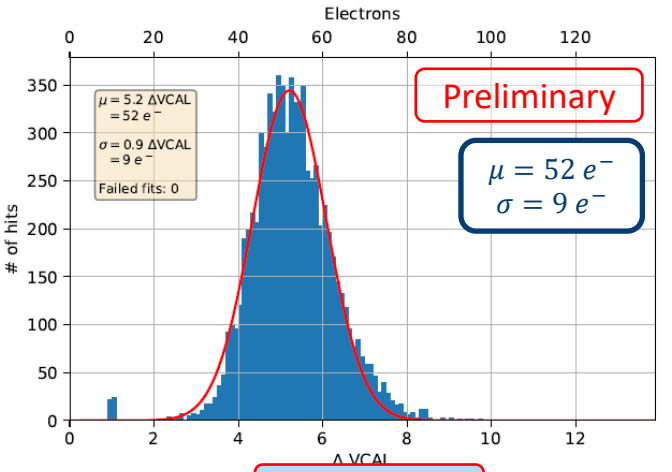
RD53A preliminary | 0 Mrad LIN | Chip S/N: 0x0C5E

Noise distribution for enabled pixels



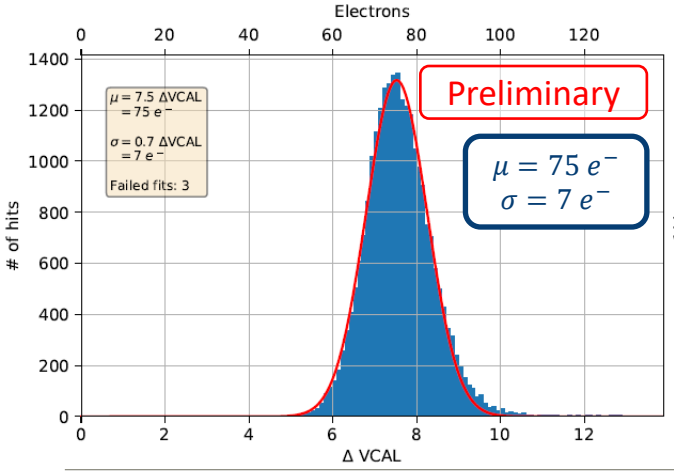
RD53A preliminary | 0 Mrad DIFF | Chip S/N: 0x0C5B

Noise distribution for enabled pixels



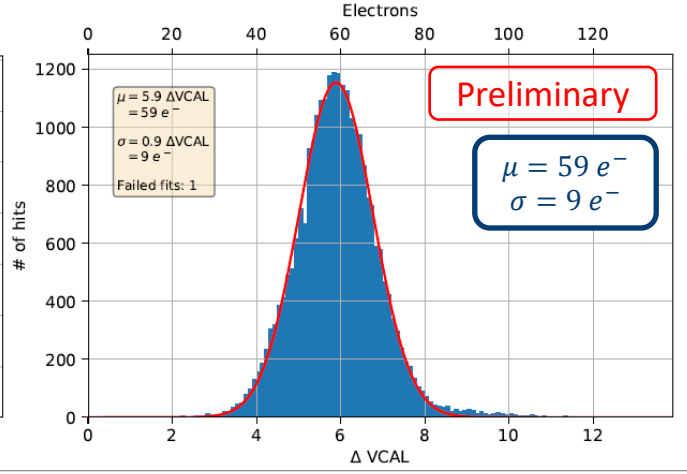
RD53A preliminary | 600 Mrad SYNC | Chip S/N: 0x0C5

Noise distribution for enabled pixels



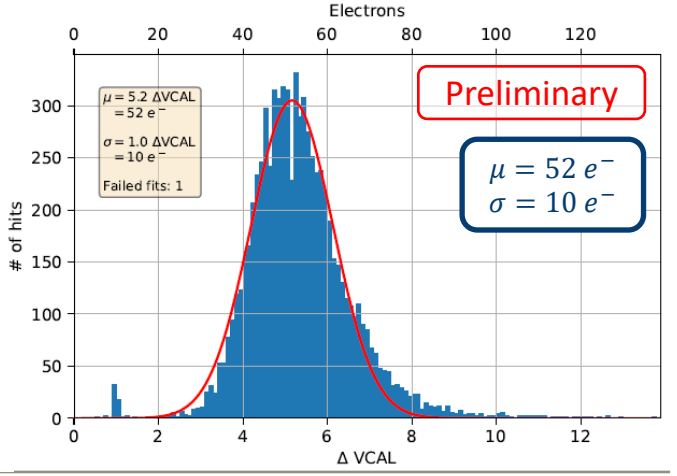
RD53A preliminary | 600 Mrad LIN | Chip S/N: 0x0C5E

Noise distribution for enabled pixels



RD53A preliminary | 600 Mrad DIFF | Chip S/N: 0x0C5B

Noise distribution for enabled pixels



CONCLUSION

- RD53A 0x0C5B has been irradiated to 600 Mrad
- Observations:
  - No significant degradation of the **cable driver** and the **VCO tuning range**
  - **POR** is not reliable at $V_{DDD} < 1\ V$ after 200 Mrad. Confirmed by simulation, to be improved in the next version.
  - I_{ref} **decreases** by ~7,5% → Mitigation by usage of external precision resistors for RD53B
  - **Operational temperature critical** after irradiation (need to stay below ~-10 °C for stable operation)
- Future plans
  - Irradiation of a few samples to different TID
  - Non-uniform irradiation
  - SEU/SET studies

UNIVERSITÄT BONN

THANK YOU

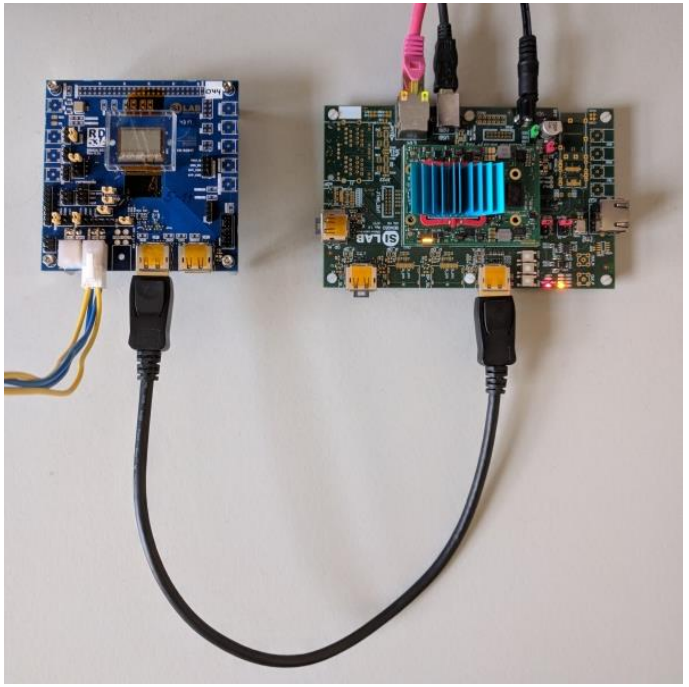
Backup

BACKUP - READOUT SYSTEM

Two readout systems for testing have been developed within the RD53 collaboration

- **YARR**: Comprehensive PCIe-based readout system with software framework written in C
- **BDAQ53**: Easy to use characterization and verification environment based on Python

- Main purpose: **Evaluation of** the **RD53A** prototype chips:
  - Electrical characterization (single chip)
  - test beam performance measurements
  - multi-chip (module) tests
  - wafer-level tests with a probe station
- BDAQ53 was used for this campaign: Ease of use
  - Single board, no additional adapters
  - Ethernet interface
  - No specific PC needed, even works with a Laptop
  - Python based software: Fast debugging
  - Alternative HW platforms supported: Xilinx KC705, USBPix3



BDAQ53 setup with RD53A Single Chip Card

BACKUP - BDAQ53 FIRMWARE

- Several firmware modules are instantiated from the Basil firmware library (FIFO, GPIO, I²C etc.)
- "Basil Bus"
  - Simple 32-bit wide bus for internal control signals
  - Firmware modules are addressed
  - Bus master: Interface to the SiTCP Ethernet IP core (1Gbit/s)
- AXI4-Stream
  - Aurora IP core from Xilinx (GTX transceivers)
  - Wrapper translates to the generic FIFO-style interface of SiTCP
- Command encoder
  - Programmable sequencer
  - Arbitration of triggers and idle/sync patterns
- Future plans
  - 10 Gbit/s Ethernet for SFP+
  - DDR3 memory FIFO