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VeloPix readout and ASIC

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This presentation will describe the ASIC and readout system designed for the new pixel vertex detector (VELO) of the upgraded LHCb experiment. All elements of the new electronics readout chain will be designed to cope with the requirement of 40 MHz full event readout rate. The pixel sensors are equipped with the VeloPix ASIC and placed at 5 mm from the beam in a secondary vacuum tank and extremely high and inhomogeneous radiation environment.

The VeloPix ASIC has been designed for data-driven readout in the trigger-less architecture of the experiment, where particle rates reach up to 800 million particles per second per cm^2, resulting in an unprecedented peak data rate of nearly 15 Gbit/s for a single ASIC. The data rate envisaged for the 41M pixels of the whole VELO will be 1.6 Tbits/s. The use of 'super pixels'and a novel architecture for the internal data-path ensures a nearly dead-timeless and very power efficient readout. Each module houses six VeloPix hybrids, wire bonded to two front end hybrids. These are connected via low mass flex tapes to a control hybrid which routes the high speed signals and transmits the control signals from the GBTx ASIC using one up and one down link of 4.8 Gbps. Small tapes (15 cm) with micro strip lines then route the high speed signals, reducing the material in the acceptance area. In the next step the signals are transmitted to the wall of the vacuum chamber at rates of 5.12 Gbits/s via 56 cm long flexible copper low mass tapes. A custom board routes the signals outside the vacuum tank and once on the air side, an Optical and Power Board converts the electrical high speed signals into optical signals for transmission from the cavern to the surface. Because of the great importance of the (nearly) faultless transmission of data at very high speeds, we have carried out a long campaign of simulations and measurements of the whole transmission chain during the past five years and performed Bit Error Rate, S-parameter, eye diagram and impedance studies.

Given the proximity to the LHC collisions region, the ASIC has to withstand extreme radiation doses of 370 MRad and $8x10^{15}$ 1MeV neq cm^{-2}. Test results of a total ionising radiation dose with X-rays and of single event upset and latch-up with heavy ion beams showed that logic cells of a custom library were vulnerable to latch-up, which could be nicely confirmed by use of a micro-focussed laser charge injection and comparing to prediction from CAD layout. The pixel analogue preamplifier and discriminator have been designed for low noise and time-walk to guarantee high efficiency on low charges collected from heavily irradiated sensors. A local in-pixel adjustment circuit provides a very uniform single threshold operation. The ASIC is produced in a commercial 130nm technology and results of wafer-probe tests will be shown.

The architecture of the readout chain from the point of view of high speed signals and the performance will be described, together with the latest results from the VeloPix ASIC.

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