Development and Performance of Phase-I Pixel DAQ in 2018

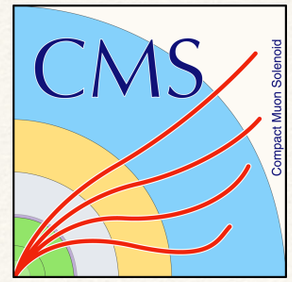
Pixel2018
Taipei, Taiwan

Atanu Modak,

Kansas State University (USA)

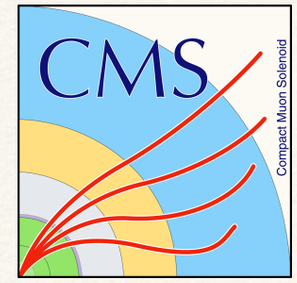
On behalf of the CMS Collaboration

Outline



- Pixel Detector
- DAQ System
- Pixel Online Software
- Firmware development
- Soft Error Recovery
- Monitoring
- Long Shutdown 2 Plans
- Summary

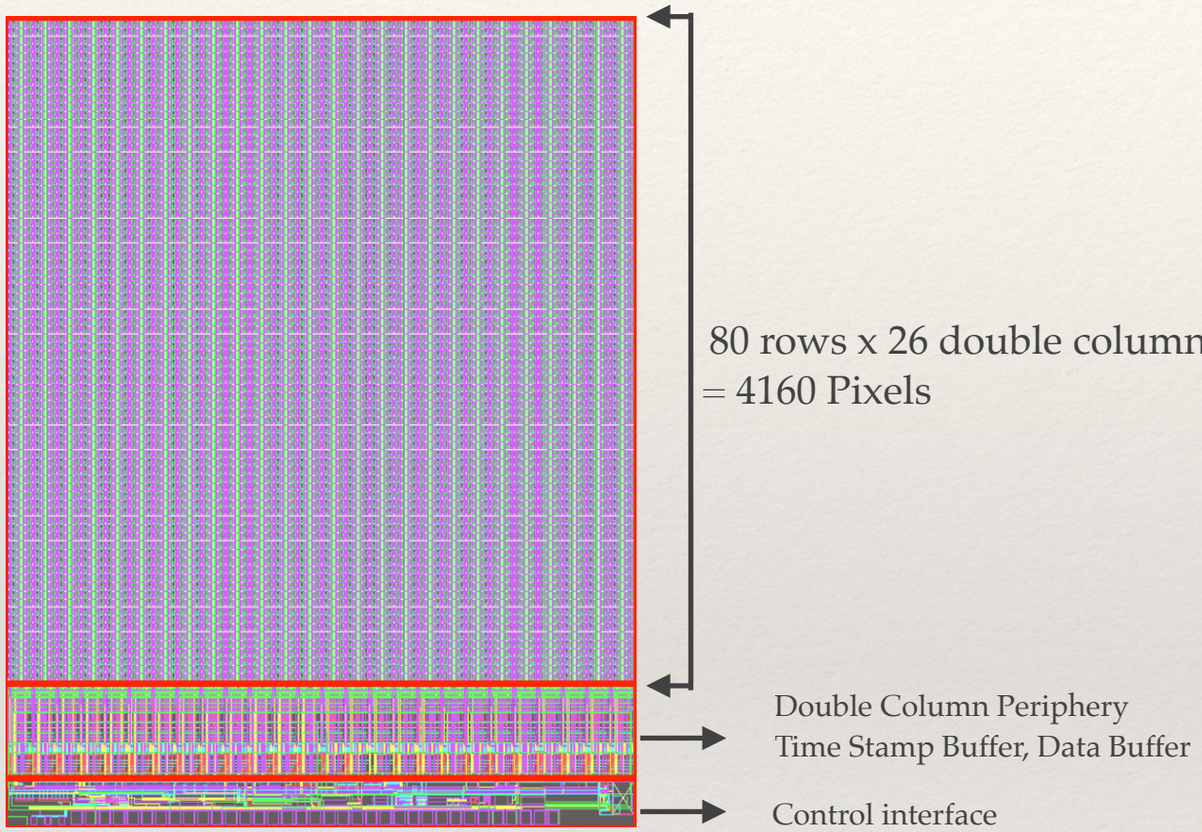
Phase-I Pixel Upgrade



- Pixel detector with one additional barrel layer and end-cap disc after Phase-I upgrade
- New front-end readout chip to cope with the higher particle hit rates
- Moved from 40 MHz Analog to 160 MHz Digital readout
- uTCA based backend DAQ to handle increased number of readout channels, higher data rate and new digital data format

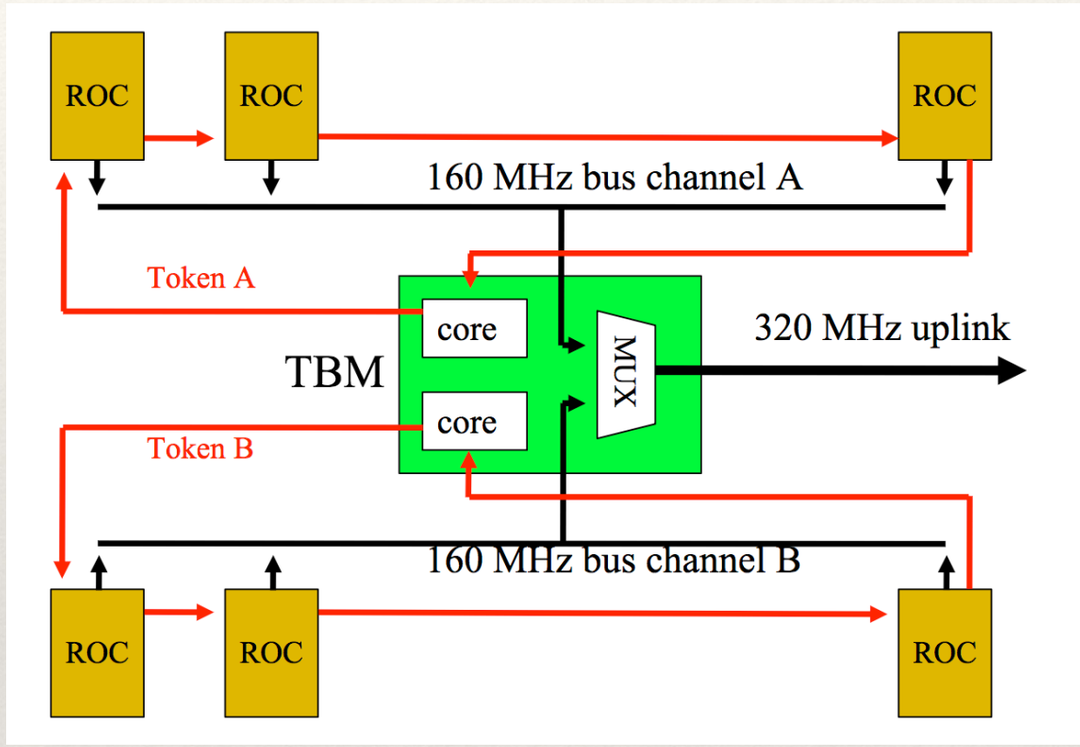
Front-end

Layout of the read out chip (ROC)



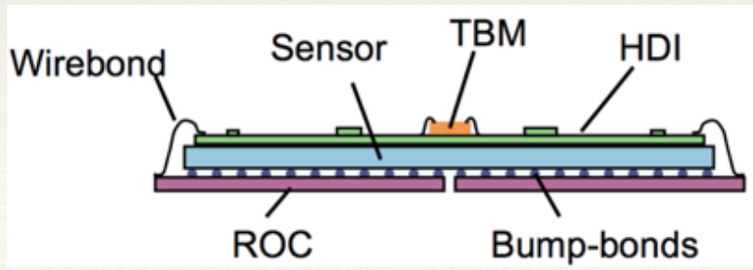
- 8 bit ADC
- Increased buffer size for timestamp (24) and data (80)
- Digital data transmission
- Digital readout at 160 MHz

Token Bit Manager (TBM) block diagram

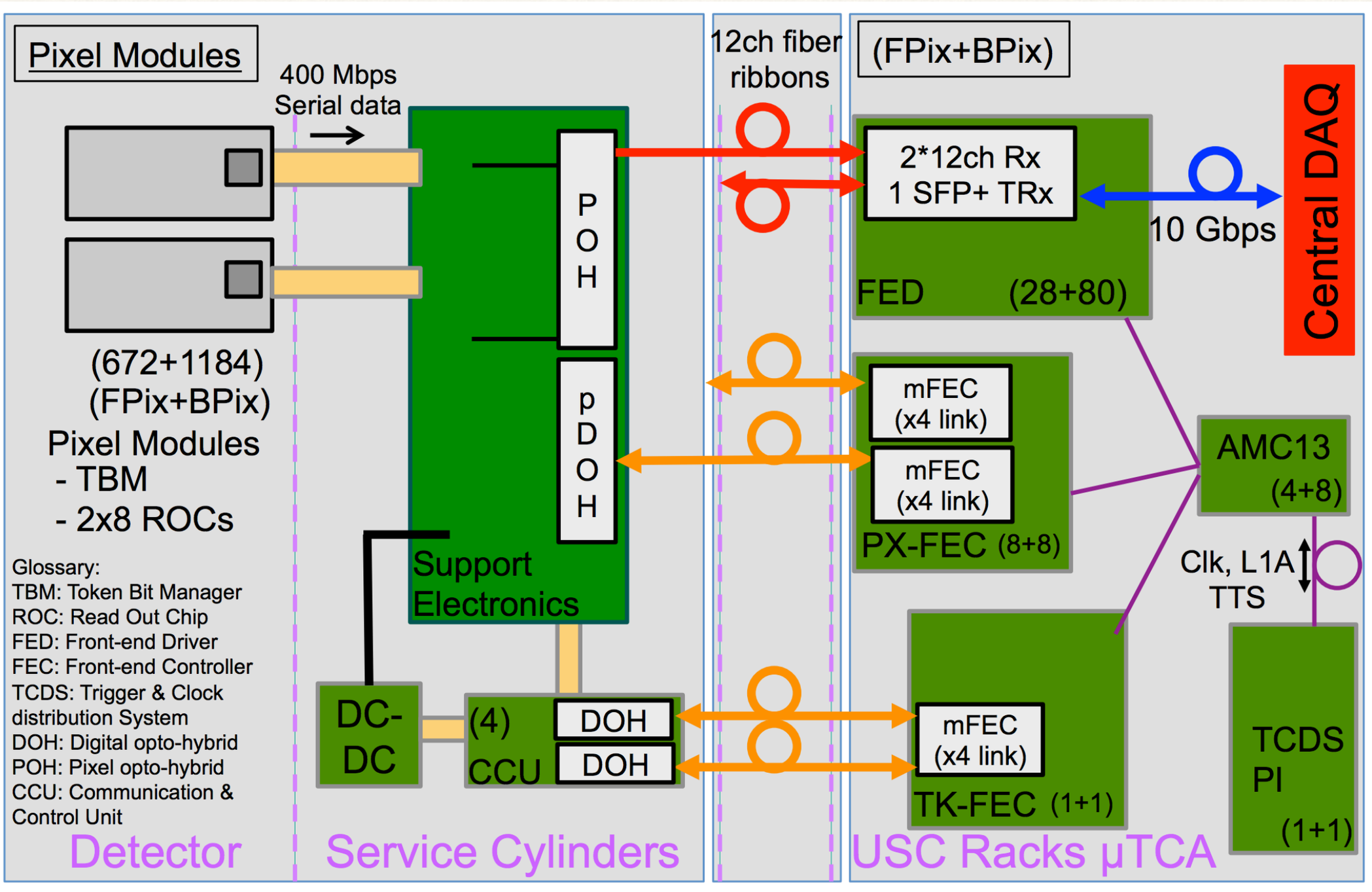


- 160 MHz digital readout scheme
- 2:1 multiplexed, 4-to-5 bit encoded data stream
- 2x160 Mbps from TBM cores A&B to 320 Mbps output

Schematic of a typical module



Pixel DAQ Architecture

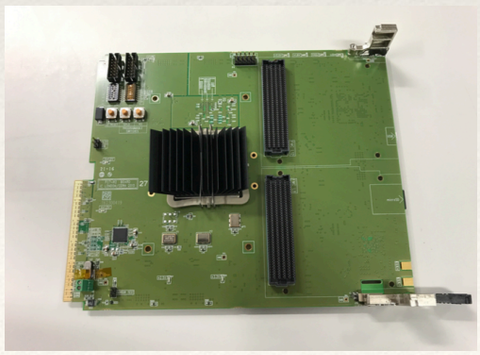


Pixel DAQ Hardware

- Pixel backend DAQ is based on Micro Telecom Computing Architecture (uTCA) standard
- Front-end drivers (FED) and Front-end Controllers (FECs) have custom uTCA cards based on FC7
  - Same hardware, different firmware
  - Optical mezzanine

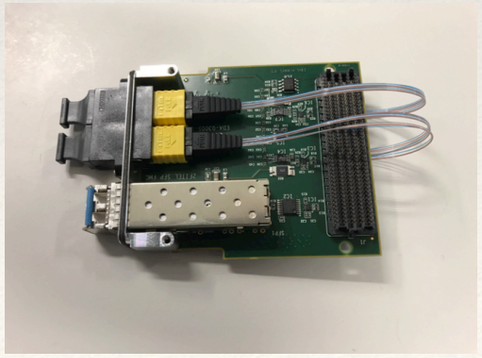
- **Tracker FEC:** Program auxiliary electronics (CCU, Portcard, Opto-hybrids etc)
- **Pixel FEC:** Distribute clock, trigger, fast signals to modules. Program Modules
- **Pixel FED:** responsible for data read out from modules and transfer it to central DAQ

FC7 Front

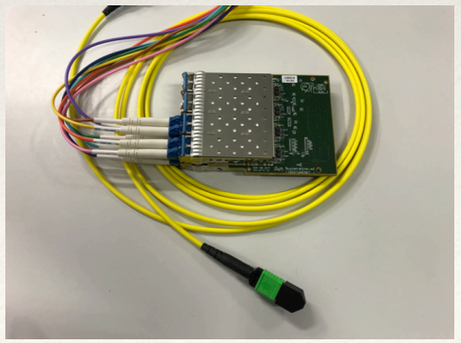


FC7 Back

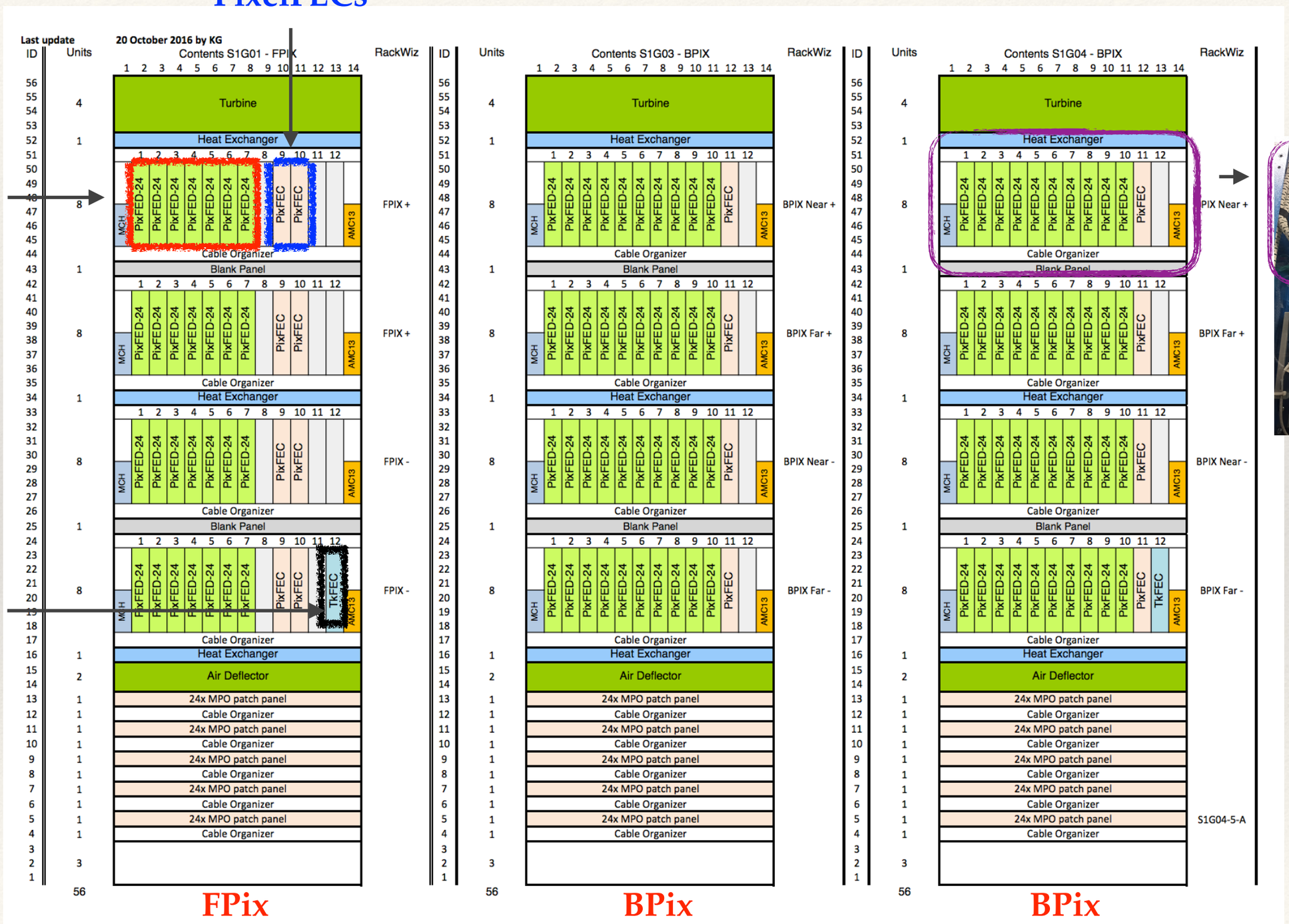
FED Mezzanine



FEC Mezzanine

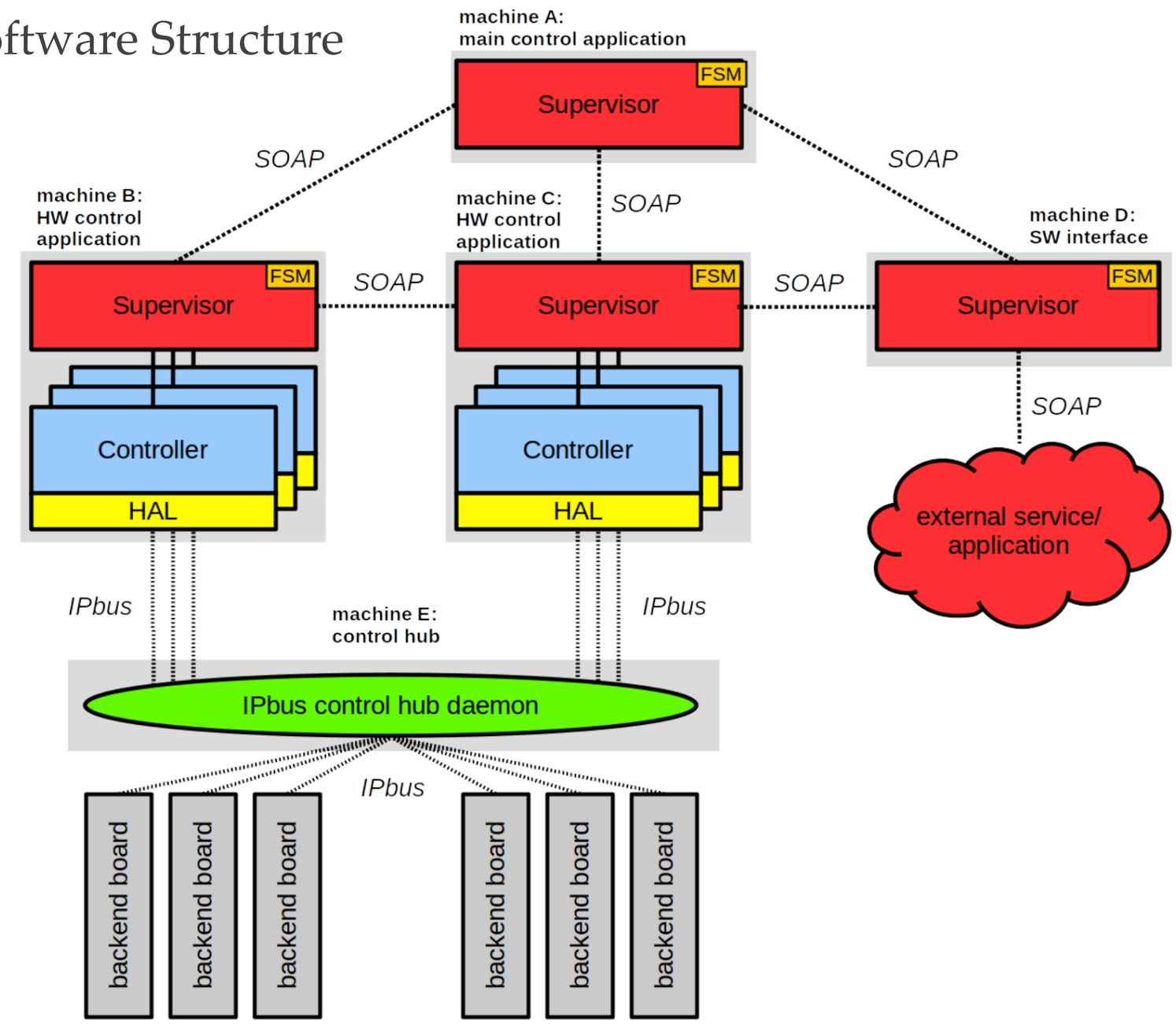


Pixel DAQ Backend layout



Pixel Online Software

Software Structure



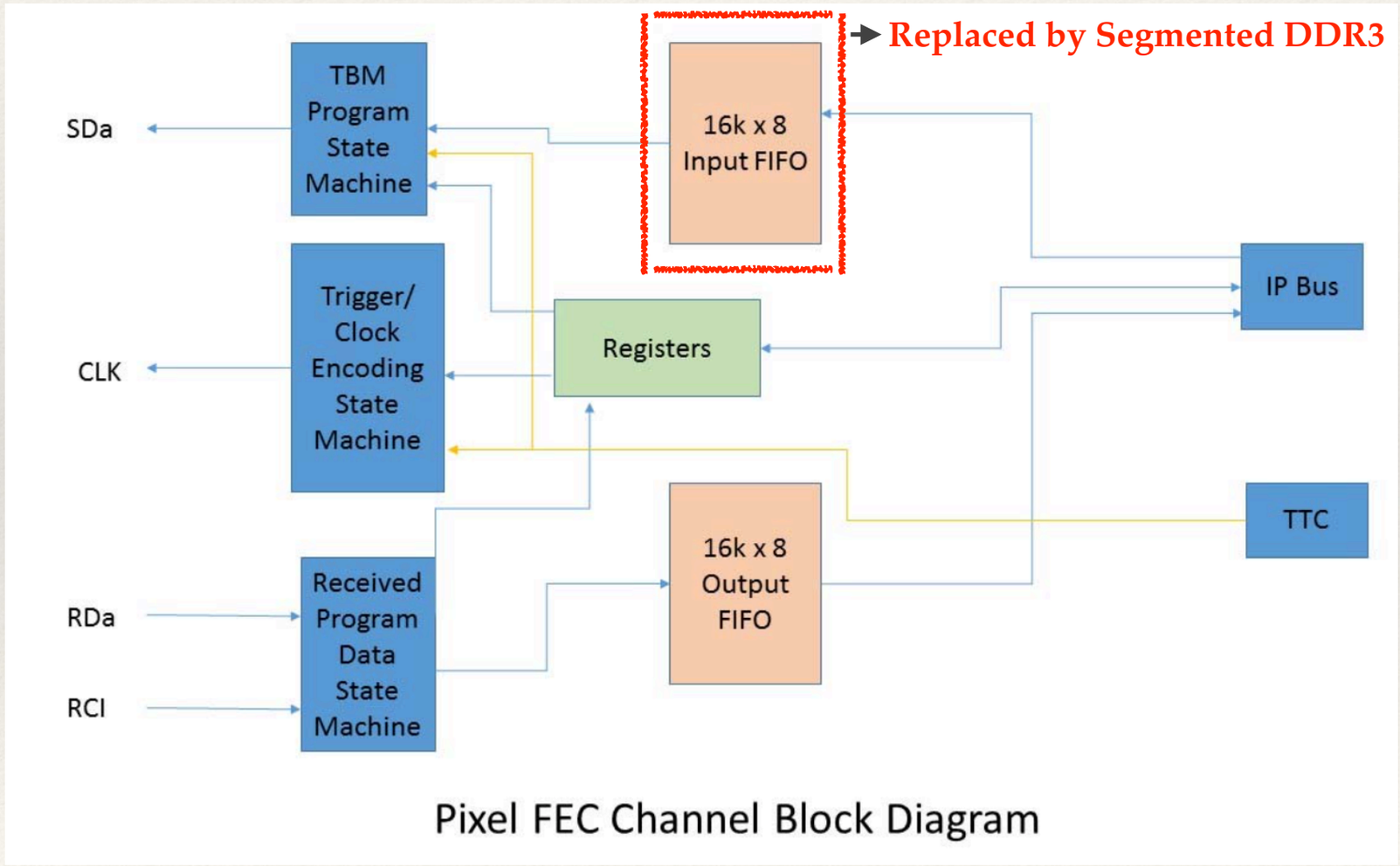
Firmware

There were two major developments on firmwares in 2018

- Pixel FEC firmware upgrade
- Pixel FED firmware upgrade for Heavy Ion physics

Pixel Front-end Controller

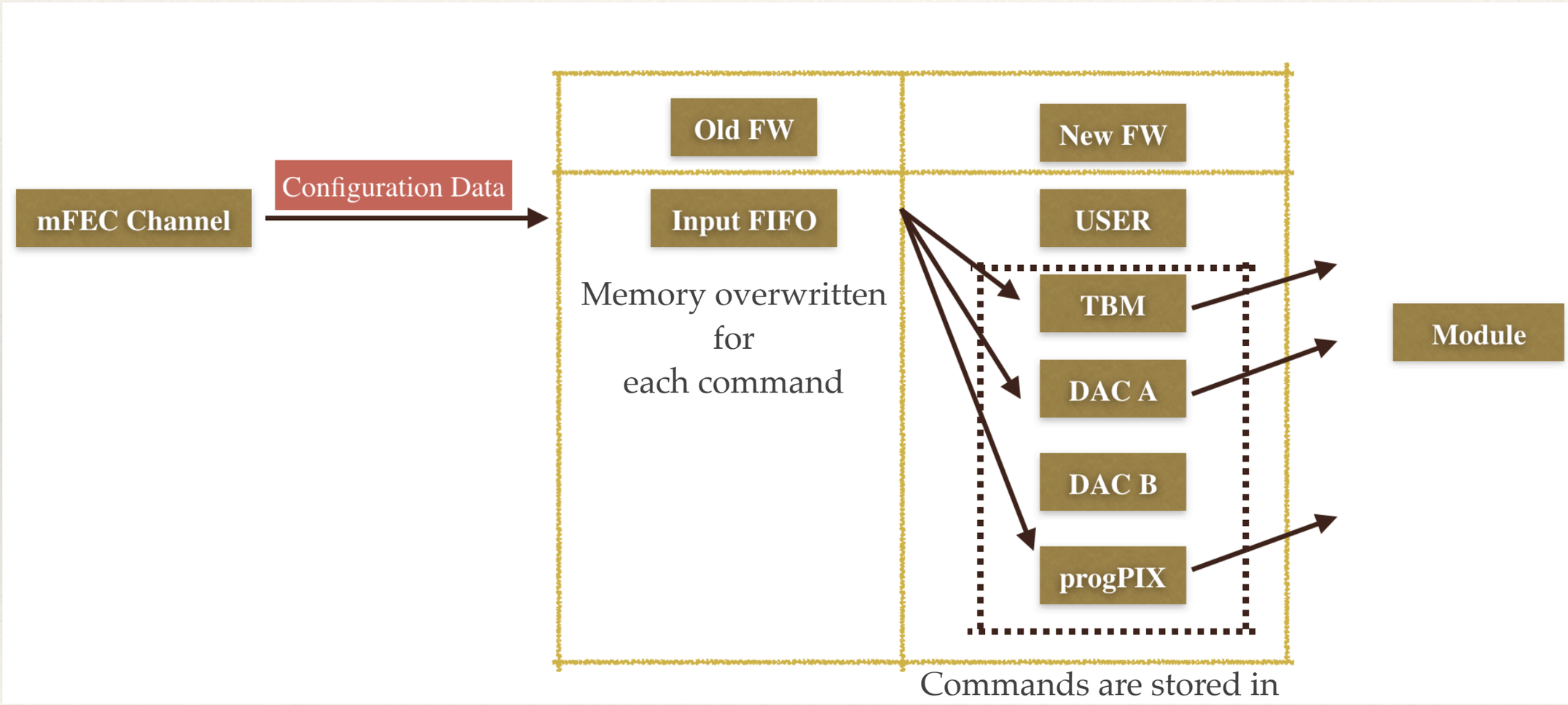
- Segmented DDR3 memory structure
- Store module configuration data in DDR3 memory locally



Pixel FEC Channel Block Diagram

Segmented Memory

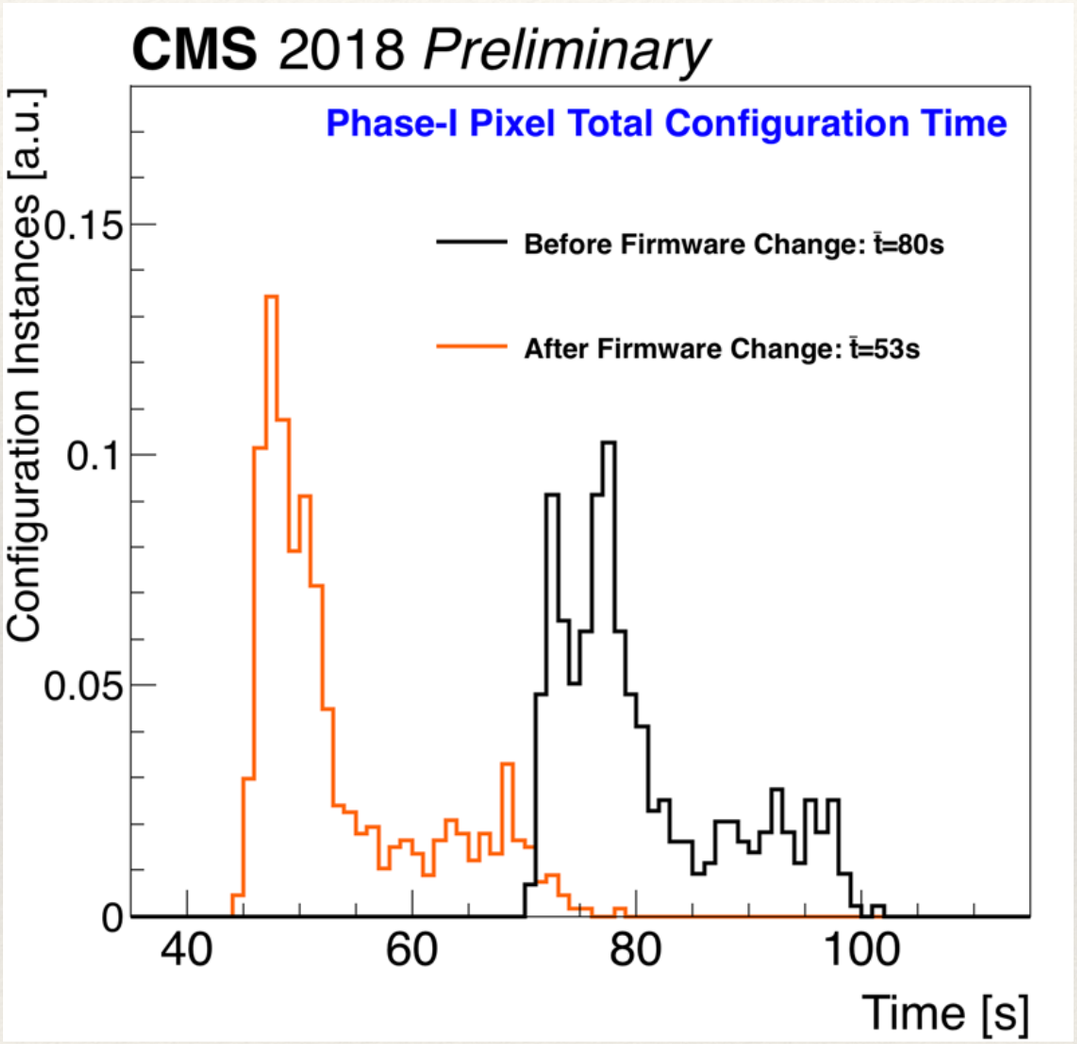
- Write different type of commands in designated memory
- Send out in parallel per channel



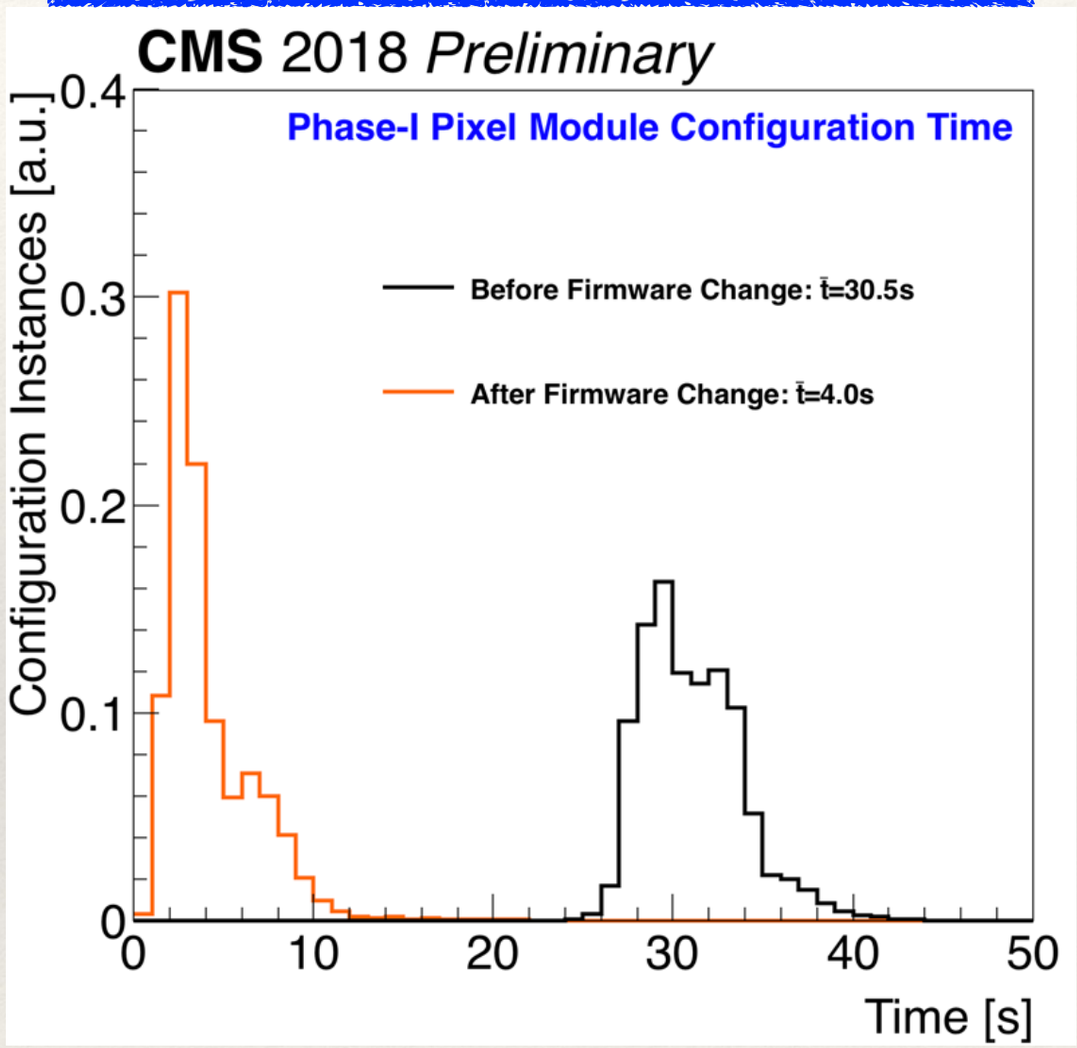
Commands are stored in Segmented memory

Pixel FEC Performance

1856 Module x 16 ROC x 4160 Pixel



Total configuration time reduced dramatically due to PixelFEC firmware upgrade

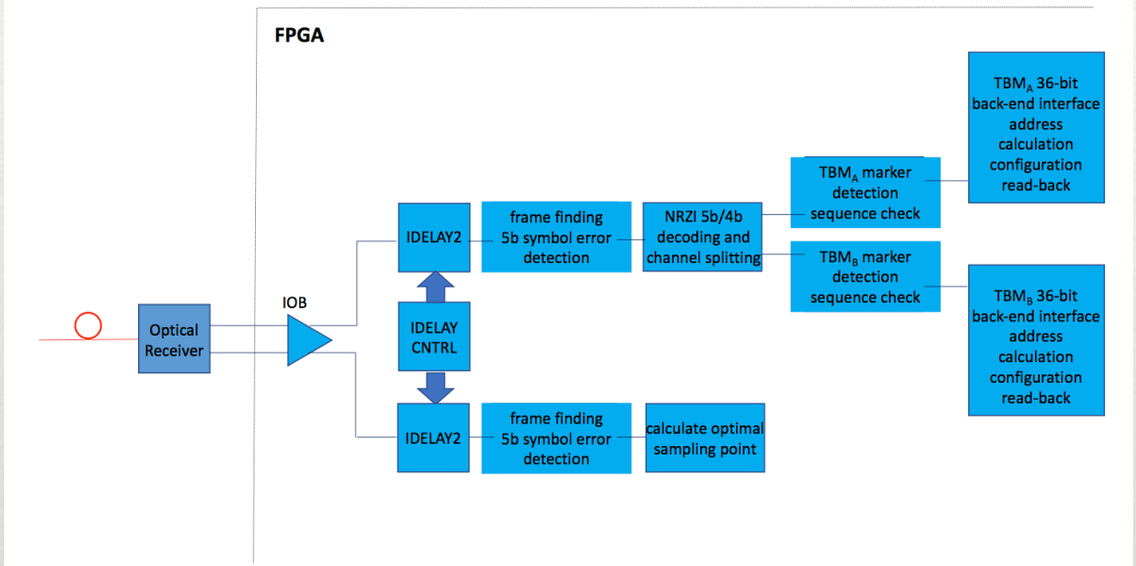


Faster Module configuration has direct impact on detector operation

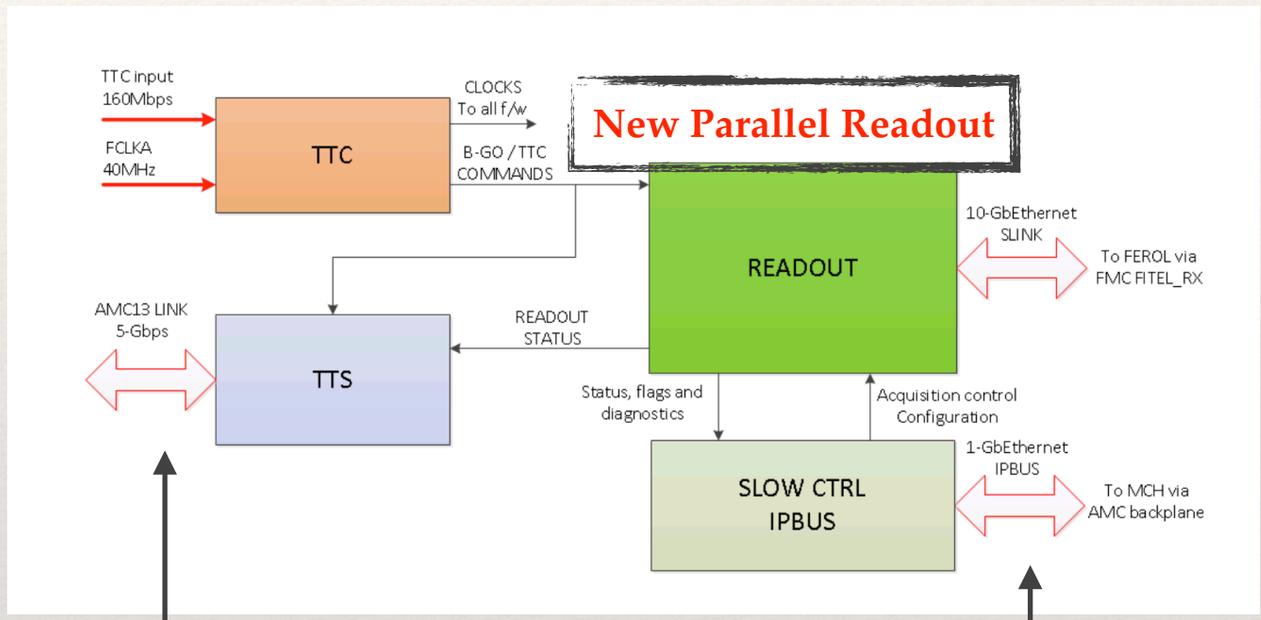
Front-end Driver Firmware

- There are two parts of the FED firmware, front-end and back-end

Scheme for FED frontend firmware

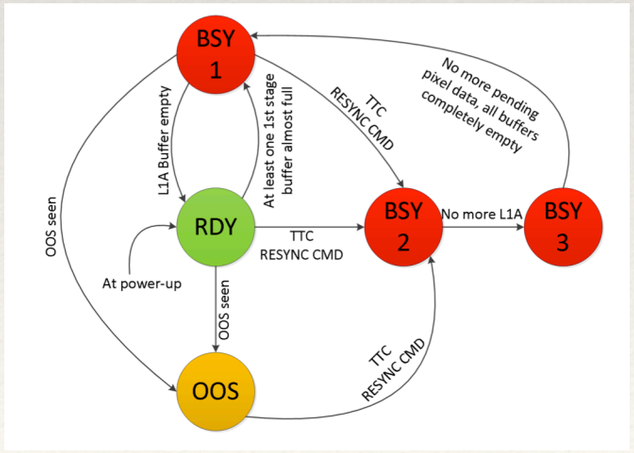


Scheme for FED backend firmware



Spy data to monitor error

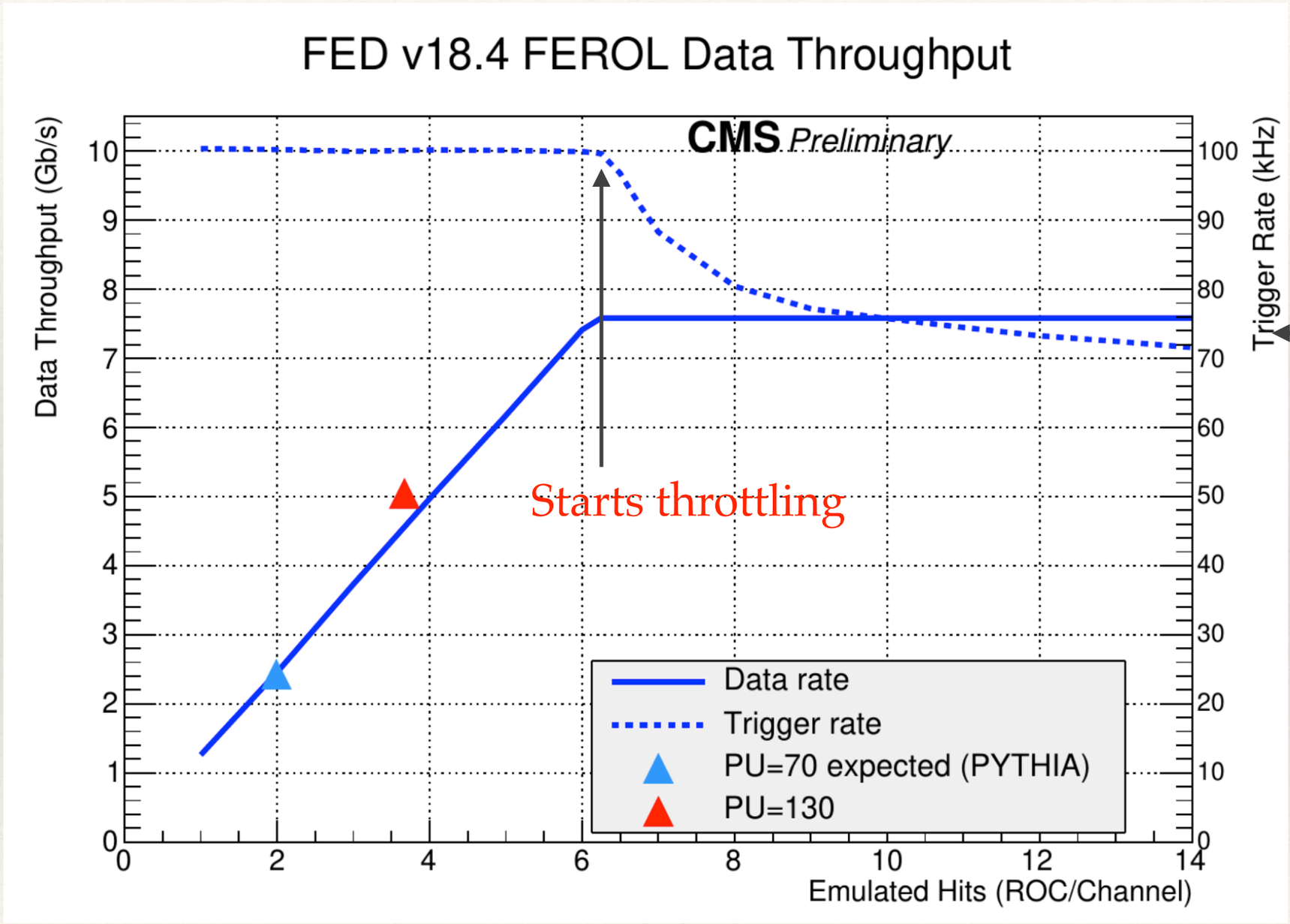
FED only receives trigger when in RDY state



FED can have 3 possible states:

- Ready (RDY)
- Busy (BSY)
- Out of Sync (OOS)

FEROL Throughput



New firmware saturates the link

FED throughput from Slink to FEROL. Solid line is the throughput, while the dotted line is the measured trigger rate. The blue (red) triangles are the throughput of simulations with a pile-up of 70 (130)

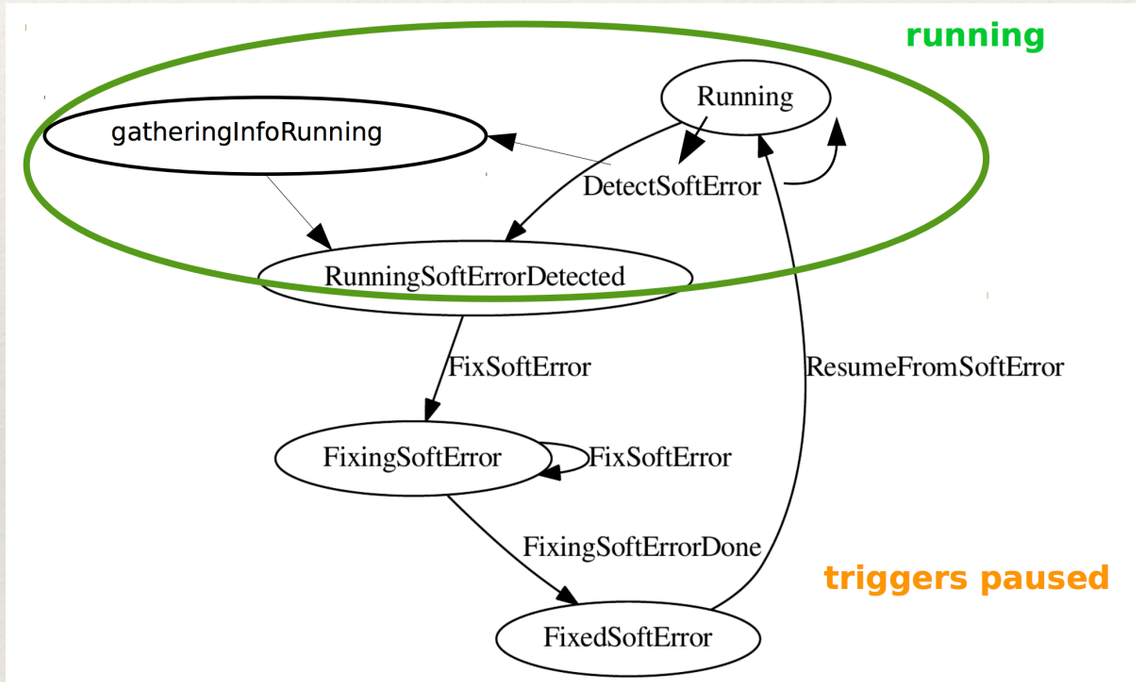
Soft Error Recovery (SER)

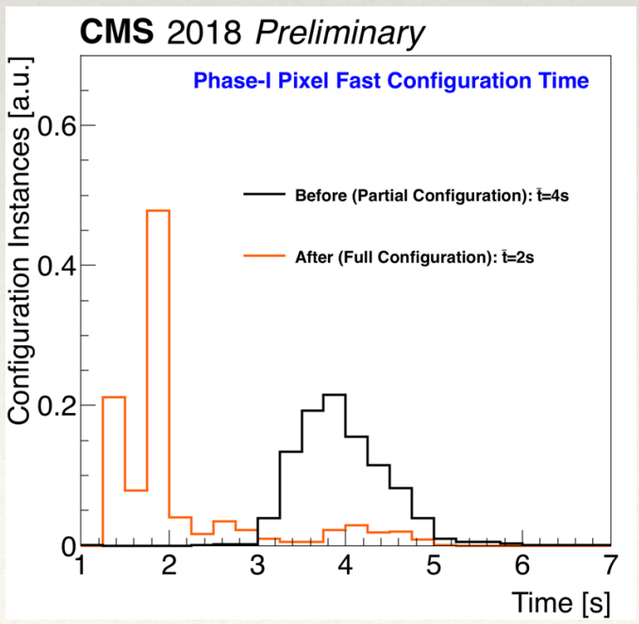
- Automatic recovery from Single Event Upset (SEU)
- Pixel is close to the interaction point, higher SEU rate

Recovery Scheme:

- Channel reported by FED as auto-masked
- with first FixingSoftError -> Reprogram Module
- Channel reported by FED as auto-masked
- with second FixingSoftError -> Reprogram Module
- Channel reported by FED as auto-masked
- with third FixingSoftError -> blacklist (no data)

Software Scheme:





Configurable threshold to trigger SER

More complete and quicker module configuration during soft error recovery

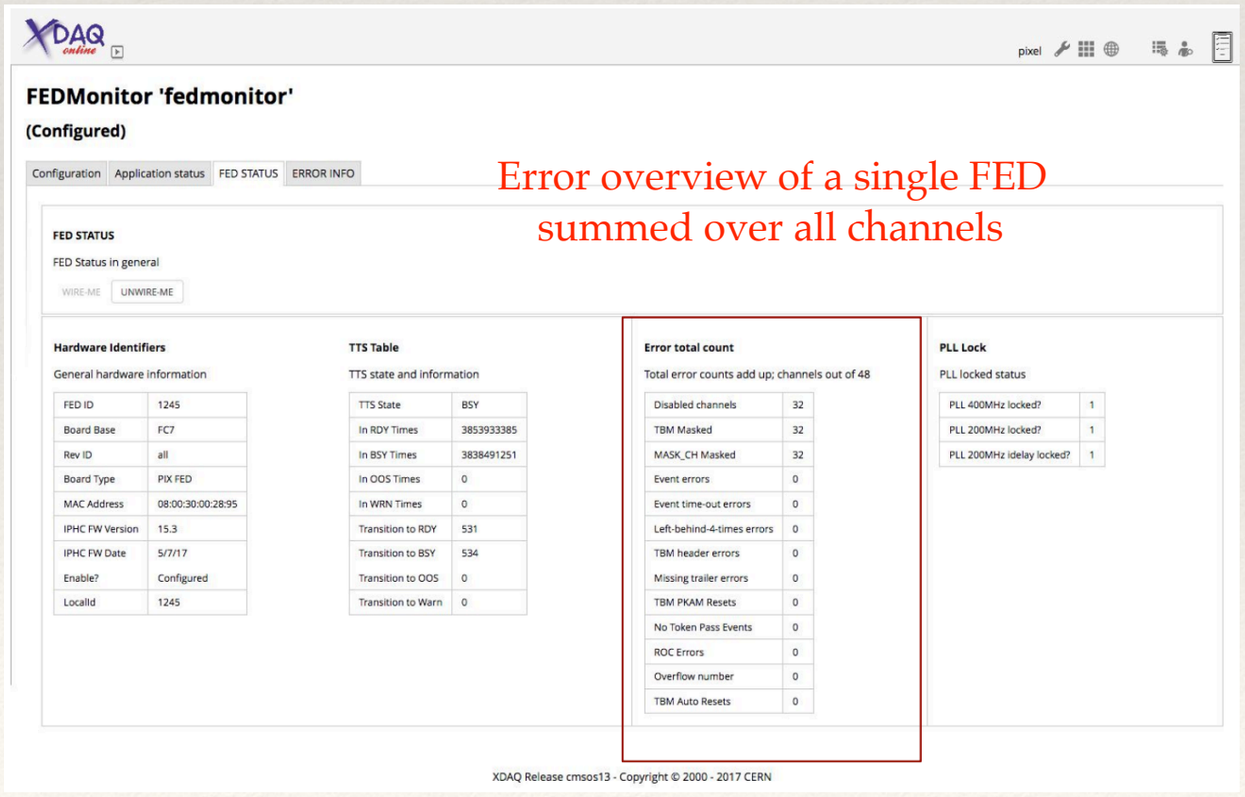
- **Full Configuration:** Pixel level programming, ~66kB data/module
- **Partial Configuration:** ROC level programming, ~0.5kB data/module

Monitoring (I)

- Monitoring is extremely important to spot problems

FED Monitor:

- FED Rack overview
- Individual FED overview
- Channel wise details fer FED
- Powerful tool to diagnose problems



Error overview of a single FED summed over all channels

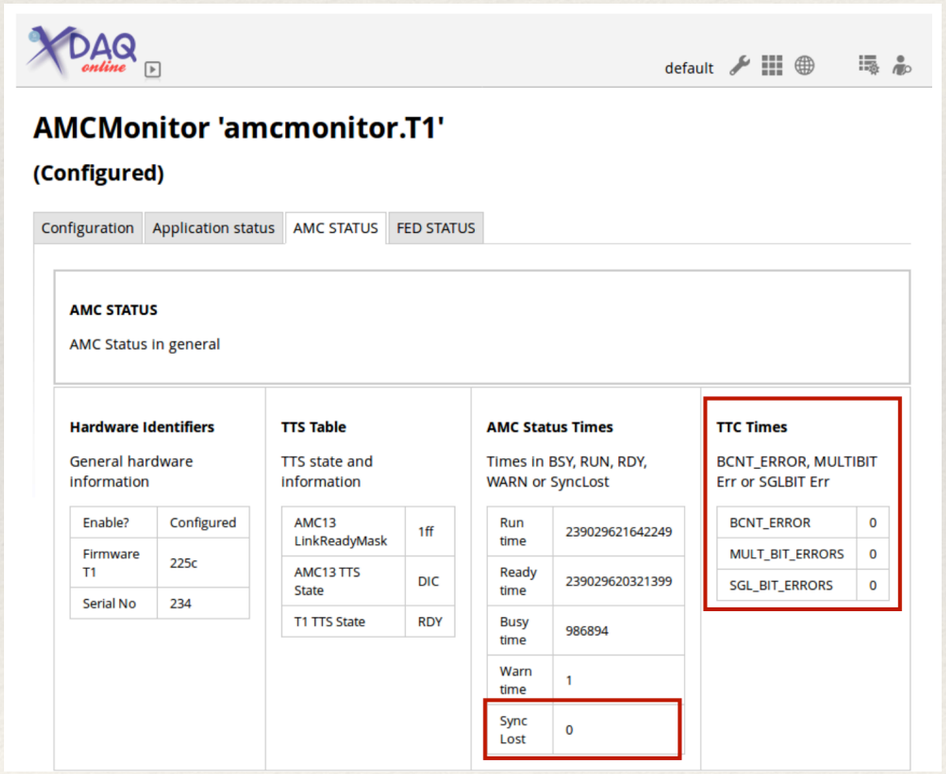
Detailed error summary for all channels in a FED

Name	NumOfGoodPhase	ME	MT	MC	EvtNumErr	EvtTOErr	MissTrailerErr	OverFlowNum	NoTokenPass	LB4T	ROC Error	TBM AutoReset	TBM Header Err	TBM PKAM Reset
CH01	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH02	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH03	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH04	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH05	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH06	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH07	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH08	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH09	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH10	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH11	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH12	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH13	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH14	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH15	21/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH16	21/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH17	21/32	0	0	0	2270	191043	4613	1275	26	0	3378	1369	0	1299
CH18	21/32	0	0	0	1210	191715	5130	1019	481	0	3074	1688	0	1353
CH19	21/32	0	0	0	277	26456	30940	424	54	0	3495	2500	0	2500
CH20	21/32	0	0	0	205	26591	0	390	54	0	3418	2474	0	2474
CH21	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH22	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH23	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH24	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH25	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH26	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH27	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH28	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH29	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH30	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH31	21/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH32	21/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH33	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH34	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH35	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH36	23/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH37	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH38	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH39	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH40	22/32	0	0	0	0	0	0	0	0	0	0	0	0	0
CH41	21/32	0	0	0	3352	286293	53732	4255	4	0	10740	4830	0	4707
CH42	21/32	0	0	0	2434	287510	2257	3698	1323	0	10256	5614	0	5236
CH43	23/32	0	0	0	42912	83061	30305	5872	178	0	6149	1328	0	1254
CH44	23/32	0	0	0	33148	83789	25694	3292	1089	0	8513	5599	0	5661
CH45	22/32	0	0	0	902	98528	60755	1413	1	0	7974	4046	0	4011
CH46	22/32	0	0	0	685	99012	3136	1385	840	0	7564	4337	0	3584
CH47	22/32	0	0	0	5824	21559	37678	2185	133	0	6159	791	0	634
CH48	22/32	0	0	0	4187	21560	31630	2198	94	0	5677	1051	0	964

Monitoring (II)

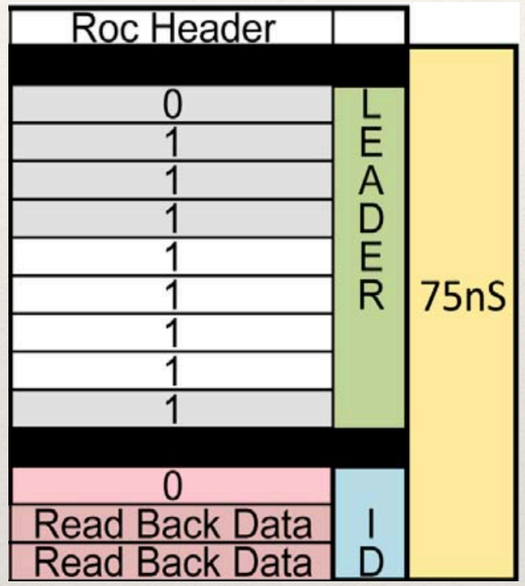
AMC13 Monitor:

- AMC13 status monitoring
- Status of individual slots in a crate
- Helps to figure out offending slot



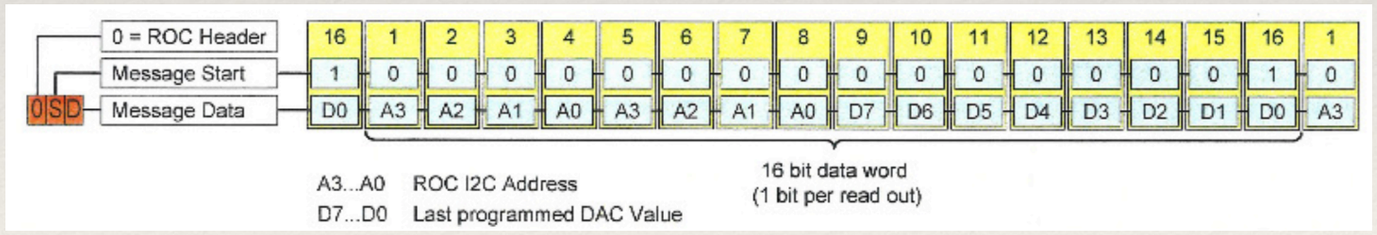
Online Readback of Read Out Chip:

- Live status of ROC properties



0SD Bits

Readback bits are part of the data format (ROC header)



Readback DAC settings: {Va, Vd, Vana, Vbg, Iana}

- There are various other tools which helped towards the smooth running of the detector in 2018

LS2 Plans

- During detector operation period not much scope for software restructuring
- LS2 provides the opportunity for long term development
- Goal is to make the software easier to maintain, develop and improve monitoring
- Massive cleanup of the software on the card
- Keep it XDAQ compatible
- Plan for new UI for different applications, added monitoring
- Configuration from database
- Firmware development for FED and FEC
- Use existing test setups for development purposes

Summary

- We had a productive year of operation in 2018
- No major issues
- Minimal data loss (5%) due to problem in Pixel DAQ, stable performance
- Developed new FED and FEC firmware
  - DDR FEC firmware improved the configuration timing drastically, enabled to write the full configuration to front-end frequently
  - Parallel draining improved the FED throughput significantly, also will be used after LS2
- Successfully dealt with the operation (daq) related issues as they appeared
- We will be using the same Pixel DAQ (backend) system in LHC Run 3
- Entering Long Shutdown 2 aiming for a major change in pixel online software