

Serial powering for the Phase 2 Upgrade of the CMS Pixel Detector

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Outline

- 1 Introduction serial vs parallel powering
- 2 Shunt-LDO regulator for the RD53A chip
- 3 Operation of a serially powered chain of RD53A chips
- 4 Readout efficiency in high hit rate environment

5 Summary







- After LS3 the instantaneous luminosity will increase to up to 7.5 times the nominal luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$.
- New sensors and new electronics are necessary to further collect high quality data.



The challenges of High Luminosity

High Luminosity Upgrade means:

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- Up to 200 proton-proton collisions.
- $\mathcal{O}(10^4)$ particles produced.

Detector requirements driving





power needs (complete overview in M.Backhaus' talk on Monday):

- High granularity to limit occupancy to $\mathcal{O}(1\%) \rightarrow$ many pixels.
- Compliance with 12.5 μs trigger latency \rightarrow lots of buffering.

 $\rightarrow\,$ smaller feature size technology (65 nm CMOS).

 $\rightarrow\,$ requires \sim 8 µA/pixel, $\sim\,$ 150 k pixels/chip $\Rightarrow\sim\,$ 1.5 - 2 A/chip.







- Designed by RD53 collaboration.
- Realized in 65 nm CMOS technology.
- Operates at 1 A and 1.4 V.
- Matrix of 192×400 pixels of $50 \times 50 \, \mu m^2.$
- Final chip will be about double in size.





Powering the pixel detector



A single chip works at V_0 , I_0 .

Parallel powering, power loss in cables: $P_{\text{cable}} = R_{\text{cable}} \cdot (n l_0)^2 \propto n^2$.





Powering the pixel detector



The CMS Pixel Detector will consist of 13488 chips \rightarrow serial powering.



Serial vs parallel powering

Advantages

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- · Huge improvement in power efficiency compared to parallel powering.
- Constant current consumption: avoids possibly lethal voltage transients.
- Only technically possible option to deliver power to the detector with an acceptable cable mass.

Disadvantages

- Increased fragility: failure of one element could compromise the entire chain.
- Increased complexity: an on-chip regulator is required to convert the input current into a constant input voltage.



Serial powering in CMS



- In CMS the cables will be \sim 100 m long.
- CMS plans to build serially powered chains of up to 11 *modules*.
- One module consists of two or four chips connected in parallel.
- In case of one (possibly two) chips failing, the remaining chips can shunt the extra current and keep working.



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• Provides constant voltage to the load.

- Shunts excess current in transistor M4.
- Configurable effective resistance and offset.
- Two SLDOs are integrated in RD53A for the analog and digital power domains.





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Turn on of the SLDOs

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Current ramp up

Current ramp down



- The SLDOs need a minimal current to start regulating (left plot).
- Once the SLDOs started up the input current can be decreased below the start up value and the regulation keeps working (right plot).





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Serially powered chain of RD53A chips







Serially powered chain of RD53A chips



Four RD53A chips mounted on PCBs







- · All four chips have a resistive behaviour.
- The total input voltage of the chain is the sum of the input voltages of the individual chips.



Chip operation - readout of calibration signals

RD53A preliminary

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Chip S/N: 0x0566







Chip operation - noise



- Distribution of pixel-by-pixel noise difference between single chip and chain, for all four chips.
- Operation in chain has no influence on the noise.





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Performance under high hit rate – X-ray setup at ETH





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Performance under high hit rate – X-ray setup at ETH







Analog hit processing



- The signal from the sensor (bump pad) is amplified and compared to a threshold voltage.
- Signal is digitized counting the Time over Threshold (ToT).



Analog hit processing - sources of inefficiencies



- Two hits within few clock cycles are registered as one big hit with large Time over Threshold.
- · Hit losses due to this effect scale linearly with hit rate.



Sources of inefficiencies - buffer architecture



- The pixel matrix is divided into *regions* of four pixels with shared timestamp buffer, optimized for clustered hits.
- Buffer overflow causes data loss in the pixel region.





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- 1. Tune the chip to achieve a uniform threshold.
- 2. Place chip in X-ray beam.
- 3. Inject test signals in a few selected pixels and read out the full matrix (only linear FE for now).
 - Low trigger frequency (100 kHz) to avoid readout limitations.
 - Read out only the bunch crossing in which the signal was injected.

Results:

- Efficiency computed from number of signals recorded in selected pixel(s).
- X-ray hit rate computed from average occupancy of other pixels in the same pixel region (i.e. sharing the memory logic).



Efficiency vs trigger latency – shunt mode



- For $3.75\,\mu s$ latency only analog losses are visible.
- For 12.5 µs (nominal), 3 GHz/cm²: efficiency < 99%, BUT photons only cause single pixel clusters → worst case.



Efficiency measurement vs simulation



- Simulation of random single hits (emulating X-ray photons) with 12.5 µs latency (thanks to Sara Marconi).
- · Good agreement between measurement and simulation.



Efficiency vs trigger latency – powering modes



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Direct powering



· Powering mode has no influence on the efficiency.



Efficiency simulation – realistic clusters



- · Simulations of clustered hits are much closer to 99%.
- Further improvement possible by counting the ToT at 80 MHz (both clock edges).



Summary and outlook

- Serial powering is the power distribution system for the Phase 2 Upgrade of the CMS pixel detector.
 - Affordable cable mass and power efficiency.
 - Tests show no impact on performance compared to single chip (parallel) operation.
- RD53A prototype chip is available and being tested.
 - 65 nm CMOS technology.
 - Integrates two shunt-LDOs for voltage and current regulation.
 - High hit rate efficiency measurements agree with simulation.
- Future:
 - Development of next chip version has started.
 - Further aspects (HV distribution, current sharing between parallel chips, ...) under study, showing promising results.





Backup

Analog front ends: three flavours for testing



- Synchronous FE: uses a baseline "auto-zeroing" instead of per-pixel threshold trimming.
- *Linear FE:* linear pulse amplification and comparison to a threshold voltage ← *results focused on this one.*
- *Differential FE:* differential gain stage in front of discriminator. Threshold is implemented by unbalancing the two branches.



Synchronous front end design

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"Auto-zeroing" mechanism (no trim DAC): a baseline is acquired every 100 µs (during LHC abort gaps) and subtracted from signal.





Linear front end design







Differential front end design





SLDO X-ray irradiation to 6 MGy at CERN

- Performance of a 65 nm, 2 A SLDO prototype was tested for radiation hardness up to 6 MGy in April 2017.
- One chip irradiated at room temperature, one at -10° C.
- Only effect: very small changes in Vin and Vout





SLDO irradiation to 6 MGy at CERN: results





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SLDO irradiation to 6 MGy at CERN: results





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Requirements for the Phase 2 CMS tracker

as specified in the Technical Design Report

- Radiation hardness up to 10 MGy and 2.3 \times $10^{16}~n_{eq}/cm^2$ for an integrated luminosity of 3000 fb^{-1}.
- Occupancy < 1% for 200 collisions per bunch crossing.
- Efficiency > 99% up to 3 GHz/cm² hit rate.
- Long trigger latency (12.5 µs), in order to use tracking information in the Level 1 trigger.
- · Improved two-track separation.
- · Low material budget.
- Tracking acceptance up to $|\eta|$ = 4

