



Single Event Upsets in the ATLAS IBL Frontend ASICs

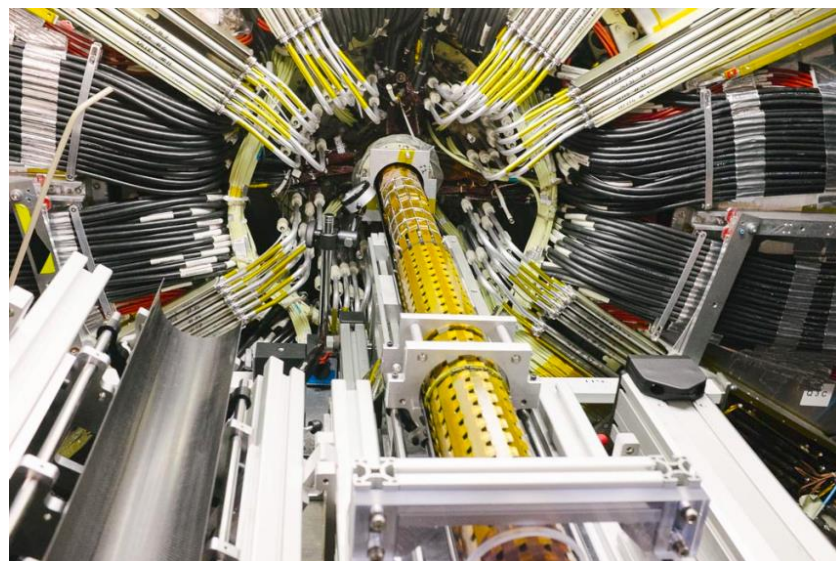
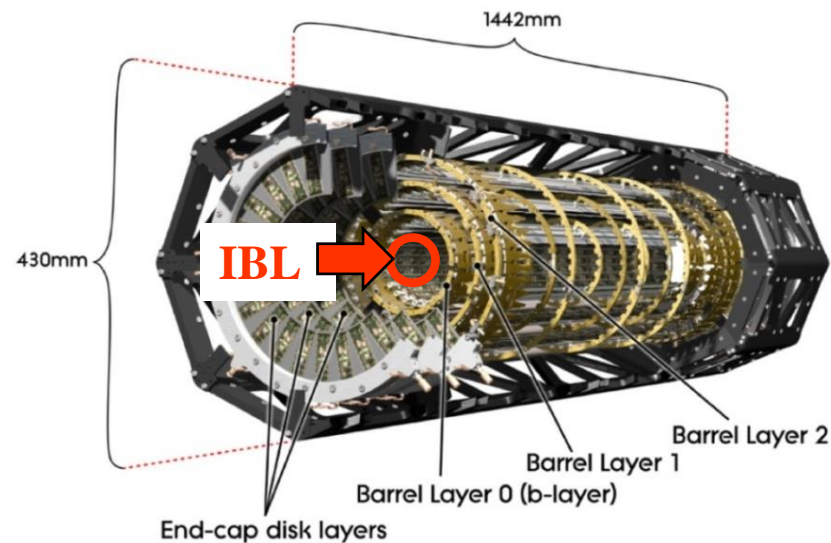
December 12th, 2018

Yosuke Takubo (KEK)

On behalf of the ATLAS Collaboration

Insertable B-Layer (IBL)

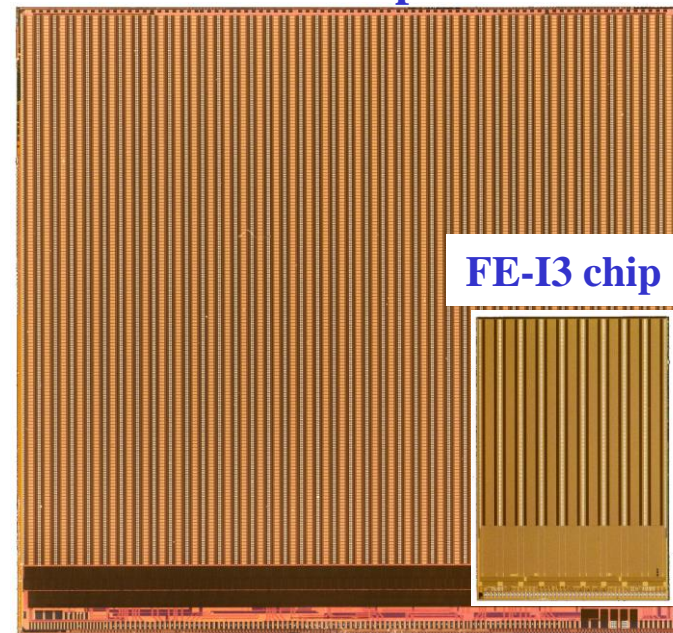
- The new innermost pixel layer ($r = 33$ mm) installed into ATLAS in 2014.
- Operational until the end of ATLAS Run-3 with peak luminosity above $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.
 - Up to $5 \times 10^{15} \text{ 1MeV n}_{\text{eq}}/\text{cm}^2$
- The n-in-n planar (75%) and 3D (25%) sensors are used.
 - The first time to use 3D sensors for HEP experiment.
- IBL improved performance of tracking and b-tagging.
 - $<40\%$ improvement for $\sigma_{\text{d}0/\text{z}0}$.



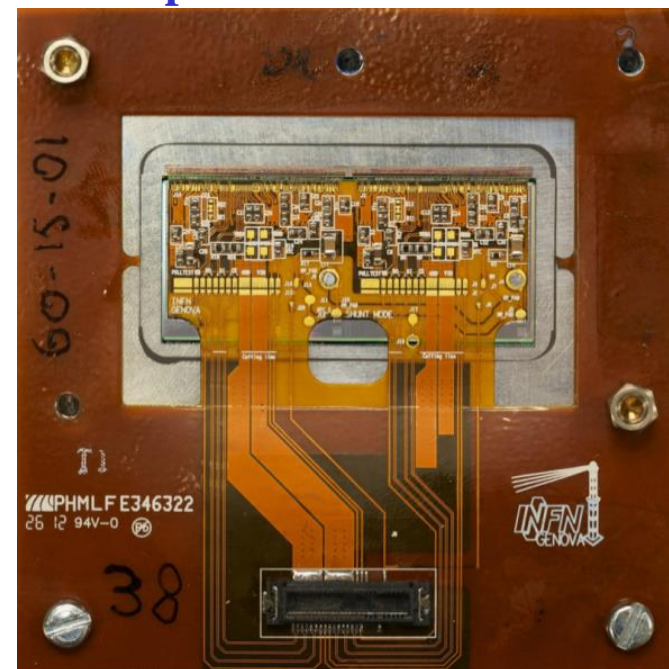
FE-I4 chip

- The front-end chip developed for IBL.
- 336 x 80 pixels (26880 pixels)
- Pixel size: 50 x 250 μm^2
- Chip size: 2 x 1.8 cm^2
 - ~4 times larger than FE-I3 used for Pixel detector existing since Run1.
- 130 nm CMOS technology
- 4-bit ToT (Time-Over-Threshold) for charge measurement
- Two (one) chips are used for a planar (3D) sensor module.

FE-I4 chip

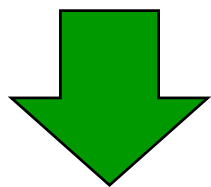


IBL planar sensor module



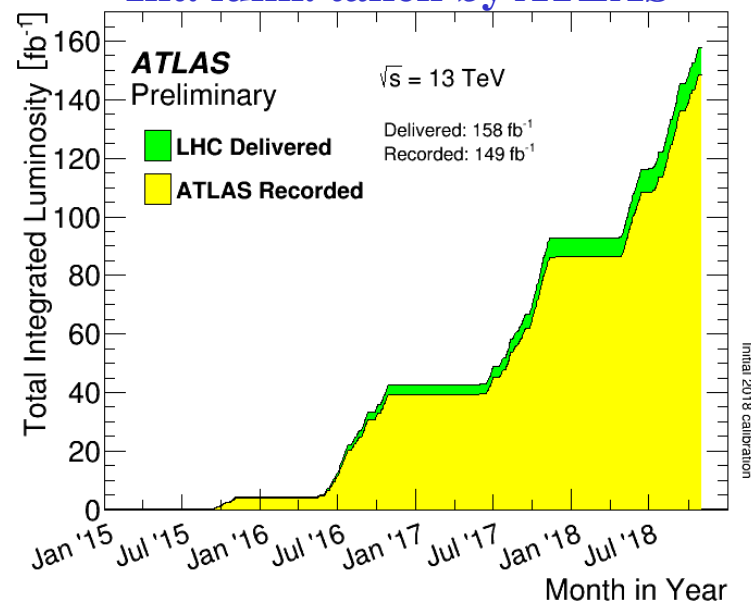
Data-taking at ATLAS Run-2

- ATLAS started to take data at 13 TeV colliding energy in 2015 (ATLAS Run-2).
- ATLAS took an integrated luminosity of 149 fb^{-1} in Run2 for pp collision.
- An instantaneous luminosity reached $2.2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ at the maximum in 2018.
 - The maximum # of pileup is ~ 60 .
 - More than 2 times larger than LHC design value!

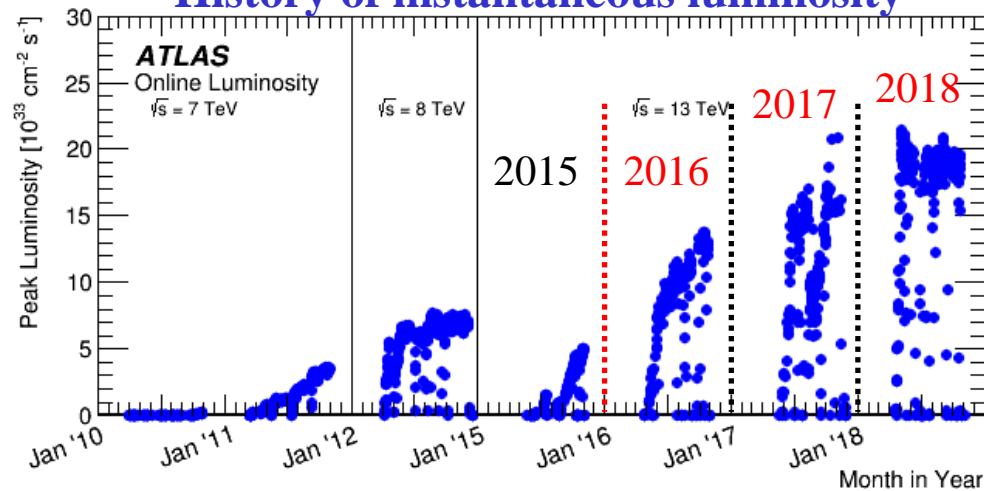


Effect of SEU/SET started to be visible in IBL since 2016.

Int. lumi. taken by ATLAS



History of instantaneous luminosity



FE-I4 Config. Memories

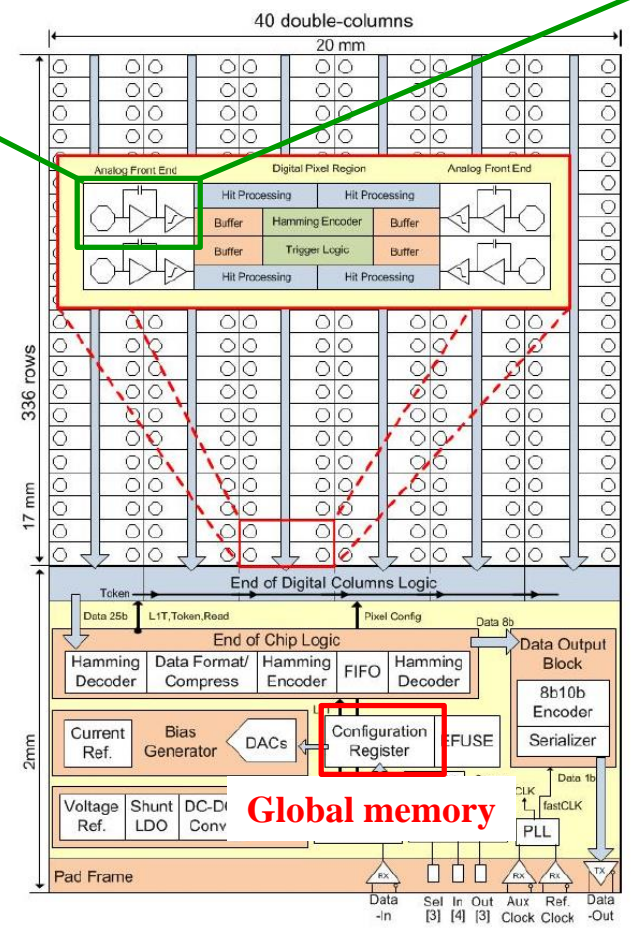
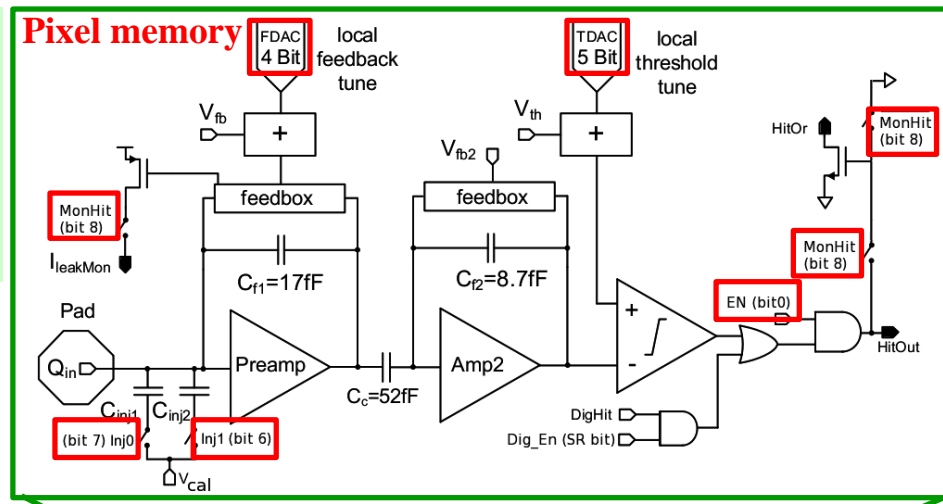
There are two types of configuration memory in FE-I4:

Global memory

- Configuration for front-end level for ToT and threshold.
- 32 registers of 16 bits

Pixel memory

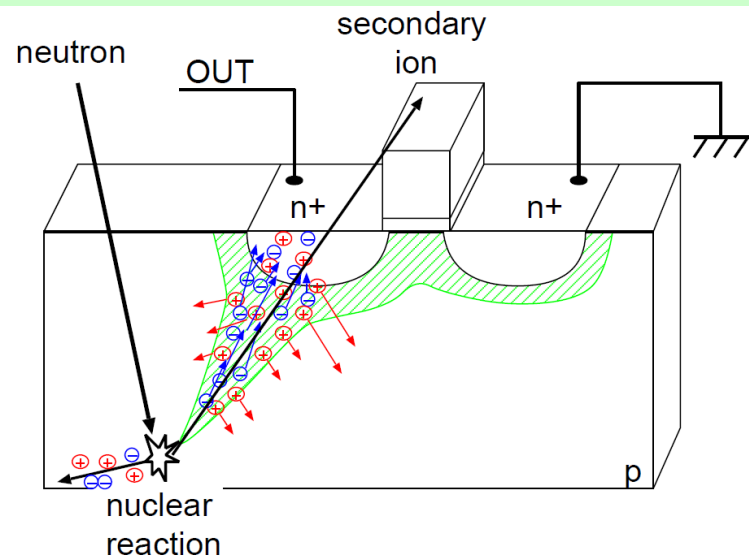
- Configuration for each individual pixel (336 x 80 pixels!).
- Fine tuning for ToT and threshold, pixel enable, etc..
- 13-bits memory per pixel.



Single Event Upset/Transient

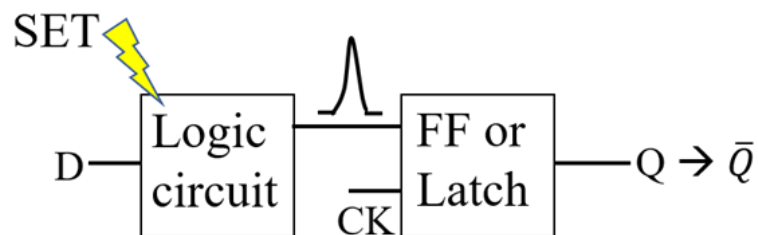
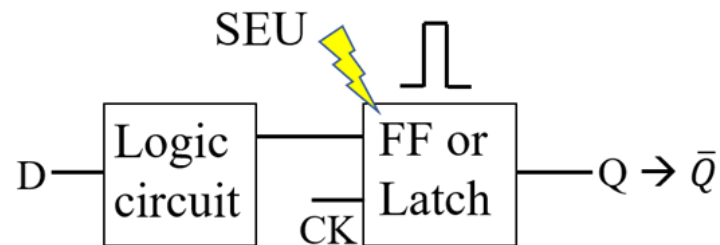
Single Event Upset (SEU)

- The charges caused by a charged/neutral particle alter the state of memory.
- On-chip memory corruption leads to detuning and reduction of hit efficiency.



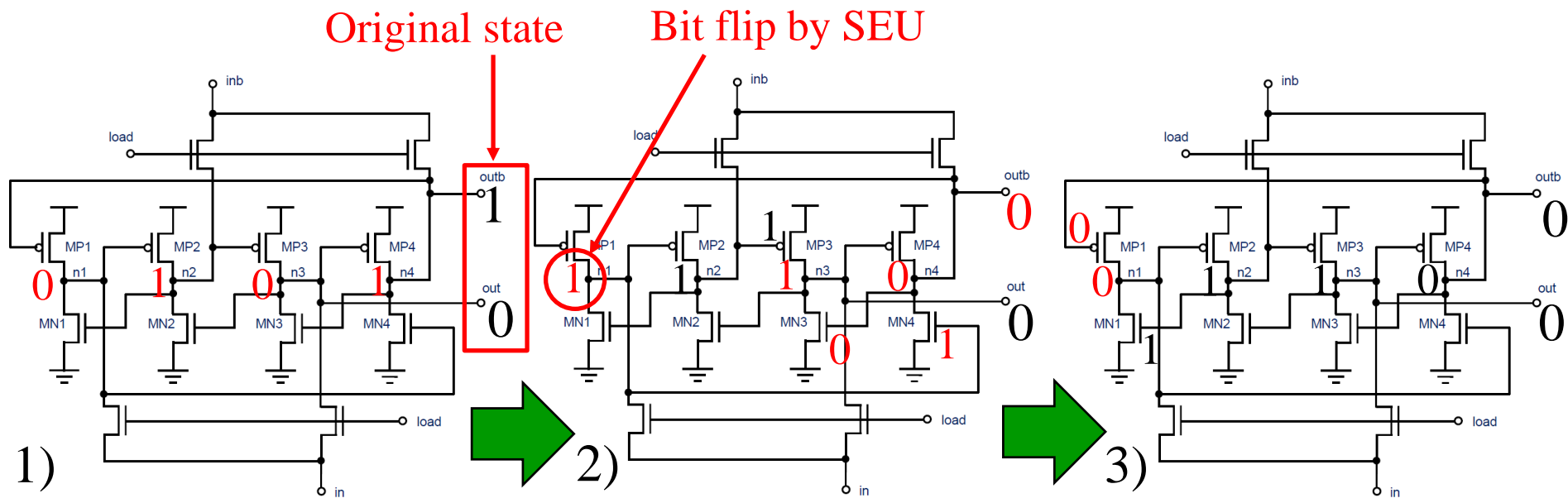
Single Event Transient (SET)

- A glitch caused by single event effect travels through combinational logic and is captured into storage element.

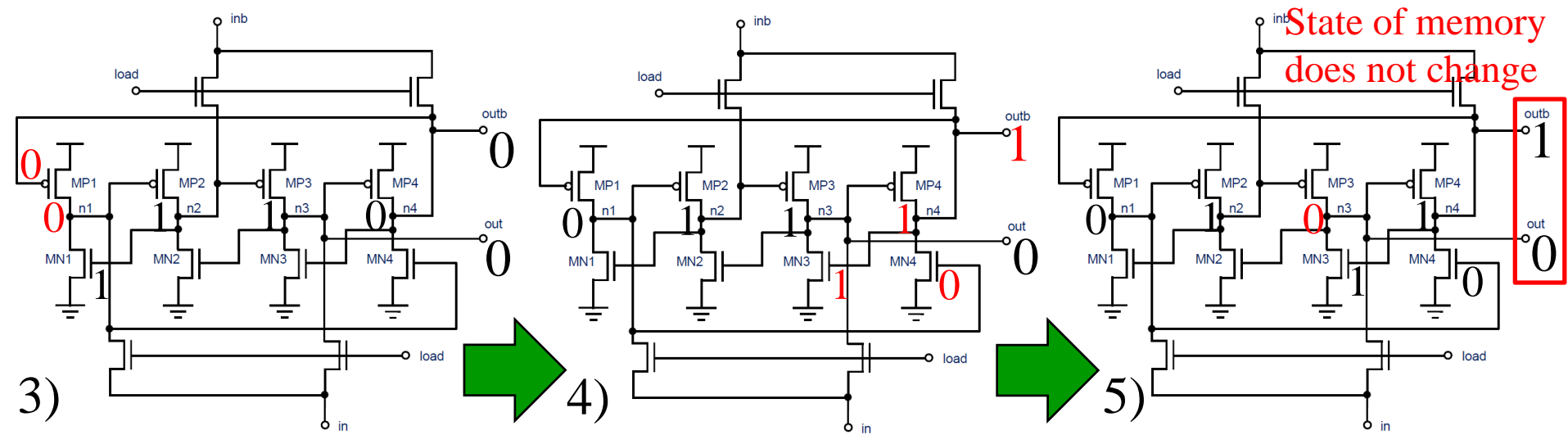


Dual Interlock Cell based memory (1)

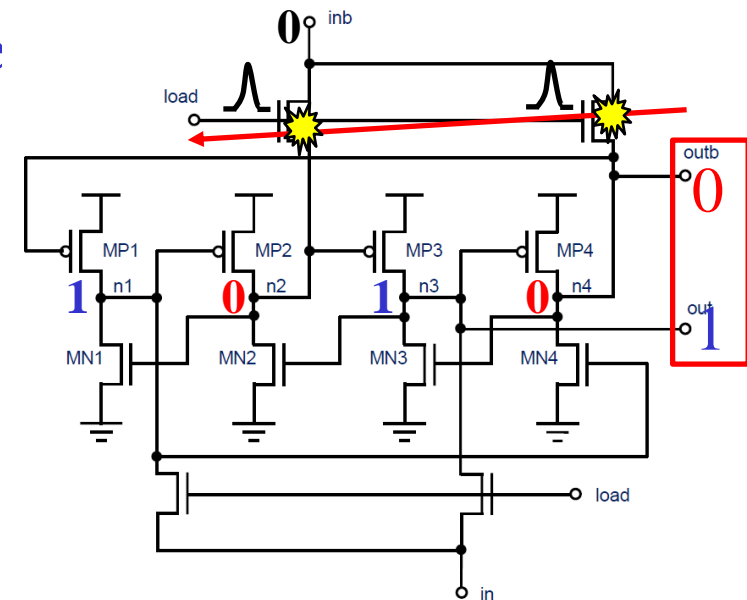
- Dual Interlock Cell (DICE) based memory is used for configuration memories in FE-I4 to protect from SEU.
- Cross coupled inverter latch structure with 4 nodes (n1-n4) stores data in two pairs of complementary values.
- Even if the state in one of 4 nodes is lost by SEU, state of the memory does not change by connection with the other nodes.



Dual Interlock Cell based memory (2)

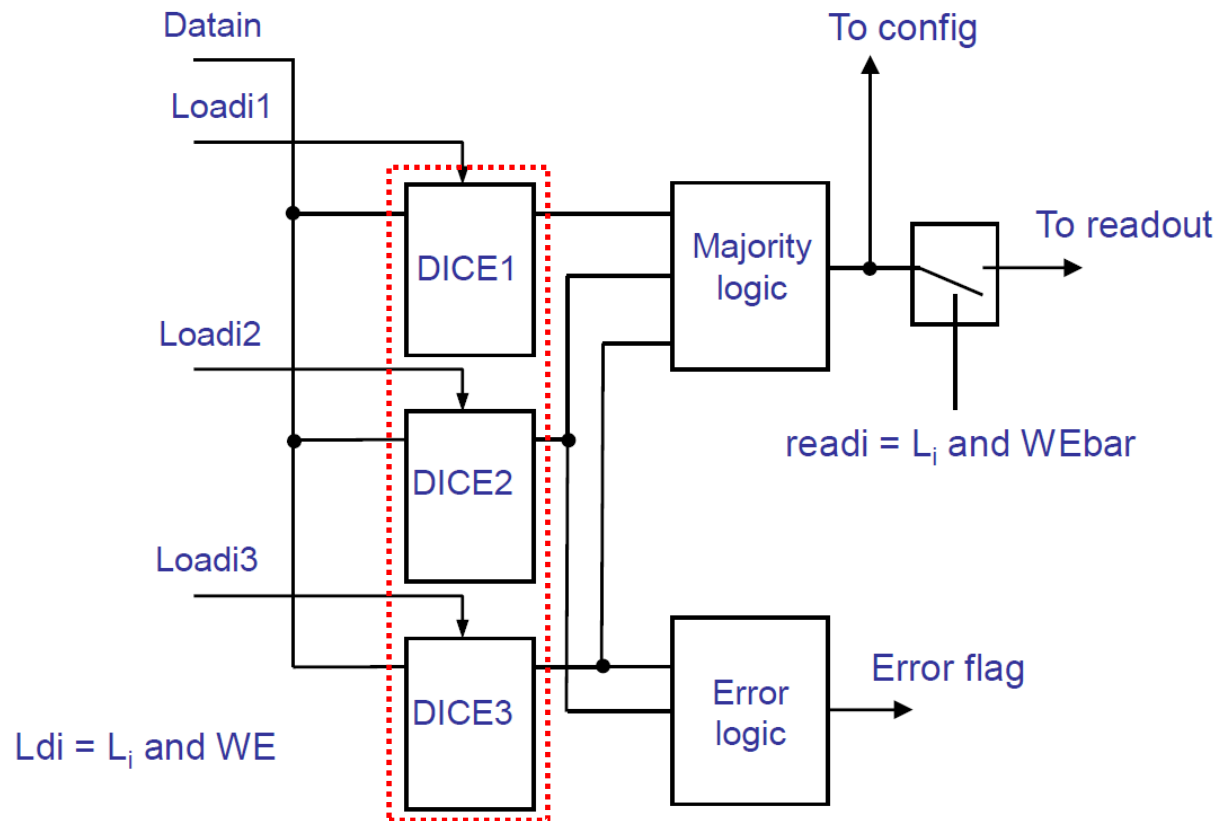


- SEU immunity is lost if two sensitive node change the state by SEU/SET.
- The tolerance of SEU is increased by Hardened By Design (HBD) approach.
 - Spatial separation of critical nodes, isolated wells, guard rings and interleaving of cells.



Triple redundant logic

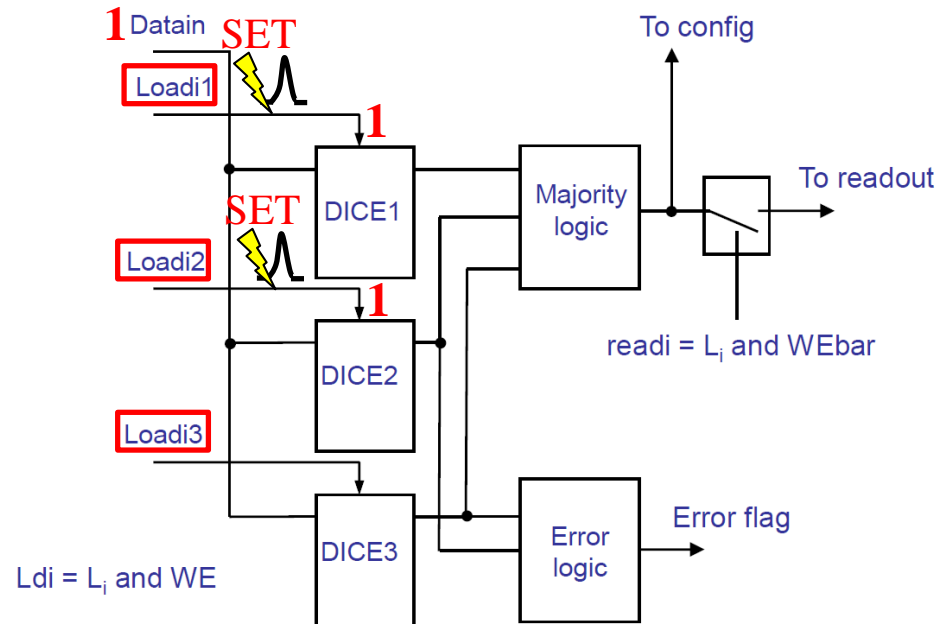
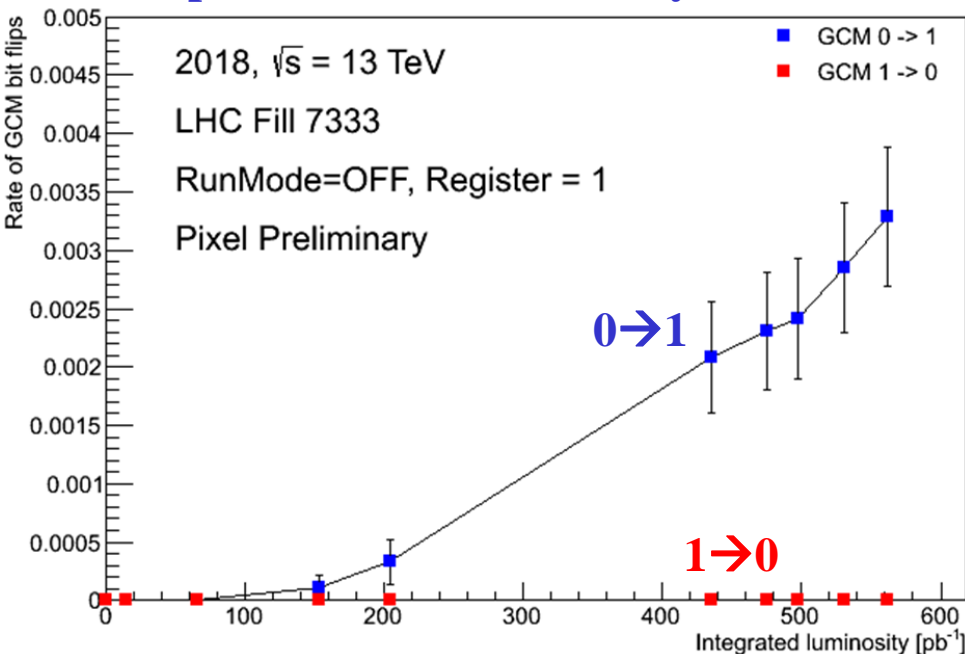
- Global memory is further protected by triple redundant logic with three DICE latches.
- The simple majority logic is used to keep the configuration.



SEU/SET rate in Global memory

- The cumulative rate of bit flips in Global memory was investigated to see effect of SEU/SET.
- High rate of $0 \rightarrow 1$ flips indicate SET (glitches) on the LOAD line with Data-in "1".
- No $1 \rightarrow 0$ transitions are observed due to the triple redundant logic.

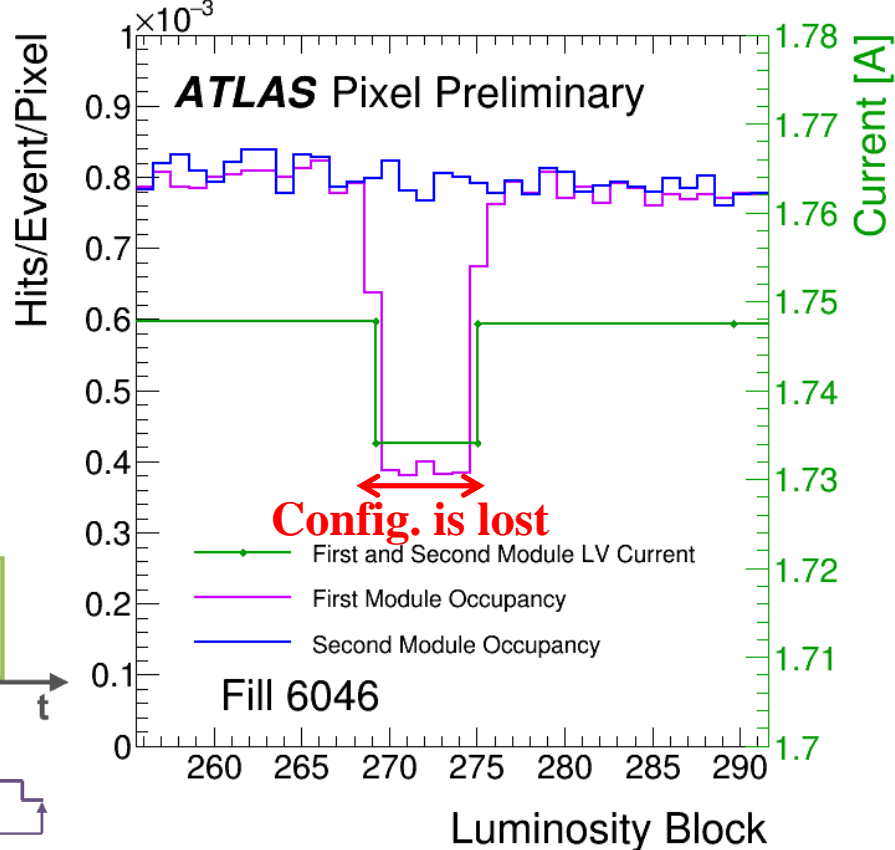
Bit flip rate in Global memory (Data IN = 1)



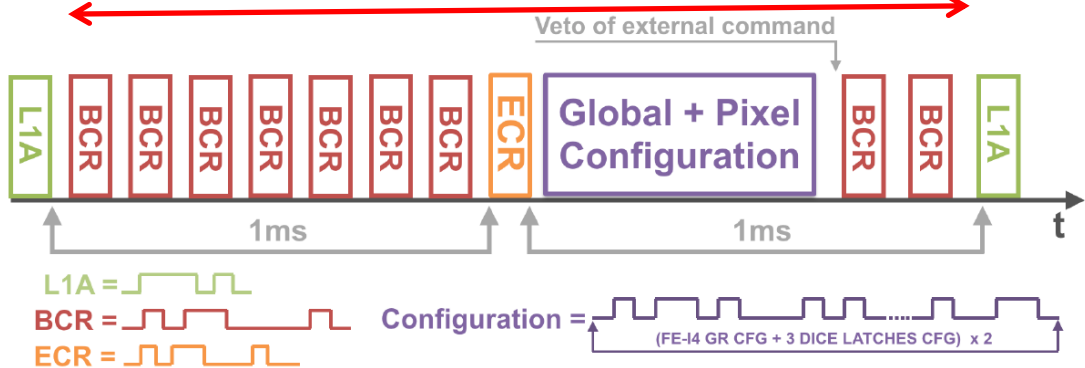
Recovery of Global memory

- Global memory corruption causes change of LV consumption, quiet modules, desynchronization, etc..
- Mechanism to refresh Global memory every 5s was deployed in 2017.
 - No extra dead time, reconfiguring at ECR (Event Counter Reset) timing of ATLAS sub-system readout.
- Proper function of the module could be restored by re-config..

Hit rate and LV current in IBL module



No trigger to IBL for 2 ms

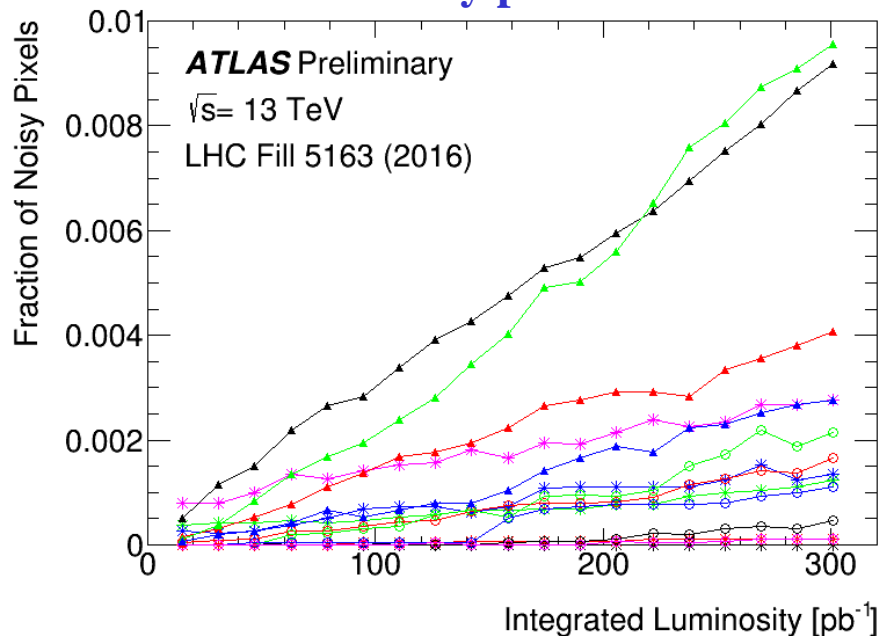


SEU/SET in Pixel memory (threshold)

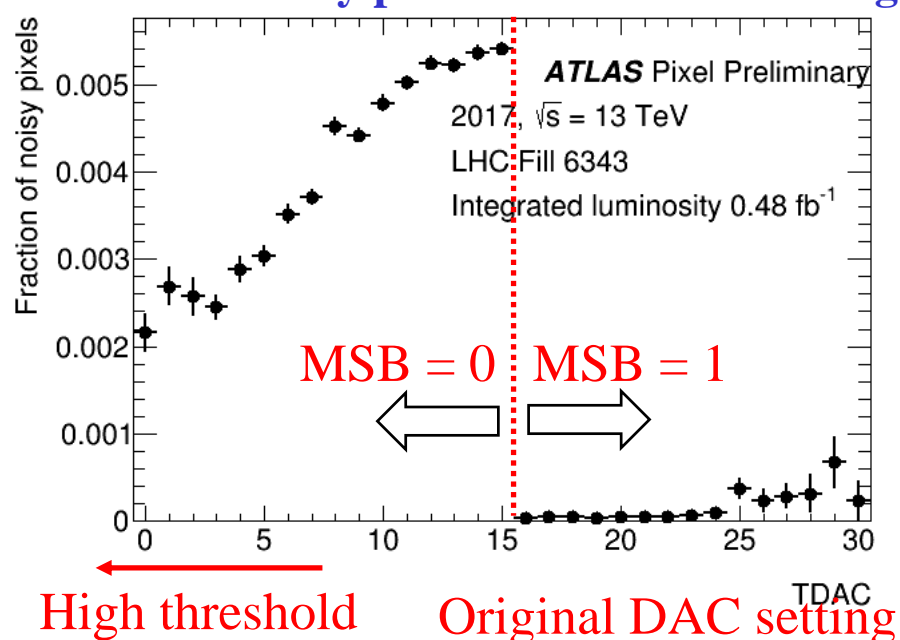
- Even with SEU tolerant logic, Pixel memory is affected by SEU/SET.
- The number of noisy pixels increases during a run.
- The noisy pixels concentrate in high original threshold setting.

→ The biggest effect comes from bit flip of MSB (Most Significant Bit) in threshold DAC (TDAC).

Fraction of noisy pixel v.s. Int. lumi.

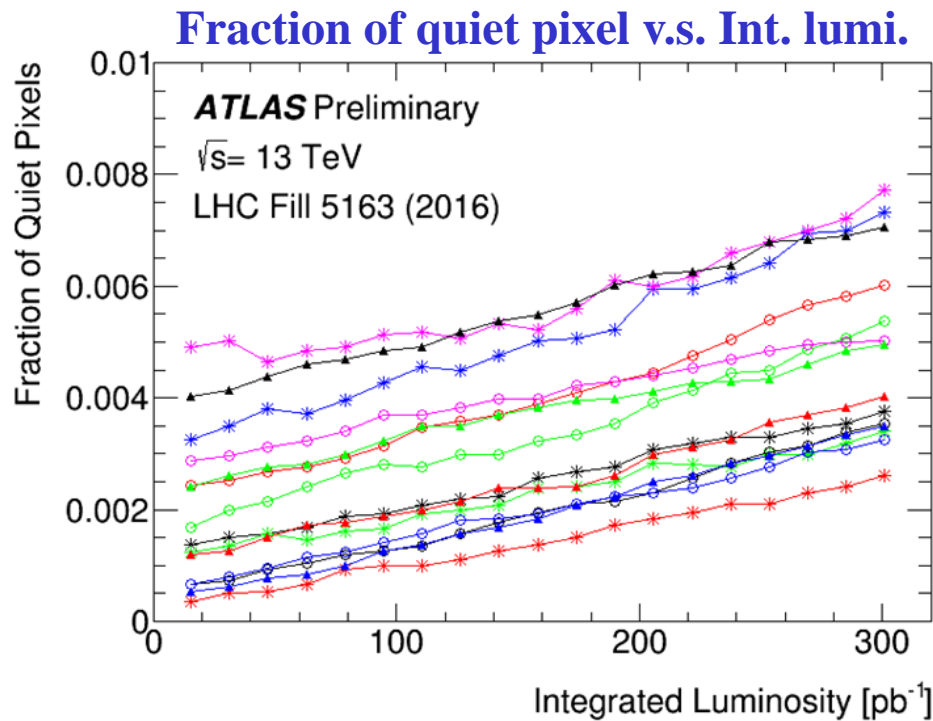
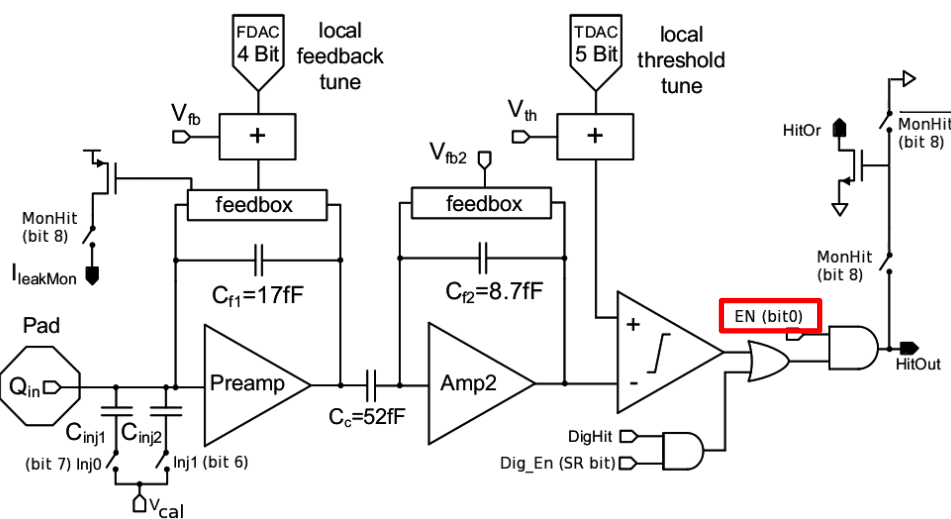


Fraction of noisy pixel v.s. Thr. DAC setting



SEU/SET in Pixel memory (Enable bit)

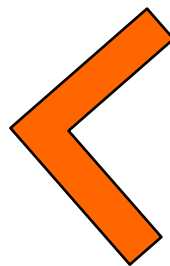
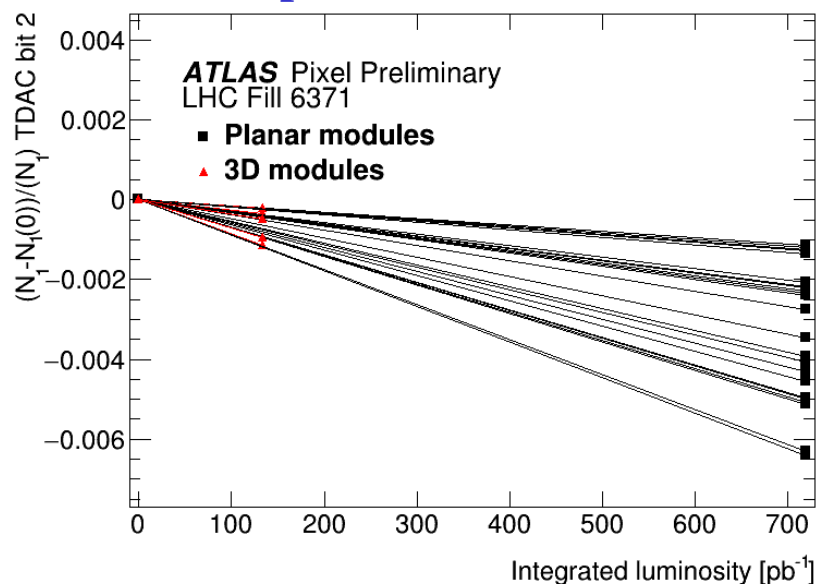
- The number of quiet pixels also increases during a run.
- The enable bit in Pixel memory would be disabled by SEU/SET.
- Offset is from disabled pixels.



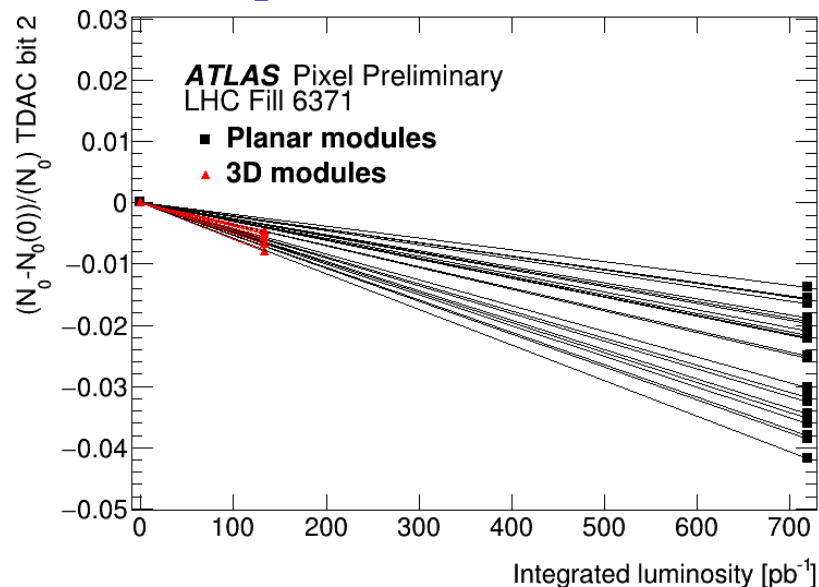
SEU/SET rate in Pixel memory (threshold)

- FE-I4 has a functionality to readback contents of Pixel memory.
- Bit flip rate was checked for one of bits in Pixel memory during a run.
- State of the bit was readback before start of collision ($N_{1/0}(0)$) and after beam dump ($N_{1/0}$), and the numbers of the bit state were compared.
- $0 \rightarrow 1$ is much larger than $1 \rightarrow 0$. \rightarrow Indicate SET! (see next page)

Bit flip rate ($0 \rightarrow 1$) v.s. Int. lumi.

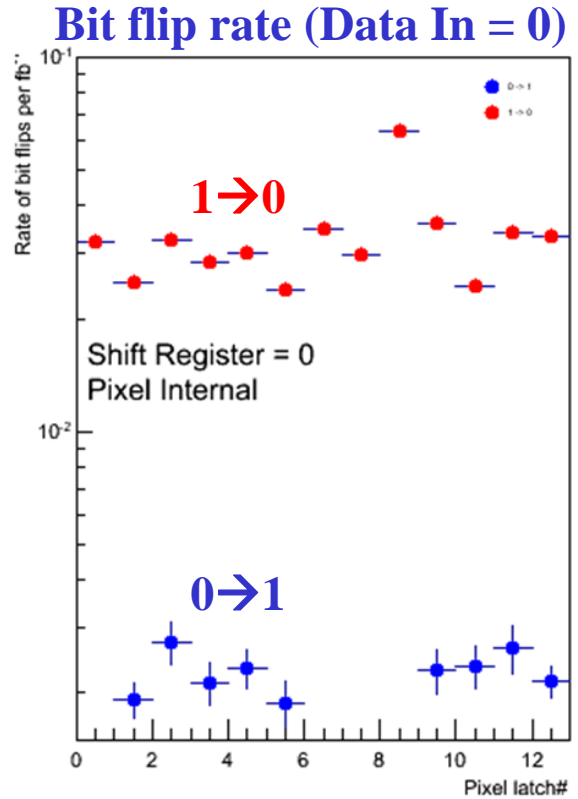
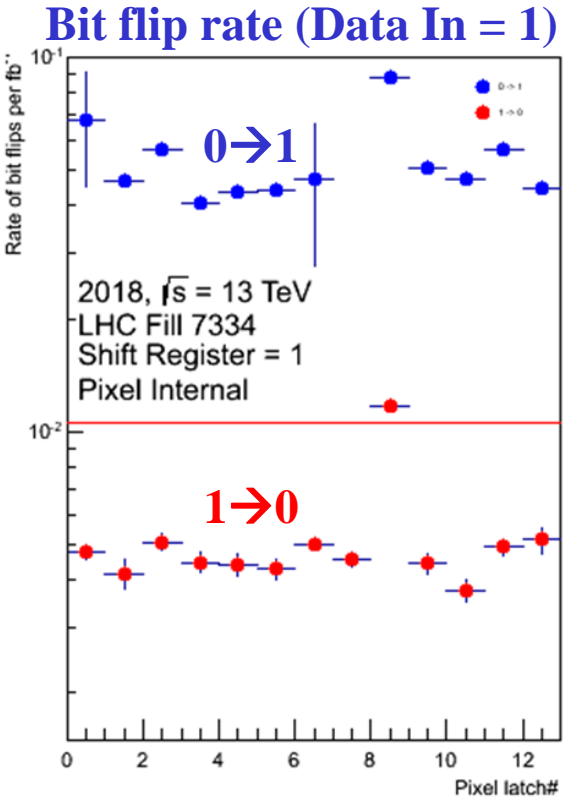
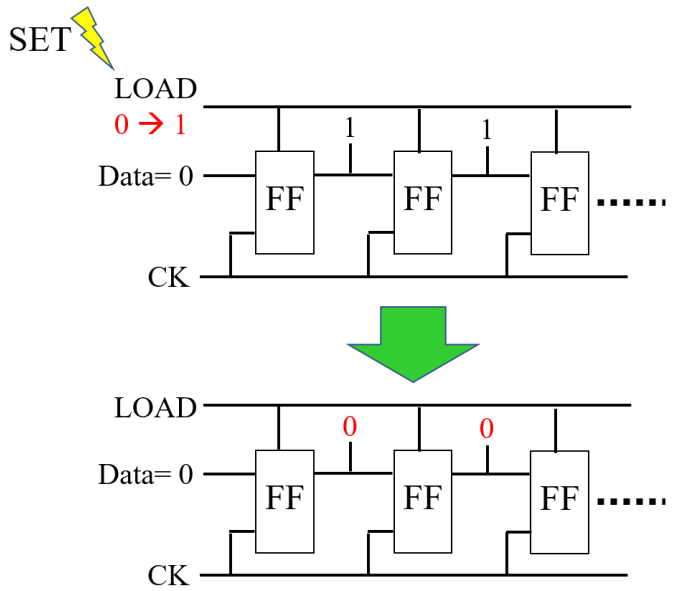


Bit flip rate ($1 \rightarrow 0$) v.s. Int. lumi.



Bit flip rate in Pixel memory

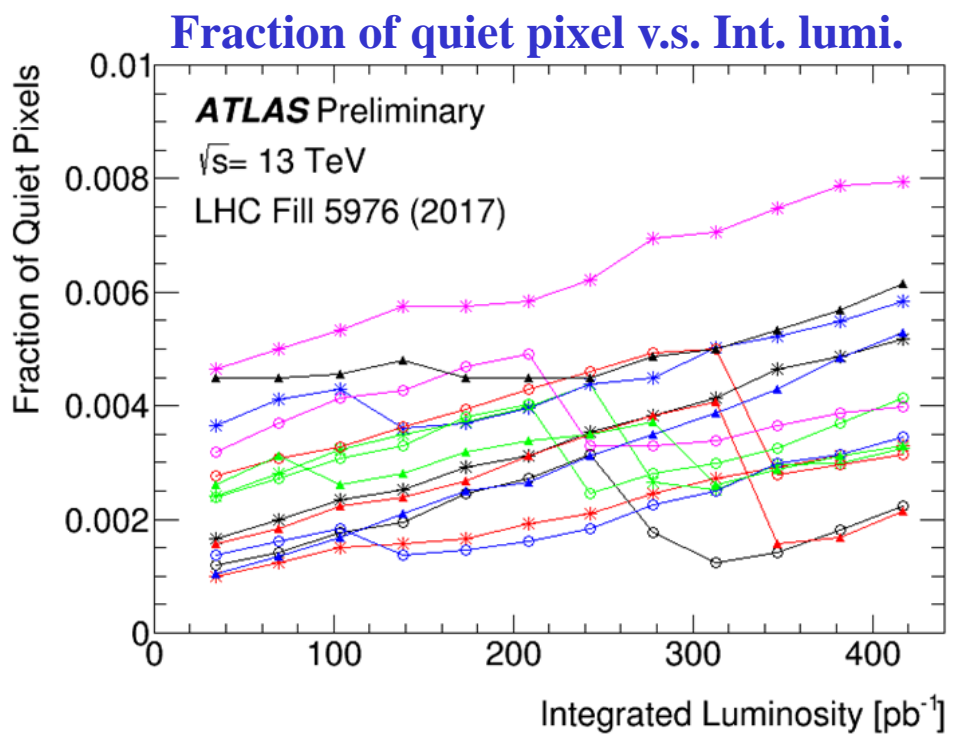
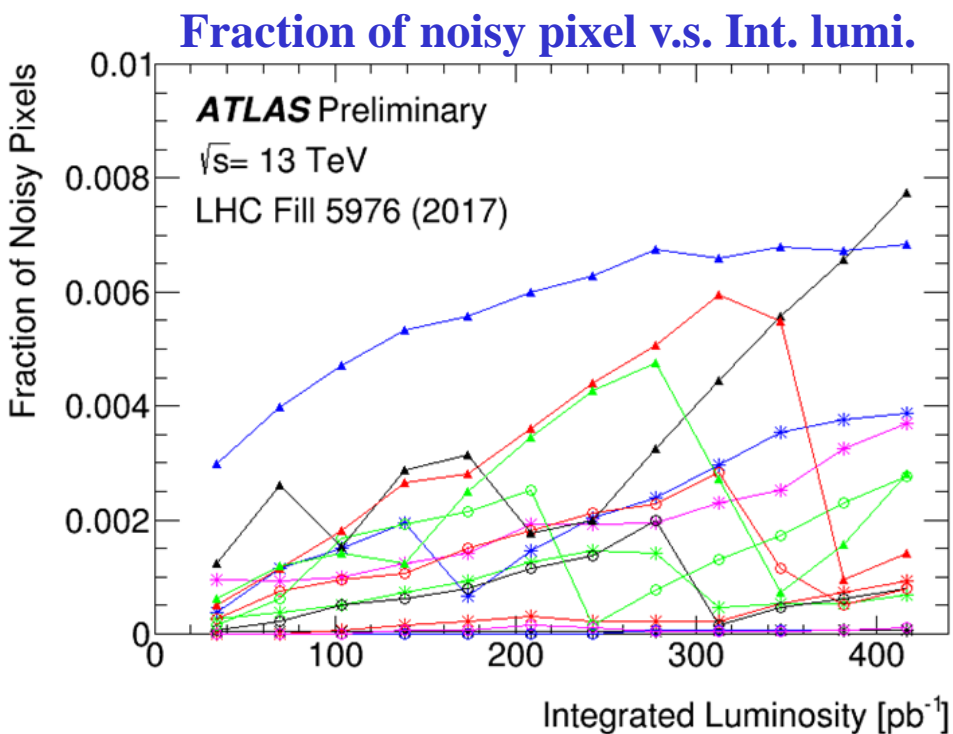
- Average rate of bit flips in Pixel memory was checked for each bit memory (13 bits in total).
 - $0 \rightarrow 1$ flips dominate for Shift Register = 1
 - $1 \rightarrow 0$ flips dominate for Shift Register = 0
- SET** (glitches)



Effect of reconfig. of Pixel memory

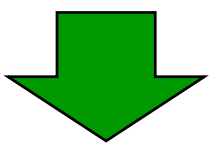
- The noisy and quiet pixels are decreased by reconfiguration action of Pixel memory during a run.
- Reconfiguration of Pixel memory can mitigate effect of SEU/SET.

→ The auto mechanism of Pixel memory reconfiguration was developed.



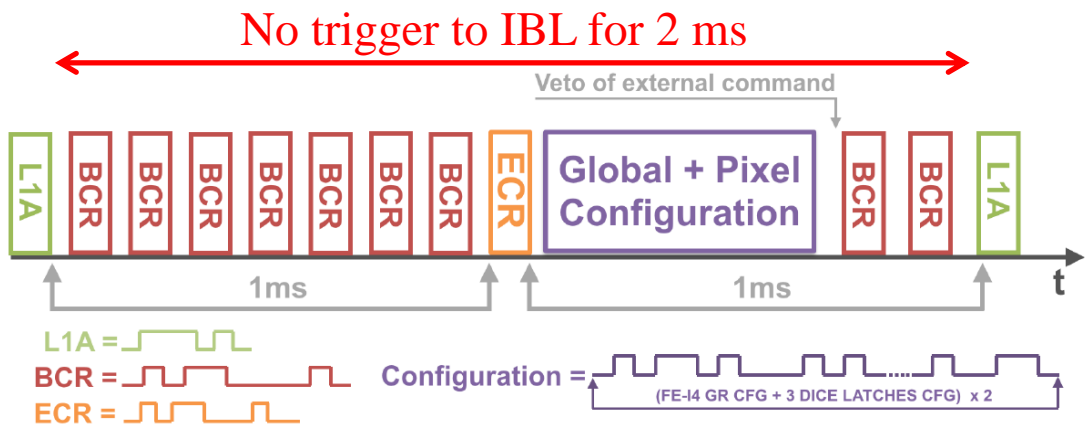
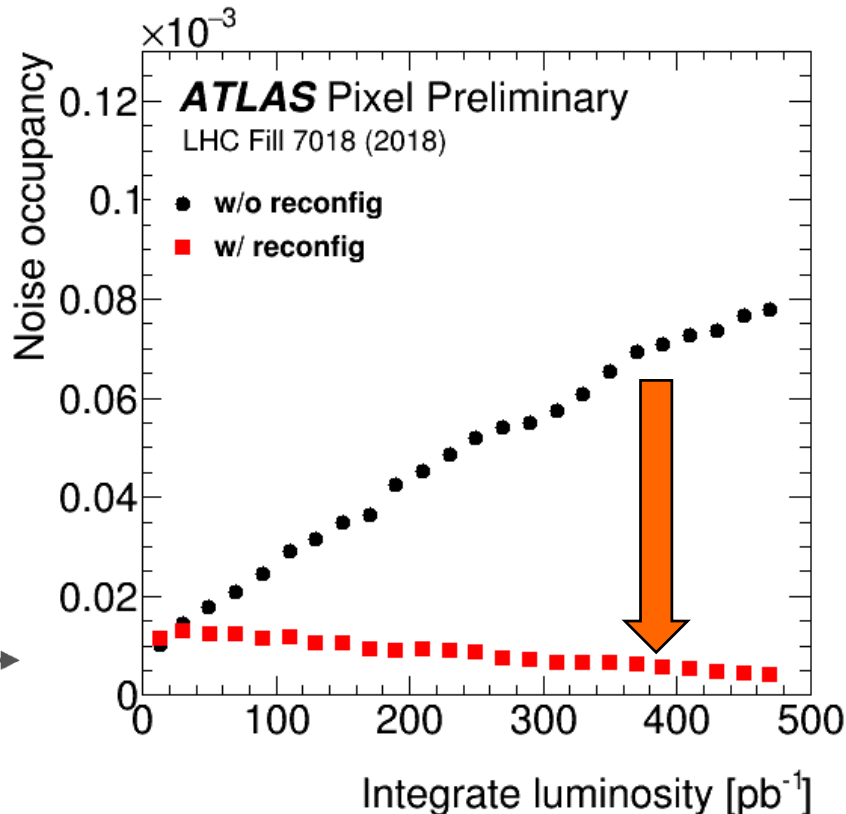
Reconfig. mechanism of Pixel memory

- The auto mechanism of Pixel memory reconfiguration was tested in 2018 data-taking.
- Configuration of Pixel memory is refreshed every 11 minutes for the same module by using ECR timing.



Noise hits caused by SEU/SET could be suppressed to negligible level.

Noise hit occupancy v.s. Int. lumi.



Summary & Conclusions

- IBL is the new innermost Pixel layer installed in 2014 in ATLAS.
- The new front-end chip (FE-I4) was developed for IBL.
- DICE and triple redundant logic are adopted for configuration memories in a FE-I4 to protect from SEU/SET.
- Effect of SEU/SET is getting visible in operation of FE-I4 chips due to high luminosity condition in LHC.
- SET has much more influence on operation of the detector than SEU in IBL.
- SEU/SET can be mitigated to negligible level by re-configuring Global and Pixel memories.

Backup

IBL sensor technology

• Planar and 3D sensors are used for IBL.

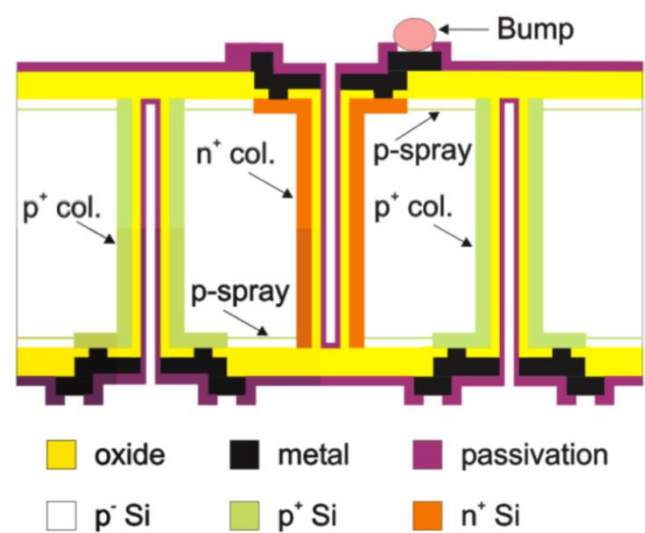
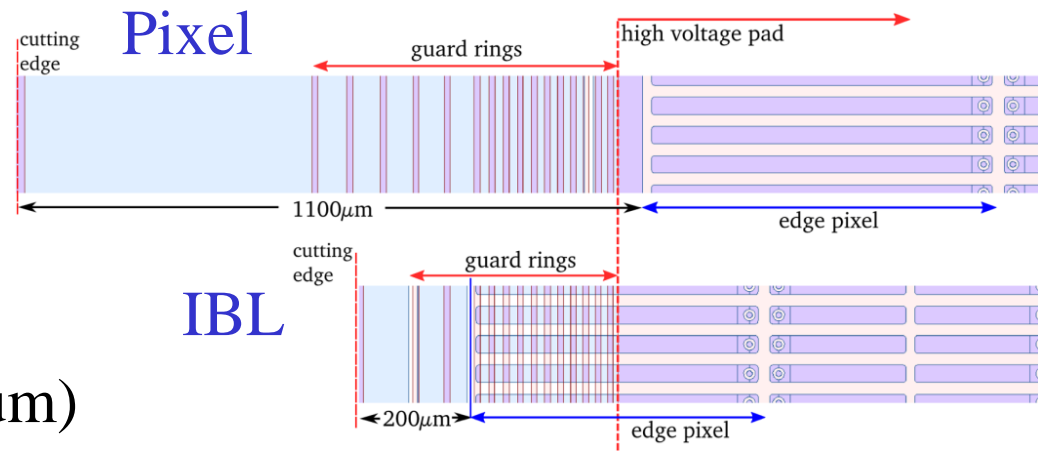
• Pixel size: 50 x 250 μm^2
 (Pixel detector : 50 x 400 μm^2)

Planar sensor

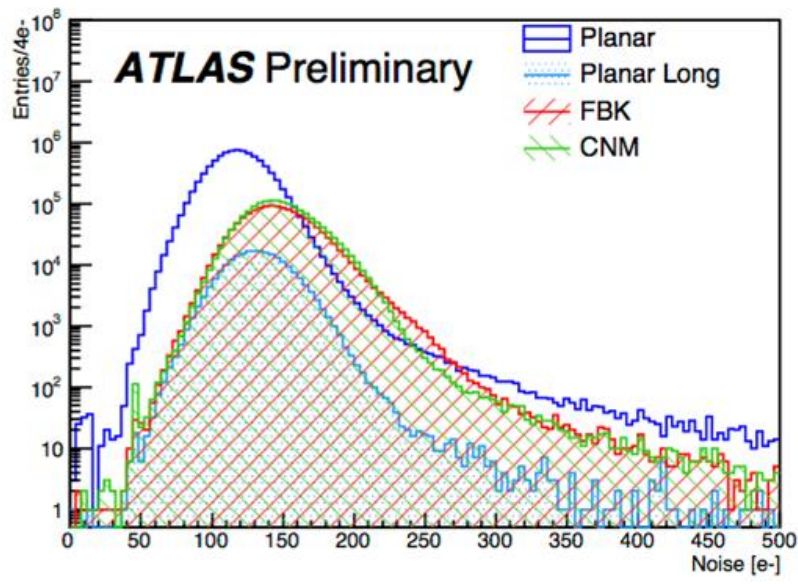
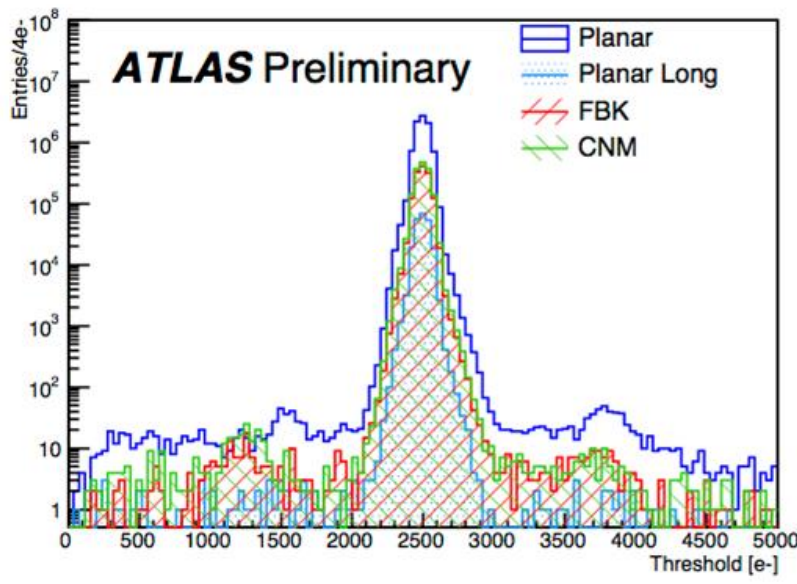
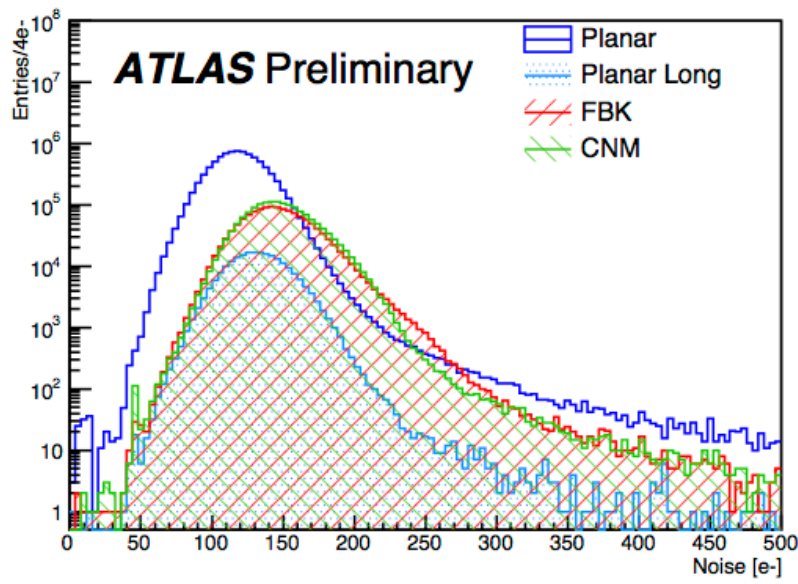
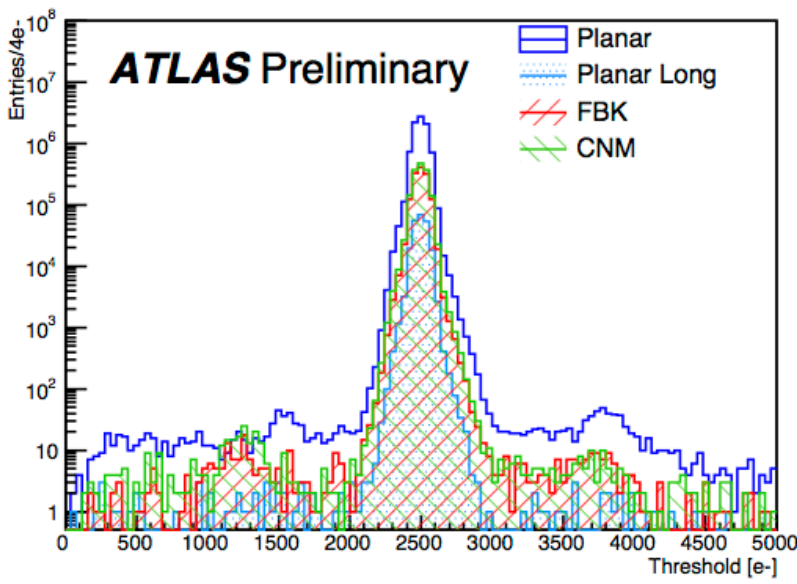
- n⁺-in-n technology
- Thickness: 200 μm (Pixel: 250 μm)
- Small inactive edge region of 200 μm with long pixels under the guard-ring.

3D sensor

- Double-side double type columns process
- n⁺ and p⁺ implant for HV and GND
- Thickness: 230 μm
- Guard ring fence: 200 μm inactive area



Tuning for ToT and threshold

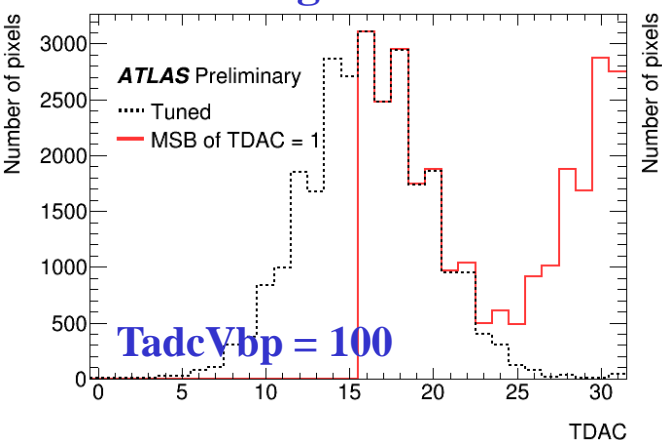


SEU effect on TDAC

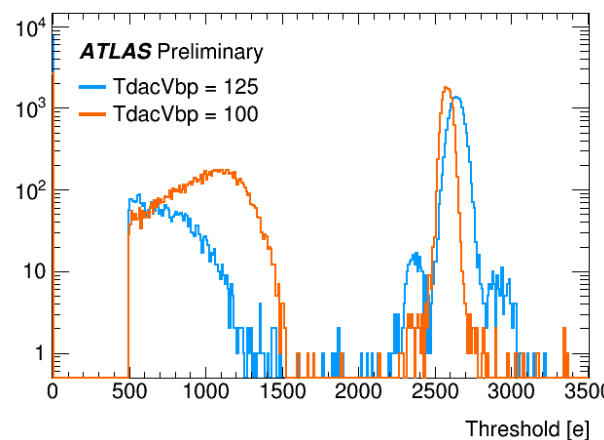
$$\text{Threshold} = \underbrace{f(\text{VthinAlt_Coarse}) + f(\text{VthinAlt_Fine})}_{\text{Global register}} + \underbrace{f(\text{TDAC} * \text{TadcVbp})}_{\text{Pixel register} \text{ and } \text{Global register}}$$

- Threshold is tuned to 2500e with TdacVbp=100 and 125.
- MSB of TDAC is changed to 1.
- FEI-I4 is more robust against noise with lower TdacVbp.

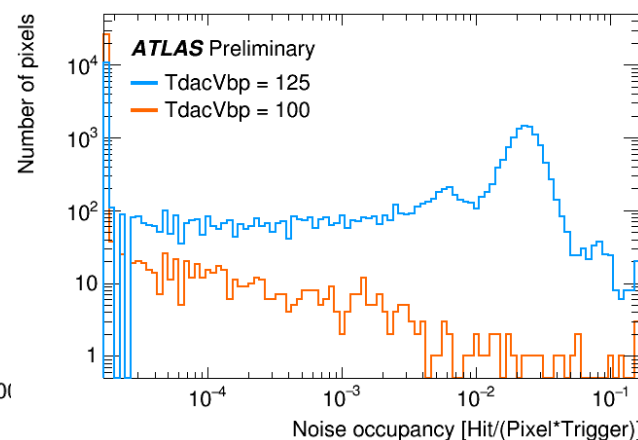
TDAC setting @ Thr.=2500e



Thr. dist. w/ TDAC MSB = 1

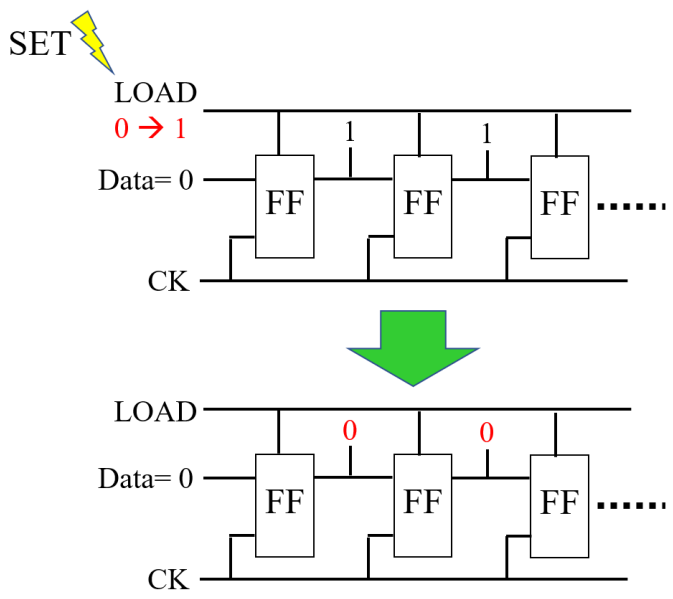


Noise occ. w/ TDAC MSB = 1

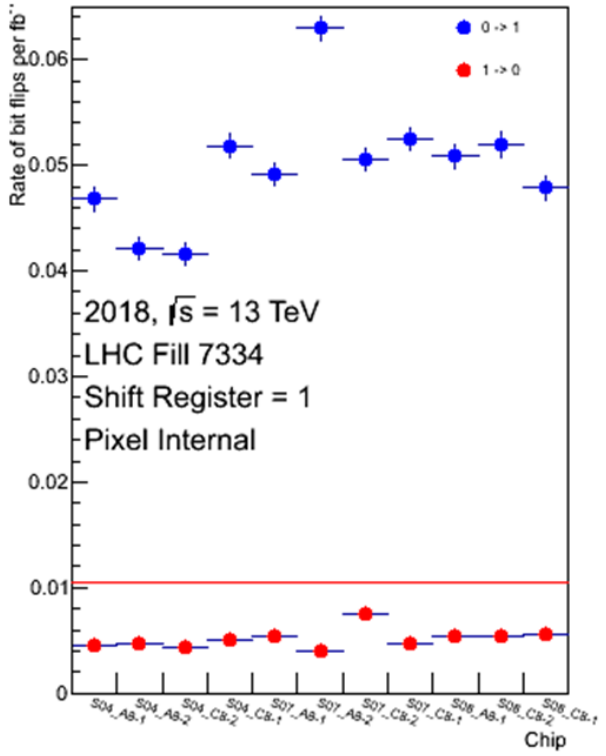


Bit flip rate in Pixel memory

- Average rate of bit flips in Pixel memory was checked for different FE-I4 chips on IBL.
 - $0 \rightarrow 1$ flips dominate for Shift Register = 1
 - $1 \rightarrow 0$ flips dominate for Shift Register = 0
- SET** (glitches)



Bit flip rate (Data In = 1)



Bit flip rate (Data In = 0)

