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Results from test-beam measurements of monolithic pixel detectors in SOI technology

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Tracking and vertex detectors at future linear colliders such as CLIC require a high-precision position measurement. A single-point spatial resolution of about 3 microns is foreseen for the CLIC vertex detector. In order to achieve this goal, detectors with low material budget and small pitch have to be developed. One solution for this are monolithic pixel structures. These do not require bump-bonding of individual sensor and read-out ASICs, which leads to an overall lower material budget with reduced multiple scattering and improved spatial resolution.
The Silicon-On-Insulator CMOS is one of the modern silicon technologies that allows to fabricate the monolithic pixel structures in which the readout electronics and the sensor matrix are integrated on the same wafer. In this talk, the test-beam data analysis results of Lapis 200nm SOI pixel detectors are presented. The SOI detectors were designed in AGH-UST in Cracow and tested at the CERN SPS H6 beam line in 2017.
The presented detectors were fabricated on two different wafers type: FZ(n) and Double SOI(p), with thicknesses of 500 um and 300 um respectively. The pixel size was 30x30 um. The tested matrix consisted of two pixel types: source-follower and charge-preamplifier architecture. The data analyses focused on spatial resolution and efficiency estimation. A novel procedure of eta-correction for multi-pixel clusters was introduced. Moreover, the influence of various clusterization methods on single-point resolution was studied. Finally, single-point resolutions below 2.4 um for the FZ(n) wafer and 3.5 um for the DSOI(p) was achieved. A high detector efficiency of about 98% was measured. Such performance shows that the tested structures are promising prototypes, fulfilling the condition for spatial resolution, for the CLIC vertex and tracking detectors.

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