Performance of the ATLASPix1 pixel sensor prototype in ams aH18 CMOS technology for the ATLAS ITk upgrade

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Reminder: ATLAS ITk upgrade

Why monolithic CMOS for pixel layer L4? Largest surface & moderate radiation

Requirements:

- Efficiency > 99%
- Timing within 25ns
- NIEL up to $1.5 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$
- TID up to 0.8 MGy
- Drop-in compatibility
ATLASPix1 prototype

**Simple, IsoSimple:**
- 25 x 400 pixels
- 130µm x 40µm pitch
- 6bit time-of-arrival
- 10bit time-over-threshold
- Streaming architecture

**M2:**
- 56 x 320 pixels
- 60µm x 50µm pitch
- Triggered architecture

**Engineering run:**
- Preproduction (Batch 1)
- Production (Batch 2)
ATLASPix1 design

Large electrode design

Uniform electric field
Short drift distance
Large(r) capacitance
Produced in ams aH18
180nm HV process

Comparator in pixel/
Logic in periphery

Per-pixel:
3 bit TDAC
1 bit enable
Unused due to issues
Time-over-threshold and charge calibration

- **55Fe**
- **90Sr**
- **3H**

Threshold scale:
- 1620 e / 164 mV

45V HV
- Threshold 75mW
- 200 Ωcm
- Unirradiated
Threshold and noise distribution

Unirradiated

n-irradiated to $10^{15} \text{n}_{\text{eq}} / \text{cm}^2$

Untuned threshold dispersion

$\sim 200 \text{ e}$
Geneva telescope setup

Geneva FE-I4 telescope

Trigger/busy scheme
ATLASPix1 trigger on FPGA

Input clock 50-160 MHz

Data rate (x10) 500-1600 Mbit/s

Timestamps (/2) 25-80 MHz
Matching residuals / n-irradiated $10^{15}$ n_{eq}/cm$^2$

Cluster size

Cuts
- 6 points on track
- $\chi^2 / \text{d.o.f.} < 5$
- $\Delta u,v < 300 \, \mu$m
Occupancies / n-irradiated $10^{15} \text{n}_{eq}/\text{cm}^2$

Tracks

Clusters

Masked pixels effect other in row

Known RAM grounding issue
Efficiency / n-irradiated $10^{15}$ n$_{eq}$/cm$^2$

Global efficiency $99.41\%$

Uniform response

Global efficiency $99.4\%$
(w/o masked lines)
Edge efficiency / n-irradiated $10^{15} \text{n}_{\text{eq}} / \text{cm}^2$

Efficient up to sensor edge
Efficiency scan / n-irradiated

A. Herkert et al. Universität Heidelberg

Data taken w/ MuPix telescope
Irradiated under bias
Batch 1 preproduction
58V HV
Threshold 125mV / 1235e
Efficiency 99.59%
Efficiency scan / p-irradiated $5 \times 10^{14} \text{n}_{\text{eq}} / \text{cm}^2$

Irradiated under bias
70V HV
Data taken w/ MuPix telescope
Naive timing

Cluster time = ToA - Trigger

Average cluster time per row

Length/capacitance dependence of periphery connection
Corrected timing  J. Kröger et al. CERN CLICdp

Measured in CLICdp
Timepix3 telescope
Telescope time resolution ~ 1.2 ns

Row-dependence correction
No timewalk correction (negligible)
RMS ~7.2ns
Fit box+Gauss $\sigma$ ~5.4ns
ATLASPix1 module prototype

F. Sabatini et al. INFN Milano

Four sensor module prototype

Compatible w/ existing Caribou readout system

Flex designed and in production
ATLASPix2

Small prototype w/ focus on periphery
SEU-tolerant global memory
Different pixel memory types
RD53A compatible command decoder
Aurora 64/66 serializer

Available in ams aH18 and TSI 0.18µm
Currently being tested
Foundry availability

Based in Austria
(formerly Austria Mikro systems)
aH18 0.18 µm HV process
Prototypes: ATLASPix1, ATLASPix2

Based in California
0.18 µm HV process
Prototypes: ATLASPix2, ATLASPix3, ...

Compatible

Does not accept submissions anymore

Replacement
Timeline

- **ATLASPix1**
- **ATLASPix2**
- **ATLASPix3**
- **ATLASPix4/CMOS1**

<table>
<thead>
<tr>
<th>Year</th>
<th>Chip</th>
<th>Status</th>
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<tbody>
<tr>
<td>2017</td>
<td>ATLASPix1</td>
<td>MuPix8, AtlasPix1 M2, AtlasPix1 Simple, AtlasPix1 IsoSimple</td>
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<tr>
<td>2018</td>
<td>ATLASPix2</td>
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<tr>
<td>2019</td>
<td>ATLASPix3</td>
<td>Full scale, Preproduction, Prototype</td>
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<tr>
<td></td>
<td>ATLASPix4/CMOS1</td>
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Collaborators
Summary

ATLASPix1 results
- Efficiency unirradiated > 99.5%
- Efficiency @ $10^{15} \text{n}_{eq}/\text{cm}^2 > 99\%$
- Time resolution < 10 ns

Towards production module:
- Single event effects
- Full-scale design
- Qualification of TSI process

Successful prototype and measurement campaign