The Monopix chips: Depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS Inner Tracker upgrade

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On behalf of the LF-/TJ- Monopix design and measurement teams:
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The ATLAS experiment will upgrade its inner tracker system for the HL-LHC

Max. instantaneous luminosity: of \(7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}\)
(~200 interactions per bunch crossing)

<table>
<thead>
<tr>
<th></th>
<th>Inner layer</th>
<th>Outer Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Occupancy</td>
<td>30 MHz/mm²</td>
<td>1 MHz/mm²</td>
</tr>
<tr>
<td>NIEL</td>
<td>(10^{16} \text{ n}_{eq}/\text{cm}^2)</td>
<td>(10^{15} \text{ n}_{eq}/\text{cm}^2)</td>
</tr>
<tr>
<td>TID</td>
<td>1 Grad</td>
<td>80 Mrad</td>
</tr>
<tr>
<td>Area</td>
<td>0(1m²)</td>
<td>0(10m²)</td>
</tr>
</tbody>
</table>

Radiation-hard hybrid pixel sensors will remain as the baseline (RD-53):
- Significant material budget (3% X₀ per layer).
- Complex (and expensive) module production.

**A complementary option for the outer layer?**
Depleted monolithic sensors in CMOS technology
THE MONOPIX CHIPS

DMAPS with an integrated column-drain read-out architecture
(fast synchronous read-out architecture)

**LF-MONOPIX01**
(March 2017)

Large fill-factor design in LFoundry 150 nm CMOS technology

**TJ-MONOPIX01**
(February 2018)

Small fill-factor design in Towerjazz 180 nm CMOS technology with a process modification

T. Wang, et al.
DOI: 10.1088/1748-0221/12/01/C01039
P. Rymaszewski et al.
DOI: http://doi.org/10.22323/1.313.0045
T. Hirono, et al.
DOI: 10.1016/j.nima.2018.10.059

T. Wang, et al.
DOI: 10.1088/1748-0221/13/03/C03039
K. Moustakas, et al.
DOI: 10.1016/j.nima.2018.09.100
**COLUMN-DRAIN R/0 ARCHITECTURE**

*Why? Sufficient rate capability with affordable in-pixel logic density for CMOS pixels*

- Column-drain has already proven to be capable to handle the hit rates of the current inner ATLAS pixel layers (FE-I3)
- Simulation studies for the outmost HL-LHC pixel layers agree

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**Hits in the column are read out on a shared data bus, arbitrated by the token passing scheme**

**BC ID (40 MHz) distributed in the column**

**Hits time-stamped in pixel**
- ToA from LE time stamp
- ToT = TE - LE
DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS (DMAPS)

DMAPS in CMOS technology are suitable candidates for the outmost pixel layers

Commercial process, no hybridization (Reduced material budget and costs), considerable depleted regions in high-resistive substrates, fast charge collection by drift, multiple wells for shielding, scalable.

**Two approaches:**

**“Large Fill Factor”**
Large collecting well containing all the electronics

**PROS:** Short drift distances, strong E-field (Rad-hard)

**CONS:** Large sensor capacitance (Compromise on timing and noise), higher analog power.

**“Small Fill Factor”**
Small collecting well, separate from the electronics

**PROS:** Very small sensor capacitance

**CONS:** Long drift distances, compromised rad-hardness
LF-MONOPIX01

- **Large fill-factor** design in LF 150 nm CMOS technology
- High resistive substrate (>2 kOhm-cm)
- Large 50 x 250 µm² pixel array (129 x 36)
- Bunch-crossing clock frequency (40MHz clock)
- 40 MHz (up to 160MHz by design) LVDS serial output
- Charge ADC sampling: 8-bit LE/TE time stamps (ToT)
- Power: 55 µW/pixel (~1.7W/cm²)

Radiation-hardness and sensor layout optimized in previous prototypes

- Succesful design efforts for cross-talk mitigation
- Fast and low-power CSA and discriminator implementations
PICTURE LAYOUT IN LF-MONOPIX01

AC coupling cap.  
CSA + Discri. + TDAC  
Pixel config. R.O. logic  
RAM/ROM cells

Depleted Area  
P-Substrate  
Deep N-Well (Collection Electrode)

~100 μm
TOT RESPONSE AND INJECTION CAPACITANCE

-> Injecting charge directly to the pre-amplifier.

+ Low feedback voltage (VPFB): Longer ToT
  (sampling with higher resolution)

\[ Y(Tot) = a * (1 - \exp(-x/c)) \]
\[ a = 153,086 \]
\[ c = 0.445 \]
\[ \chi^2 = 0.717 \]
\[ \text{MaxToT} = 120.568 \]

(Assuming 3.6 eV/e-)

\[ ^{241}\text{Am}: \quad 16539 \text{ e-} \]
\[ \text{Tb X-rays:} \]
\[ K_\alpha \quad 12353 \text{ e-} \]
\[ K_\beta \quad 13997 \text{ e-} \]

\[ C_{\text{inj}} = Q / V \sim 2.75 \text{ fF} \]

ToT can also be used for event differentiation or time-walk corrections.
**BREAKDOWN AND DEPLETION**

**Breakdown Voltage ~ -280 V**

**Large collected charge (~10^4 e-) in a highly resistive (>2 kOhm-cm) substrate.**

**200μm thick chip fully depleted at ~60V**

(Measurements at room temperature)
NOISE AND GAIN

**Gain** within 10-12 µV/e-  
(Mainly related to the discriminator version)

**ENC** within 180-240 e-, with a dispersion between 30 to 70 e-.

* Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C

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Performance after NIEL irradiation to $1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$

- No loss in gain after irradiation
- Up to 150 e- noise increase due to ~1 MRad TID background in JSI
TUNING OF THRESHOLD DISTRIBUTIONS

**Injection tuning:** Fix global threshold
+ Binary search for optimal local threshold tuning

- Threshold tunable down to \(~1400\text{e}^-\)
- Noise occ. \(< 10^{-7} \text{ hits/BX}\)

Before tuning:
- \(\sigma_2 >> \sigma_1 (\sim 600\text{e}^-)\)

After tuning:
- \(\sigma_2 \sim \sigma_1 (\sim 100\text{e}^-)\)

Unirradiated

Threshold still tunable after irradiation

\(\sigma_1 \sim 130\text{e}^-\)

@ \(1 \times 10^{15} \text{n}_{eq}/\text{cm}^2\)

**Baseline tuning:** Lower global threshold close to baseline
+ Tune local threshold according to noise hits

- Threshold tunable down to \(~1400\text{e}^-\)
- Noise occ. \(< 10^{-7} \text{ hits/BX}\)

Tuned threshold dispersion \(~100\text{e}^-\)
Leakage current and TOT response

- **Leakage current**
  - Measured at -27.5°C
  - Bias: -200V @ -27.5°C

- **ToT response**
  - Breakdown voltage still > 200V after $1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ NIEL
  - ToT response not affected
**TB WITH 2.5 GEV ELECTRONS: HIT EFFICIENCY**

- **Non-irradiated**
  - Hit efficiency @ Noise occ. $< 10^{-7}$, TH~1700e- ($<10^{-7} @ 1400e-)$
  - 1% masked pixels from noise tuning (not broken).

- **Neutron irradiated (1 x $10^{15}$n$_{eq}$/cm$^2$)**
  - Hit efficiency @ Noise occ. $< 10^{-8}$, TH~1700e-
  - $< 0.2%$ masked pixels from noise tuning.
  - Efficiency loss between pixels, as expected.

99.6% @ -200V

98.9% @ -130V

(Voltage limited due to technical issues)
TB WITH 180 GEV PIONS: IN-PIXEL EFFICIENCY

- Deep N-well (Collecting electrode...)
- P-well (Inter-pixel region, isolation of electronics...)
- N-well (R/O electronics...)

**Efficiency**

- **99.7% @ -200V**
- **98.8% @ -5V**

**Uniform efficiency**

**Efficiency drop only between pixels at VERY low bias V**

5 μm*5 μm bins
TIMING PERFORMANCE (AT DEFAULT SETTINGS)

- >80% of events are within 2 bins after neutron irradiation up to $1 \times 10^{15} \text{neq/cm}^2$.
  \textbf{Remarkable for a} $C_d\sim400\text{ff}$ \textbf{and promising for new designs with smaller} $C_d$ (Optimized Fill-Factor).
- \textbf{There is still room for improvement:}
  Optimization of parameters (current of CSA, discriminator, etc.), higher bias voltage, back side process.

Measurements with thinned chips and higher resolution ongoing.
• **Small fill-factor** design in TJ 180 nm CMOS technology
• Highly resistive p-epitaxial layer (1 kOhm-cm) with a process modification (additional n-type planar layer)
• Large 36 x 40 µm² pixel array (224 x 448)
• Bunch-crossing clock frequency (40MHz clock)
• 40 MHz CMOS serial output per flavour
• Charge sampling: 6-bit LE/TE time stamps (ToT)
• Power: 3 µW/pixel (~0.18 W/cm²)
PROCESS MODIFICATION IN TOWERJAZZ 180NM

Standard Process

Modified Process

Rad-hard modified process tested on an “Investigator” chip

97% efficiency after $1 \times 10^{15} \text{n}_{eq}/\text{cm}^2$
(100e- threshold, 30 µm square pixel)

W. Snoeys et al.
DOI: 10.1016/j.nima.2017.07.046

H. Perenegger, et al.
DOI: 10.1088/1748-0221/12/06/P06008
Different P-well coverage on top and bottom column regions

2x2 pixel array (Top view)
CALIBRATION OF THE INJECTION CIRCUIT

• Calibration values are similar in "Top" and "Bottom", but different for unirradiated and irradiated samples:
  - **Unirradiated:** ~33e-/DAC
  - **1x10^{15} Irradiated:** ~42e-/DAC
Unirradiated: $\mu = 349e^{-}$, $\sigma = 34e^{-}$

1x$10^{15}$ Irradiated: $\mu = 569e^{-}$, $\sigma = 66e^{-}$

ENC increased by $\sim 10e^{-}$ after $1x10^{15} n_{eq}/cm^2$ (Probably due to TID bckg)

* Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C
IN-PIXEL EFFICIENCY (UNIRRADIATED)

Low efficiency "corners" correlated with large active areas used for decoupling capacitors

--- Design layout to be optimized in future designs
MEAN HIT EFFICIENCY VS DEEP P-WELL COVERAGE

- Lower efficiencies in Full DP-Well regions (Bottom) than in Removed DP-Well (Top) ones.
Large efficiency drop (30-50%) after $1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ neutron irradiation.

---> Fixes to the TJ modified process in pixel corners to enhance E-Field (M. Munker, PIXEL 2018 / Talk 53)
TIMING PERFORMANCE

Distributions of "HIT_OR signal - External trigger timestamp" in seed pixels from test beam (640 MHz sampling)

93% | 98% (hits within 50 ns)

Unirradiated

1x10^{15} n_{eq}/cm^2
**CONCLUSIONS**

**Operational column-drain read-out** on fully monolithic CMOS pixel detectors in both small and large fill factor designs on a large pixel matrix

<table>
<thead>
<tr>
<th>DMAPS type</th>
<th>LF-MONOPIX01</th>
<th>TJ-MONOPIX01</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Large FF</td>
<td>Small FF</td>
</tr>
<tr>
<td></td>
<td>(150nm CMOS</td>
<td>(180nm CMOS, mod.</td>
</tr>
<tr>
<td></td>
<td>LFoundry)</td>
<td>Towerjazz)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Signal MPV</th>
<th>LF-MONOPIX01</th>
<th>TJ-MONOPIX01</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Non-Irrad</td>
<td>$10^{15}n_{eq}/cm^2$</td>
</tr>
<tr>
<td>~16ke- (@60V)</td>
<td>~5.6ke</td>
<td>~1.6ke-</td>
</tr>
<tr>
<td>~200±50e</td>
<td>~350±50e</td>
<td>~15±2e</td>
</tr>
</tbody>
</table>

| ENC | LF-MONOPIX01 | TJ-MONOPIX01 |
| ~1400±100e | >1700±130e | >350±35e | >570±65e |
| >350±35e | >570±65e |

| Threshold | LF-MONOPIX01 | TJ-MONOPIX01 |
| ~150±50e | ~350±50e | ~15±2e | ~25±3e |

| Mean Effic. | LF-MONOPIX01 | TJ-MONOPIX01 |
| 99.6% | 98.9% | 97.1% | 69.4% |

| Hits in 50ns | LF-MONOPIX01 | TJ-MONOPIX01 |
| 98.7% (*) | 83% (*) | 93% | 98% |

(*) Still room for optimization.
WHAT'S NEXT?

- **LF-MONOPIX02 (end 2019)**
  - Next iteration with CSA and discriminators with the best performance.
  - Smaller pixel size (150x50) to reduce detector capacitance.

- **TJ-MONOPIX02 (end 2019)**
  - Pixel layout according to the best performing fix to the TJ modified process in miniMALTA.
  - Threshold tuning and reduction.
  - Optimize active area layout in pixels.

- **CMOS-1 (mid-2020)**
  
  RD-53 like, full size chip in a selected CMOS process and fill-factor approach.

<table>
<thead>
<tr>
<th></th>
<th>LF-MonopixO2</th>
<th>RD53 outer layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>50 × 150 μm²</td>
<td>50 × 50 μm²</td>
</tr>
<tr>
<td>Analog power</td>
<td>16 - 20 μA/pixel</td>
<td>3 - 4 μA/pixel</td>
</tr>
<tr>
<td>Digital power</td>
<td>4 - 5 μA/pixel</td>
<td>2 - 3 μA/pixel</td>
</tr>
<tr>
<td>In-time thres.</td>
<td>1500 - 2000 e⁻</td>
<td>1500 e⁻</td>
</tr>
<tr>
<td>Min. detectable charge</td>
<td>1000 - 1500 e⁻</td>
<td>1000 e⁻</td>
</tr>
</tbody>
</table>

M. Munkers's presentation (PIXEL 2018 / Talk 53)
Thank you for your attention.

Q&A Time!

This research project received funding from the European Union’s Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

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**CMOS DEMONSTRATOR PROGRAM**

A collaborative R&D effort within ATLAS focused on DMAPS prototypes with fast read-out architectures in different CMOS processes.

Previous iterations of these prototypes (passive sensors, or active ones with a first stage of the Front-End within the pixel) allowed to optimize the designs and improve radiation-hardness.

<table>
<thead>
<tr>
<th>Chip name</th>
<th>Technology</th>
<th>Fill factor</th>
<th>Pixel size [µm^2]</th>
<th>R/O architecture</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATLASpix</td>
<td>Foundry 1 180nm</td>
<td>Large</td>
<td>56 x 56</td>
<td>Asynchronous</td>
<td>Measurements</td>
</tr>
<tr>
<td>MALTA</td>
<td>Foundry 2 180nm</td>
<td>Small</td>
<td>36 x 36</td>
<td>Asynchronous</td>
<td>Measurements</td>
</tr>
<tr>
<td>TJ Monopix</td>
<td></td>
<td>Small</td>
<td>36 x 40</td>
<td>Synchronous</td>
<td></td>
</tr>
<tr>
<td>Coolpix</td>
<td></td>
<td>Large</td>
<td>50 x 250</td>
<td>Synchronous</td>
<td></td>
</tr>
<tr>
<td>LF Monopix</td>
<td>Foundry 3 150 nm</td>
<td>Large</td>
<td>50 x 250</td>
<td>Synchronous</td>
<td>Measurements</td>
</tr>
<tr>
<td>LF2</td>
<td></td>
<td>Large</td>
<td>50 x 50</td>
<td>Synchronous</td>
<td></td>
</tr>
</tbody>
</table>
FROM LF-CPIX TO LF-MONOPIX

LF-CPIX Demonstrator (50 x 250 µm²)

LF-MONOPIX01 (50 x 250 µm²)

Large fill factor design. $C_d \sim 400\text{fF}$

An increase in detector capacitance has implications on timing and noise

Electronics are directly coupled to the collecting node through $C_{pw}$

- Special efforts on design to minimize cross-talk with digital signals
- Increase of minimum operational threshold
**PROTOTYPE DEVELOPMENT LINE**

**CCPD_LF**
- Subm. in Sep. 2014
- 33 x 125 µm² pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test

**LF-CPIX (DEMO)**
- Subm. in Mar. 2016
- CPIX Demonstrator in LF
- 50 x 250 µm² pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test

**LF-MONOPIX01 (Monolithic)**
- Subm. in Aug. 2016
  (Back: End of Mar. 2017)
- "Demonstrator size"
- 50 x 250 µm² pixels
- 150 nm CMOS
- Fast (Col. Drain) standalone R/O

Irradiated without substantial performance loss

Fully integrated Speed and digital R/O
DESIGN CHALLENGES

MINIMIZING CROSS-TALK

In Token propagation:

“Current steering logic”
-> Limit the current to avoid glitches

In Data R/O (LE/TE, address):

Differential lines + Source followers
-> Avoids current injection into the PW when switching from high to low

Column-drain R/O logic

8-bit LE/TE time-stamps (ToT) + Address
PREAMPLIFIERS AND DISCRIMINATORS

Bias $I \sim 17 \mu A$
Peak time $\sim 20$ ns
(4ke- signal)
ENC (Simulation) $\sim 170$ e-

Bias $I \sim 15 \mu A$
Peak time $\sim 25$ ns
(4ke- signal)
ENC (Simulation) $\sim 135$ e-

Bias $I \sim 4.5 \mu A$
Two-stage open loop structure

Self-bias $< 4 \mu A$
Self-biased differential amplifier + CMOS inverter

Faster
(Analog power from periphery)

Faster

$\sim 34$ ns
$\sim 23$ ns

T. Wang, Bonn
TOT RESPONSE AND CALIBRATION

Data from energy loss by 2.5 GeV electrons (MIPs) in silicon for different bias voltages (without cluster size selection)

Landau+Gaussian convolution fit to describe every calibrated distribution.

Applying per-pixel calibration

~250 μm depleted at 100V

R ~ 7.3 kOhm-cm

> 2 kOhm-cm, but also higher than previous measurements in other wafers from the same foundry (3.5 and 5.5 kOhm-cm)
ENC within 120 to 240 e-, with a dispersion between 30 to 70 e-.

Gain within 10-12 µV / e-
Untuned threshold dispersion for flavours with the V1 discriminator ~400-600 e- (plus 350-400 e- for those with integrated pixel R/O logic and the V2 discriminator)
NOISE OCCUPANCY AT LOW THRESHOLD

- Non-irradiated
  - Threshold: 1400 e-
  - Dispersion due to noise baseline tuning
  - Bias V: -200V
  - Cooled with dry ice.

- Neutron irradiated ($1 \times 10^{15} n_{eq}/cm^2$)
  - Threshold: 1700 e-
  - Bias V: -130V (due to technical issues)
  - Cooled with dry ice.

Noise occupancy <10^{-7} @ TH~1400e-

Noise occupancy <10^{-8} @ TH~1700e-
(After irradiation)
TEST BEAM CAMPAIGNS

- **MIMOSA26 x 6**
  - Pixel size: 18.2 μm x 18.2μm
  - 1152 μs/frame (rolling shutter)

- **FE-I4 x 1**
  - Pixel size: 250 μm x 50 μm
  - Timing resolution: 25ns (trig. by scintillator + TLU)

LF-MONOPIX (unirradiated and neutron-irradiated samples) exposed to MIPs at ELSA (2.5 GeV e-) and the H8 line of CERN's SPS (180 GeV pions)

Sample of event correlation (@SPS) MONOPIX <-> MIM26 (6)
TEST BEAM CAMPAIGNS

MONOPIX planes (unirradiated and neutron-irradiated samples) exposed to MIPs at ELSA (2.5 GeV e−) and the H8 line of CERN’s SPS (180 GeV pions):

Measurements for different bias and threshold settings.

- Avg: 2.2
- Max: ~20 clust/frame

- Avg: 0.8
- Max: ~6 clust/frame
TB @ ELSA: IN-PIXEL EFFICIENCY

Non-irradiated @ -200V:
Uniform efficiency

Neutron irradiated \( (1 \times 10^{15} n_{\text{eq}}/\text{cm}^2) \) @-130V
Observed efficiency loss between pixels
E-TCT MEASUREMENTS

*Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C

E-TCT measurement on LF test structures thinned to 200µm
I. Mandić, RD50 workshop 2017

E-TCT measurement on LF-MONOPIX (775µm thick)
Improvement after Backside-process

Not thinned, not irradiated
Not thinned, 1e13
Not thinned, 5e13
Not thinned, 1e14
Thinned, not irradiated
Thinned, 1e13
Thinned, 5e13
Thinned, 1e14
Thinned, 5e14
Thinned, 1e15
Thinned, 2e15

E-TCT measurement on LF test structures thinned and Backside-processed to 200µm
I. Mandić, RD50 workshop 2017

Reduction in leakage current after thinning and BS-process

* Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C
Gain of ~400 uV/e- (or larger) achieved under different bias schemes
IN-PIXEL EFFICIENCY (UNIRRADIATED PMOS VS HV)

PMOS

- W4_Pmos PSUB=-20V, PWELL=-5V, HV=-0V, Pix_Efficiency_RDPW (Unirradiated)
  - 95.9%

- W4_Pmos PSUB=-20V, PWELL=-5V, HV=30V, Pix_Efficiency_RDPW (Unirradiated)
  - 93.5%

HV

- W4_HV PSUB=-16V, PWELL=-0V, HV=30V, Pix_Efficiency_RDPW (Unirradiated)
  - 97.1%

- W4_HV PSUB=-16V, PWELL=-0V, HV=30V, Pix_Efficiency_RDPW (Unirradiated)
  - 93.7%
DIFFERENCES DUE TO N-LAYER DOPING

W04 (HV): UNIRRADIATED

- Mean efficiency larger for unirradiated W4 than for W12

W12 (HV): UNIRRADIATED

(Noise occupancy < 10 Hz/pixel)
The cluster size decreases after irradiation ---> Less charge sharing.
We observe charge sharing in the unirradiated sample, but not after irradiation (This observation agrees with the cluster size measurement during test beam)