The Monopix chips: Depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS Inner Tracker upgrade

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On behalf of the LF-/TJ- Monopix design and measurement teams:
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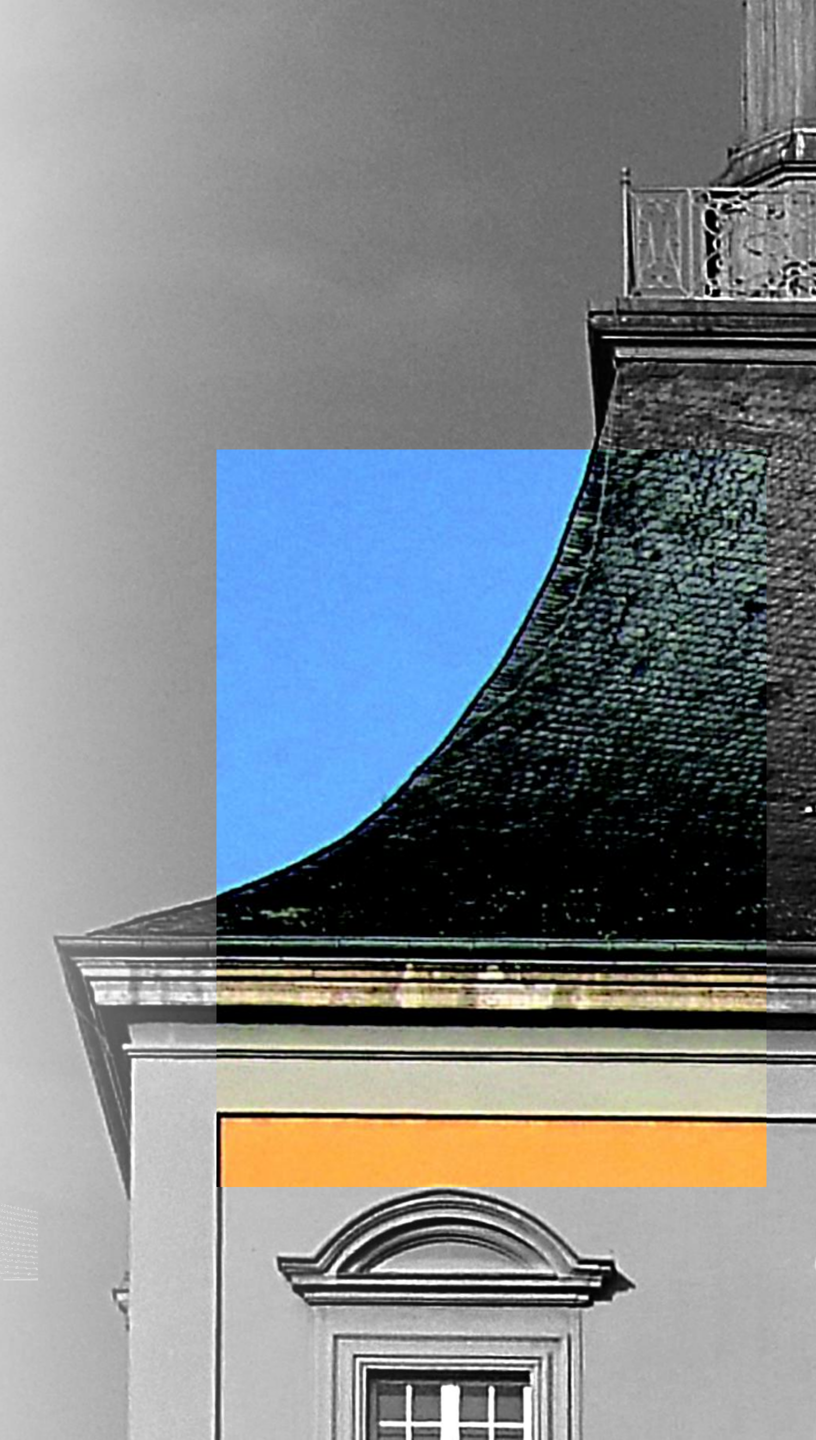
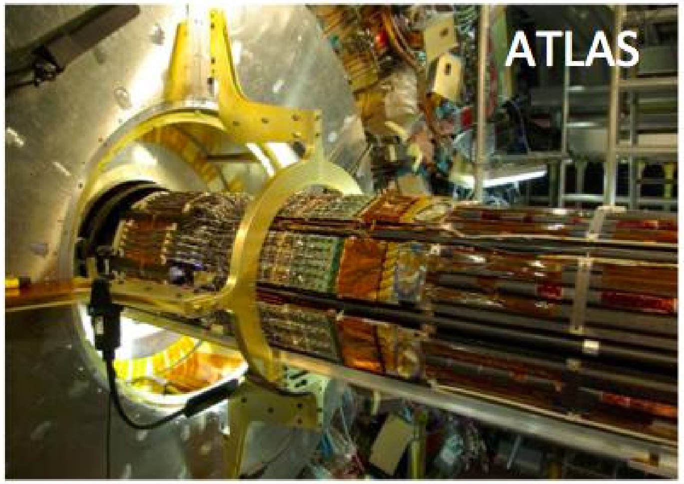


THE ATLAS INNER TRACKER UPGRADE FOR THE HL-LHC

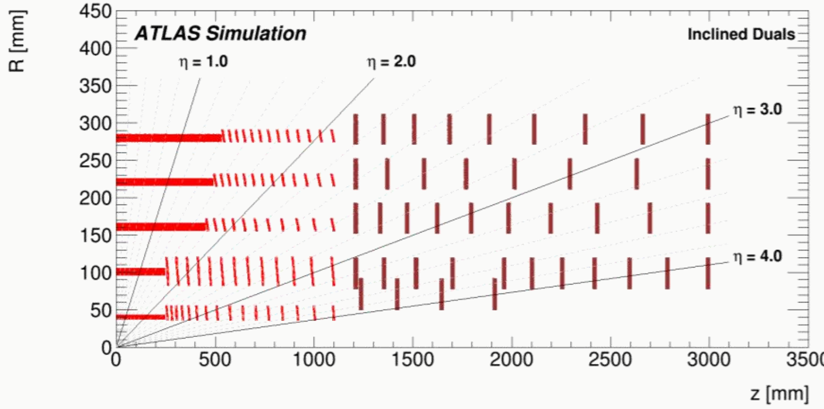
The ATLAS experiment will upgrade its inner tracker system for the HL-LHC



Max. instantaneous luminosity: of 7.5 x 10^{34} cm^{-2} s^{-1}
(~200 interactions per bunch crossing)

	Inner layer	Outer Layer
Occupancy	30 MHz/mm²	1 MHz/mm²
NIEL	10^{16} n_{eq}/cm^2	10^{15} n_{eq}/cm^2
TID	1 Grad	80 Mrad
Area	O(1m²)	O(10m²)

\+ **Fast R/O architecture with 25 ns precision**



ATLAS ITK Pixel Layout
(CERN-LHCC-2017-021 / ATLAS-TDR-030)

Radiation-hard hybrid pixel sensors will remain as the baseline (RD-53):
- Significant material budget (3% Xo per layer).
- Complex (and expensive) module production.

A complementary option for the outer layer?
Depleted monolithic sensors in CMOS technology

THE MONOPIX CHIPS

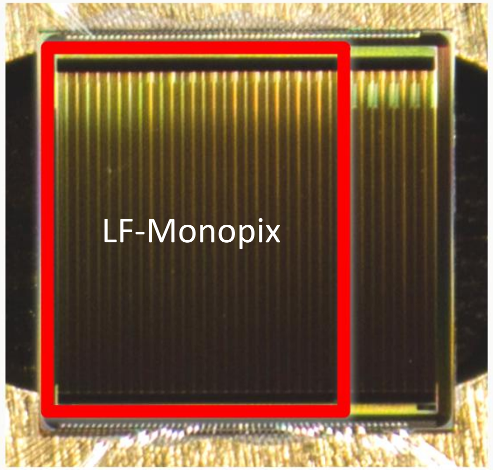
DMAPS with an integrated column-drain read-out architecture

(fast synchronous read-out architecture)

LF-MONOPIX01

(March 2017)

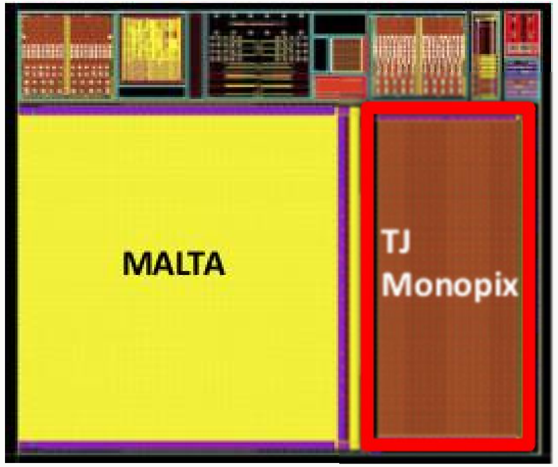
Large fill-factor design in **LFoundry 150 nm CMOS** technology



T. Wang, et al.
DOI: 10.1088/1748-0221/12/01/C01039
P. Rymaszewski et al.
DOI: http://doi.org/10.22323/1.313.0045
T. Hirono, et al.
DOI: 10.1016/j.nima.2018.10.059

TJ-MONOPIX01

(February 2018)

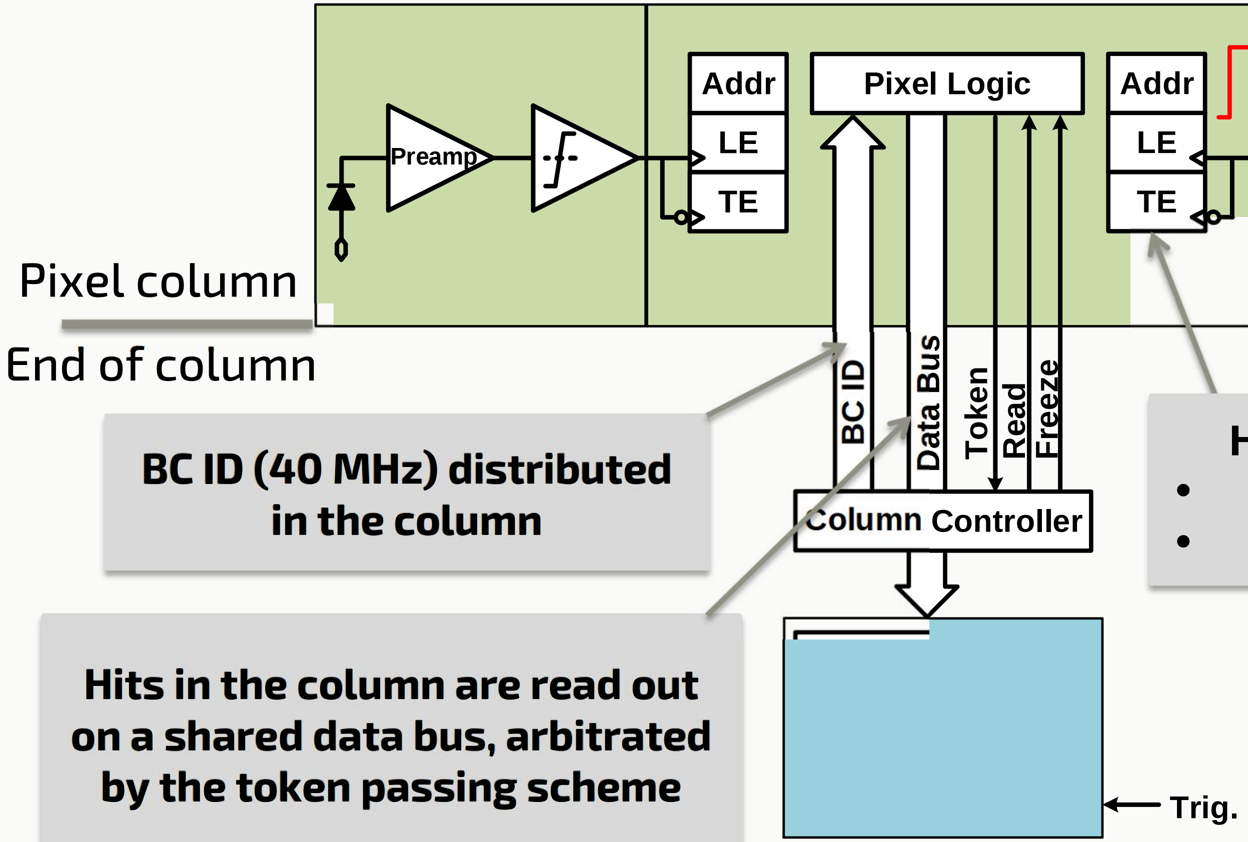


Small fill-factor design in **Towerjazz 180 nm CMOS** technology with a process modification

T. Wang, et al.
DOI: 10.1088/1748-0221/13/03/C03039
K. Moustakas, et al.
DOI: 10.1016/j.nima.2018.09.100

COLUMN-DRAIN R/O ARCHITECTURE

Why? Sufficient rate capability with affordable in-pixel logic density for CMOS pixels



BC ID (40 MHz) distributed in the column

Hits in the column are read out on a shared data bus, arbitrated by the token passing scheme

Hits time-stamped in pixel

- ToA from LE time stamp
- ToT = TE -LE

Column-drain has already proven to be capable to handle the hit rates of the current inner ATLAS pixel layers (FE-I3)

☑

Simulation studies for the outmost HL-LHC pixel layers agree

☑

DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS (DMAPS)

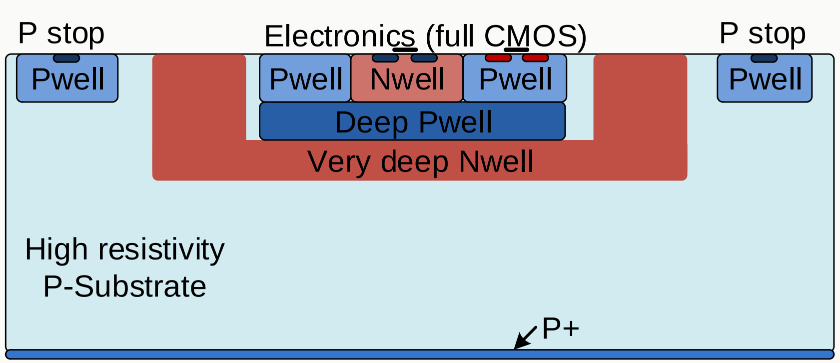
DMAPS in CMOS technology are suitable candidates for the outmost pixel layers

Commercial process, no hybridization (Reduced material budget and costs), considerable depleted regions in high-resistive substrates, fast charge collection by drift, multiple wells for shielding, scalable.

Two approaches:

"Large Fill Factor"

Large collecting well containing all the electronics

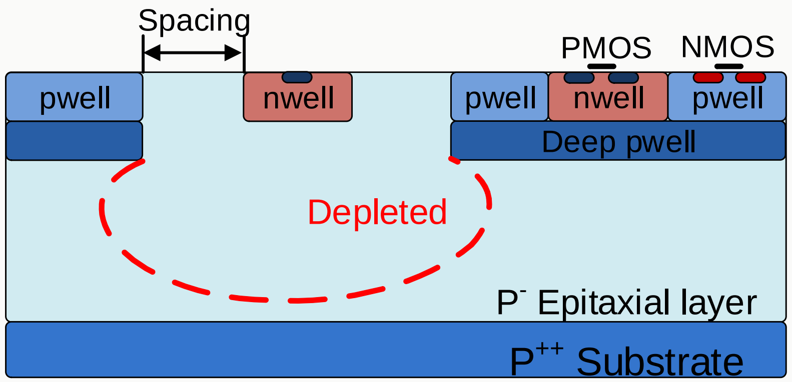


PROS: Short drift distances, strong E-field (Rad-hard)

CONS: Large sensor capacitance (Compromise on timing and noise), higher analog power.

"Small Fill Factor"

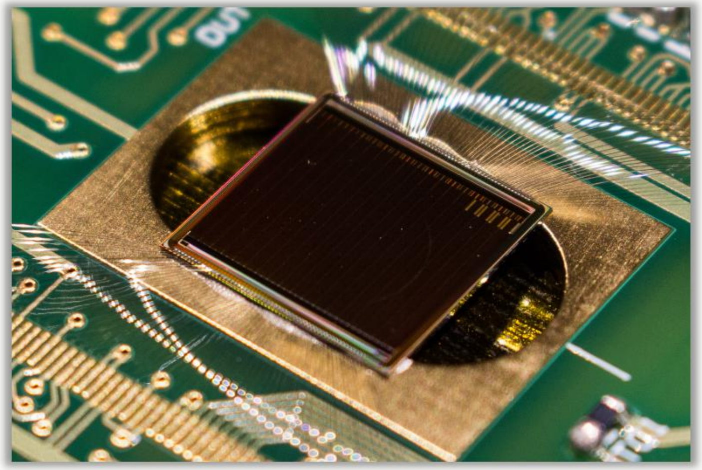
Small collecting well, separate from the electronics

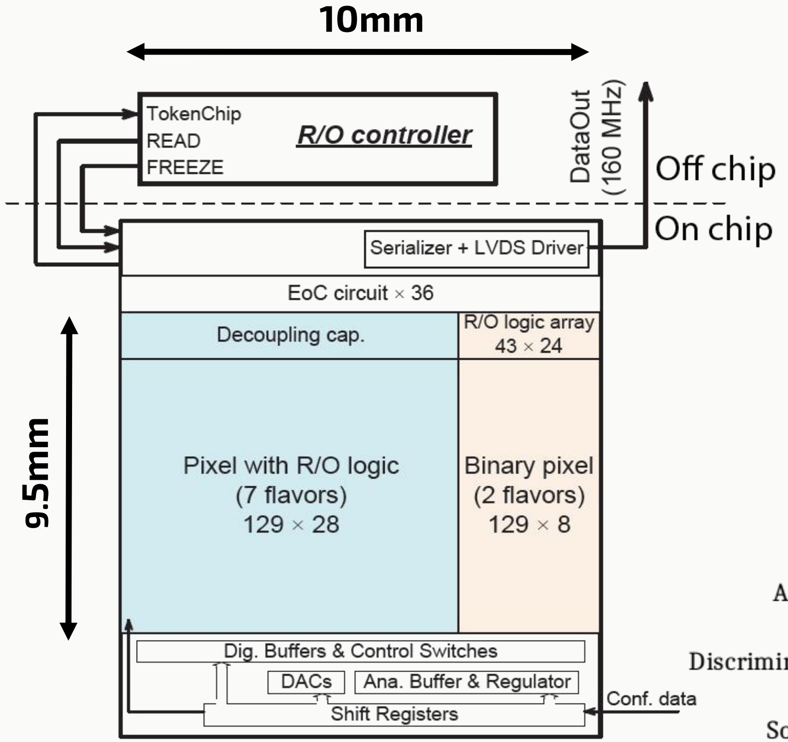


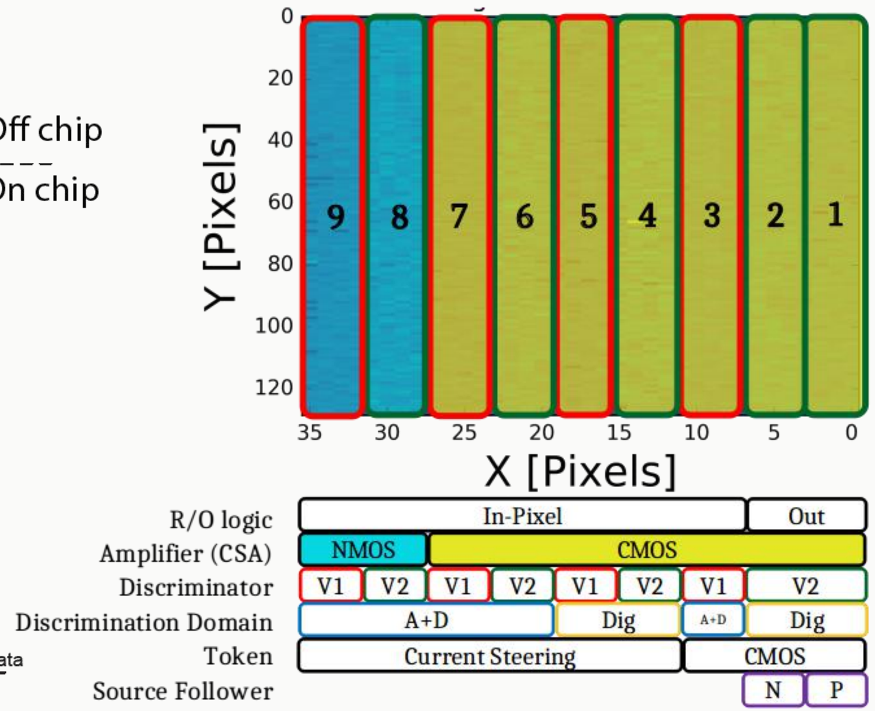
PROS: Very small sensor capacitance

CONS: Long drift distances, compromised rad-hardness

LF-MONOPIX01







- **<u>Large fill-factor</u>** design in **LF 150 nm CMOS** technology
- High resistive substrate (**>2 kOhm-cm**)
- Large **50 x 250 µm²** pixel array (**129 x 36**)
- Bunch-crossing clock frequency (**40MHz clock**)
- 40 MHz (up to **160MHz** by design) LVDS serial output
- Charge ADC sampling: **8-bit LE/TE time stamps (ToT)**
- Power: **55 µW/pixel (~1.7W/cm²)**

Radiation-hardness and sensor layout optimized in previous prototypes

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Succesful design efforts for cross-talk mitigation

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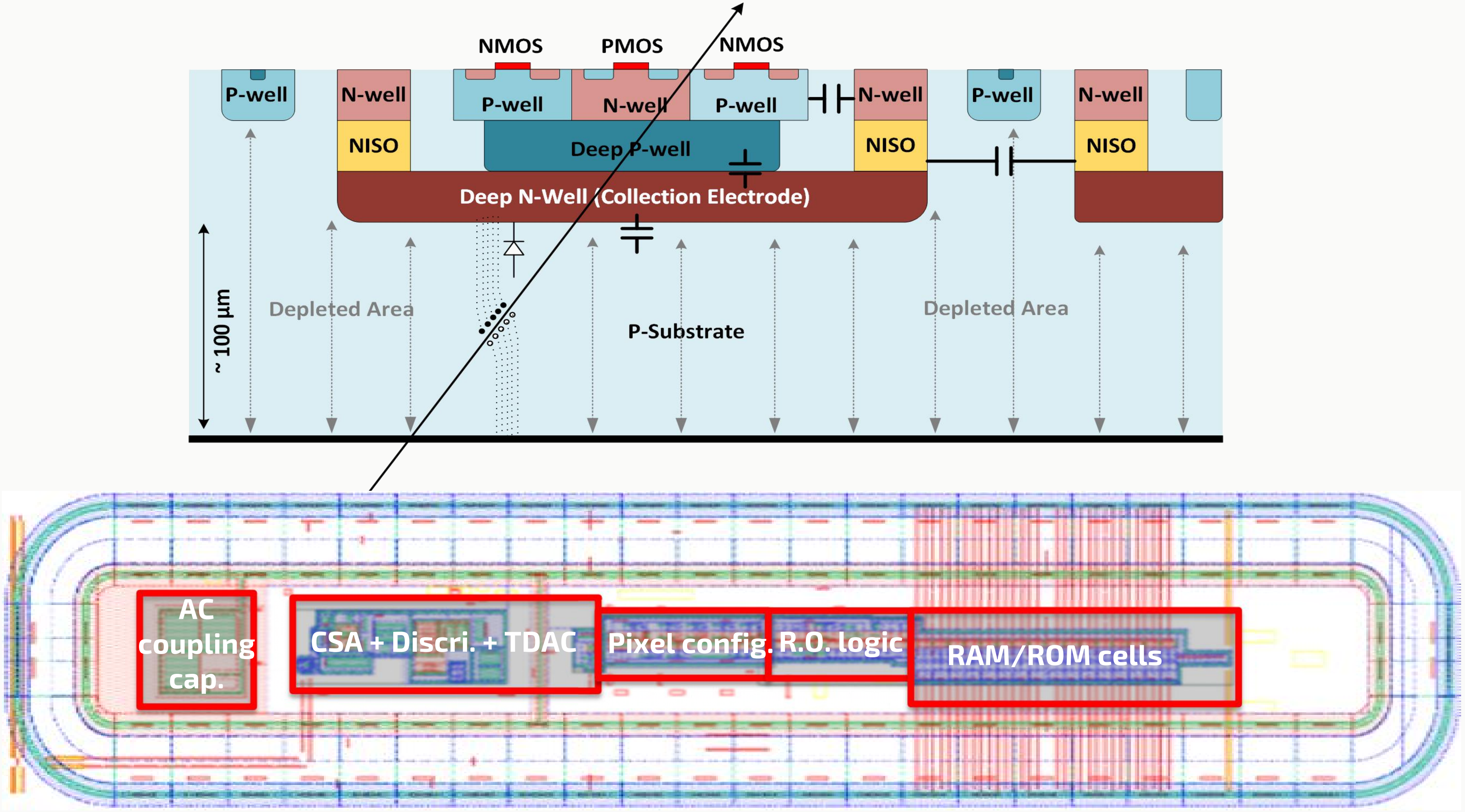
Fast and low-power CSA and discriminator implementations

☑

PIXEL LAYOUT IN LF-MONOPIX01

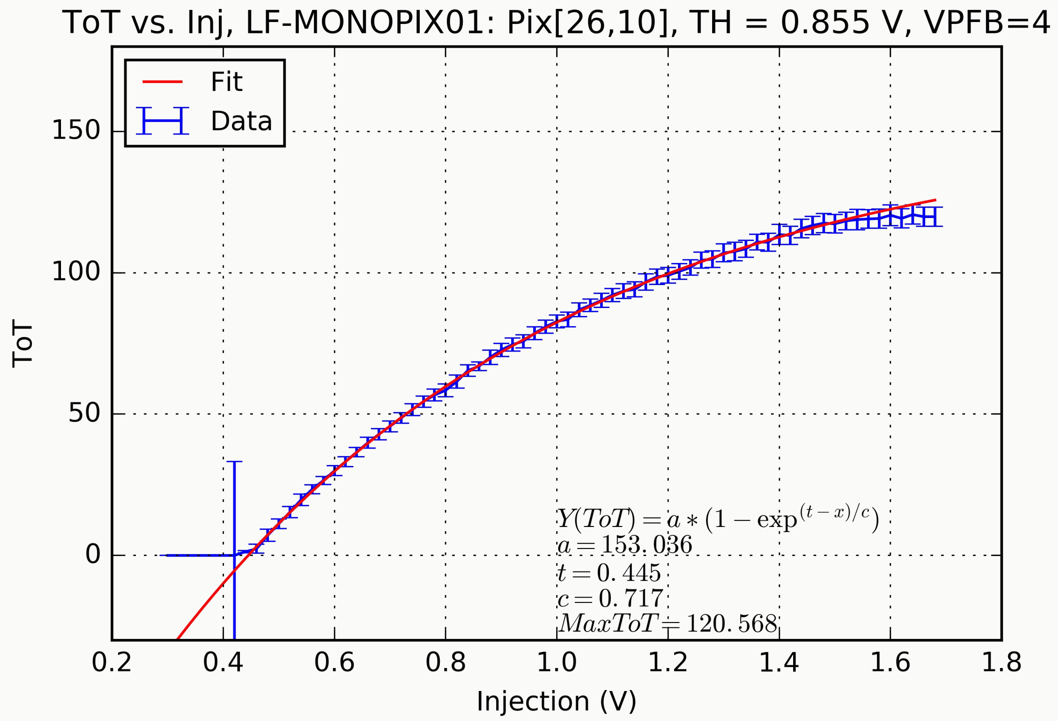


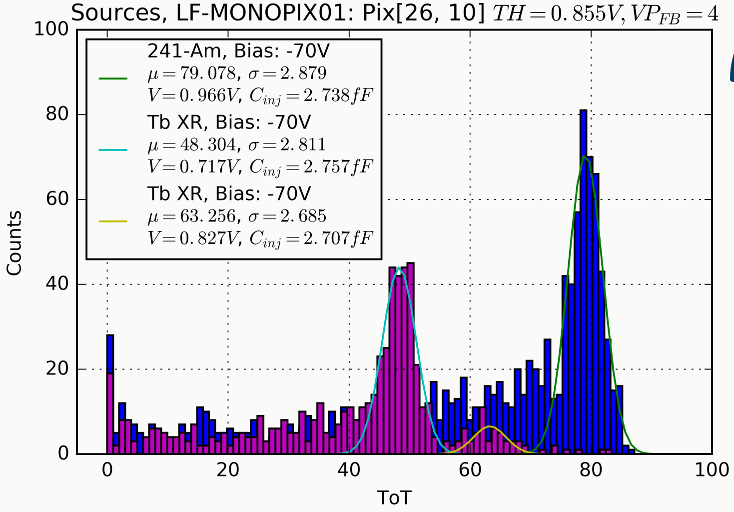
TOT RESPONSE AND INJECTION CAPACITANCE

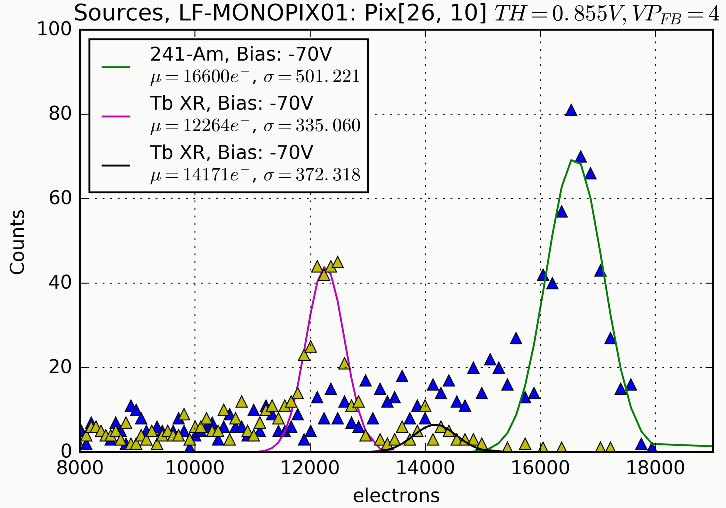
-> Injecting charge directly to the pre-amplifier.

+ Low feedback voltage (VPFB): Longer ToT

(sampling with **higher resolution**)







(Assuming 3.6 eV/e-)

^{241}Am:

16539 e-

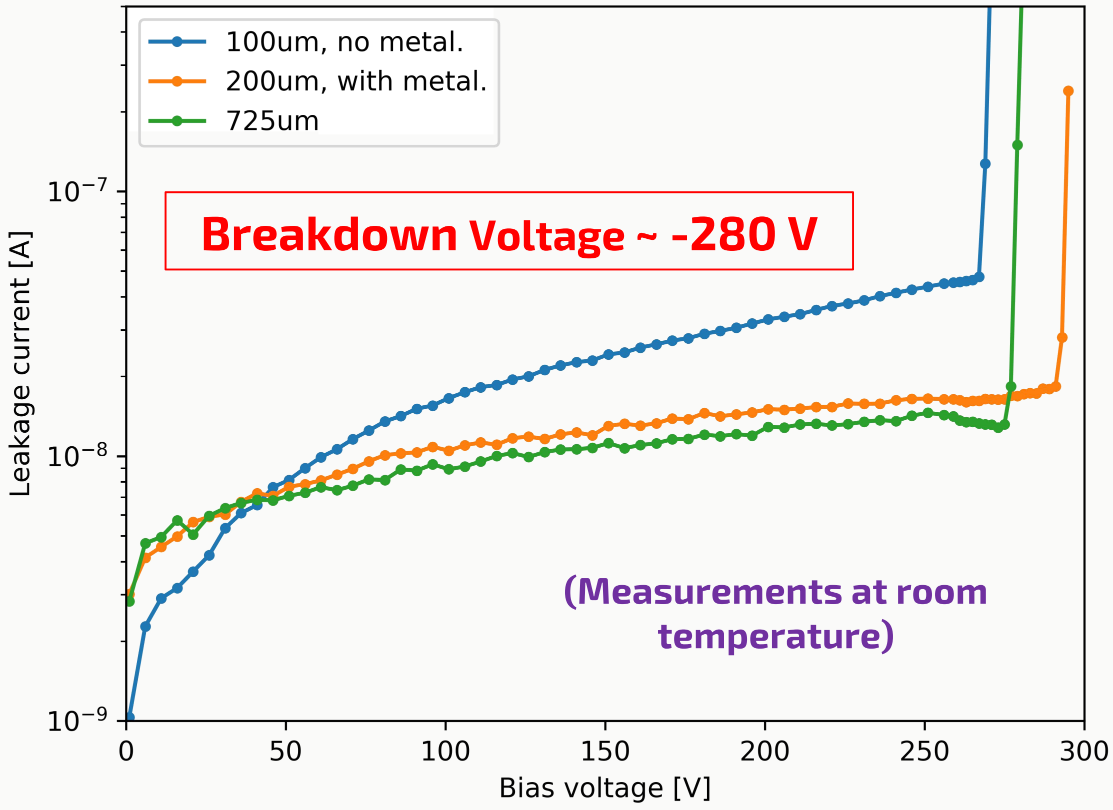
Tb X-rays:

K_α	12353 e-
K_β	13997 e-

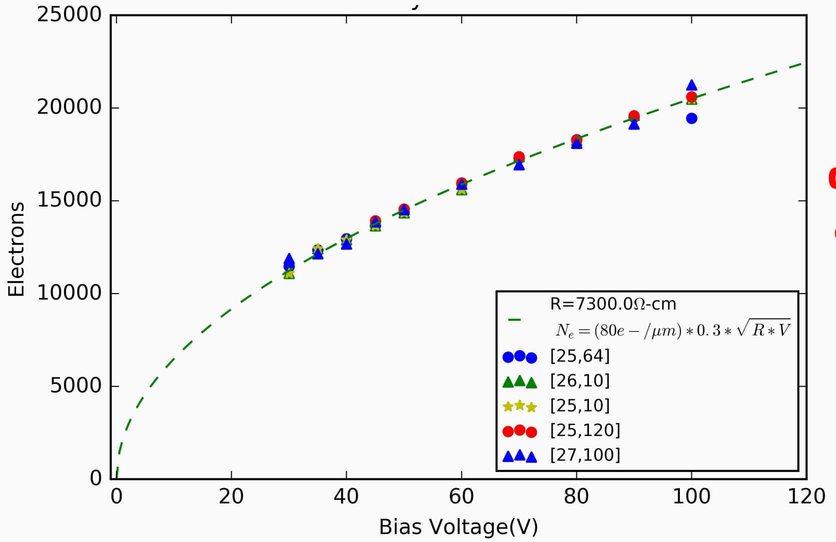
C_{inj} = Q / V ~ 2.75 fF

ToT can also be used for event differentiation or time-walk corrections.

BREAKDOWN AND DEPLETION

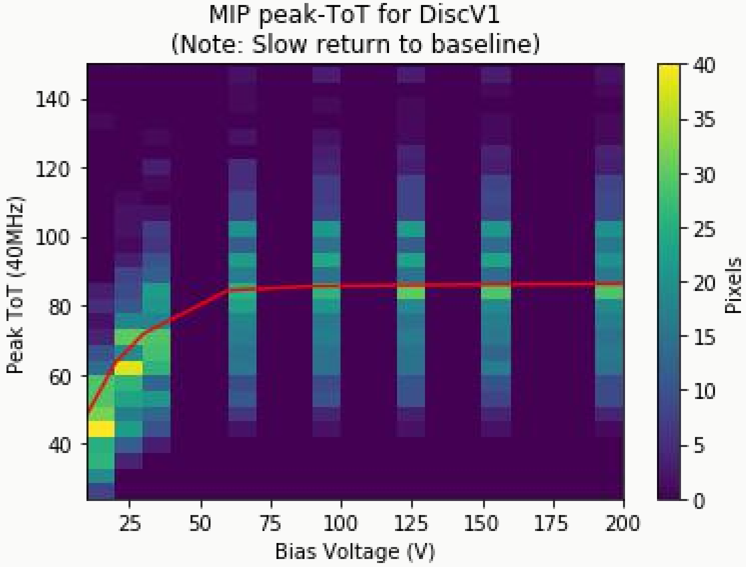


Most Probable Value for MIPs measured in LF-MONOPIX



Large collected charge (~10^4 e-) in a highly resistive (>2 kOhm-cm) substrate.

☑



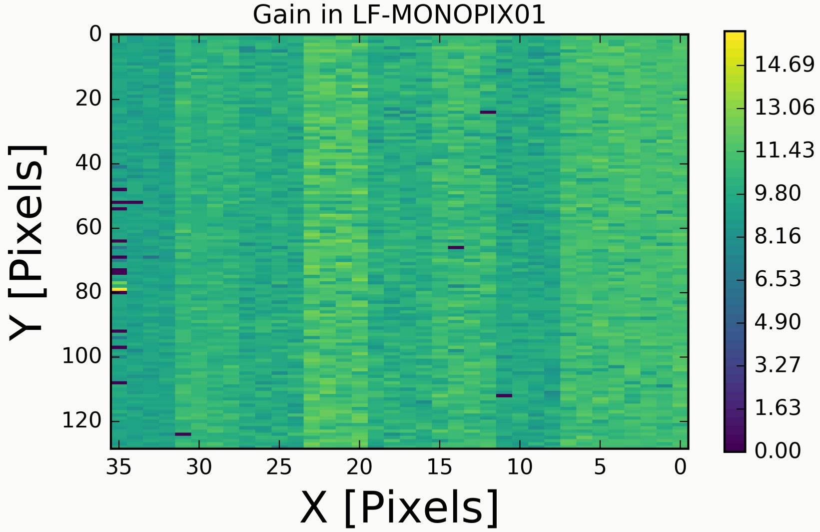
200μm thick chip fully depleted at ~60V

☑

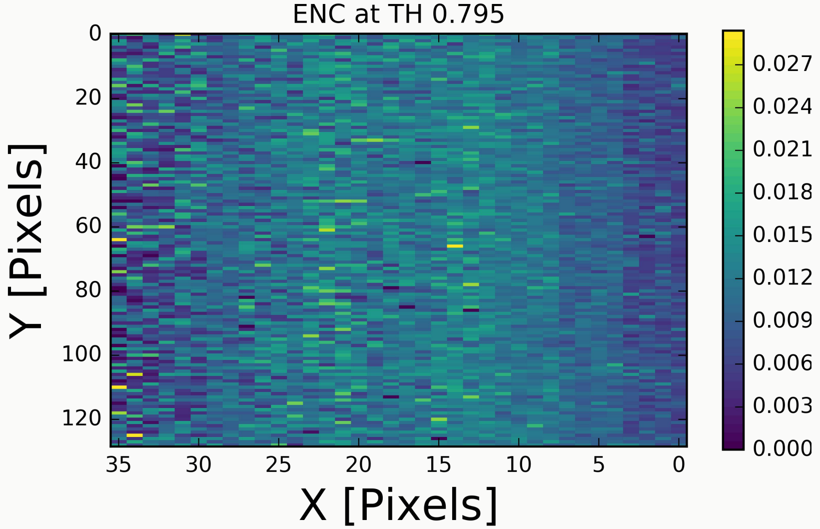
NOISE AND GAIN

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*

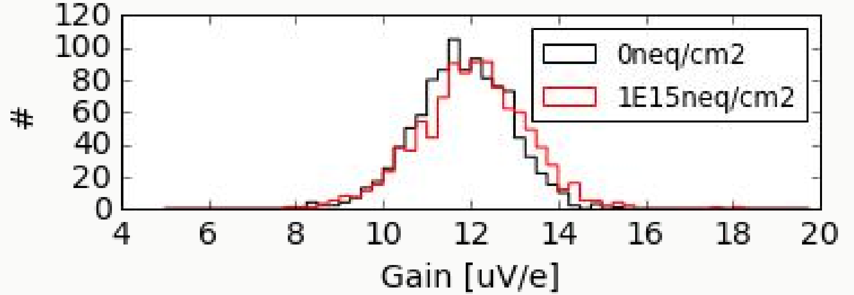
Gain within **10-12 µV/e-** (Mainly related to the discriminator version)

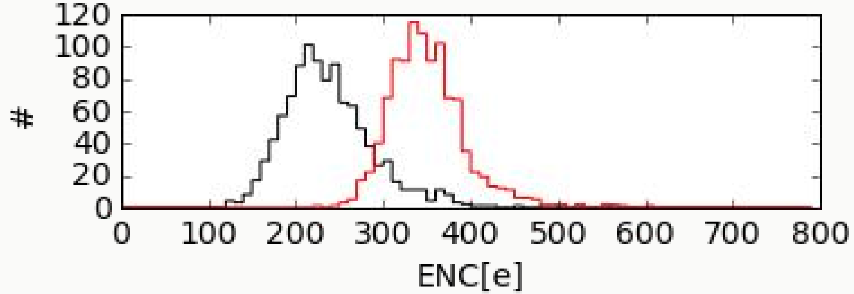


ENC within **180-240 e-,** with a dispersion between **30 to 70 e-**.



Performance after NIEL irradiation to $1x10^{15}n_{eq}/cm^2$

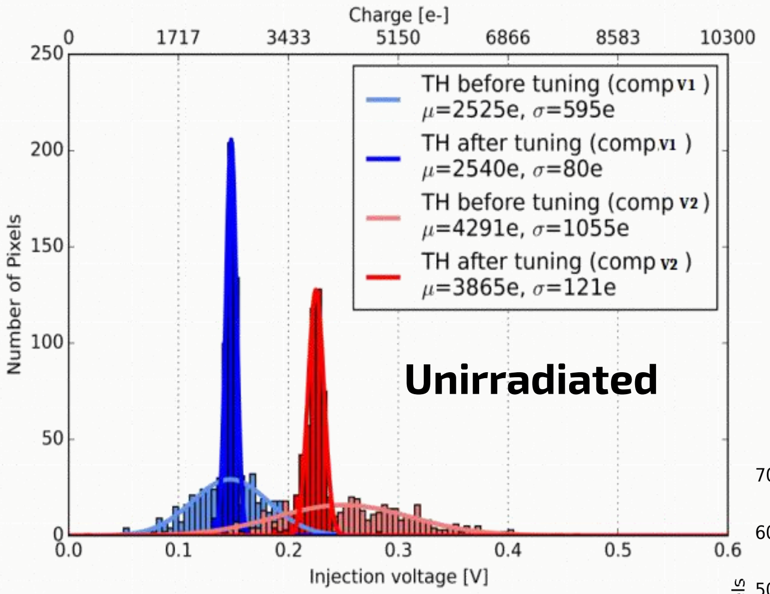




- **No loss in gain** after irradiation
- **Up to 150 e- noise increase** due to ~1 MRad TID background in JSI

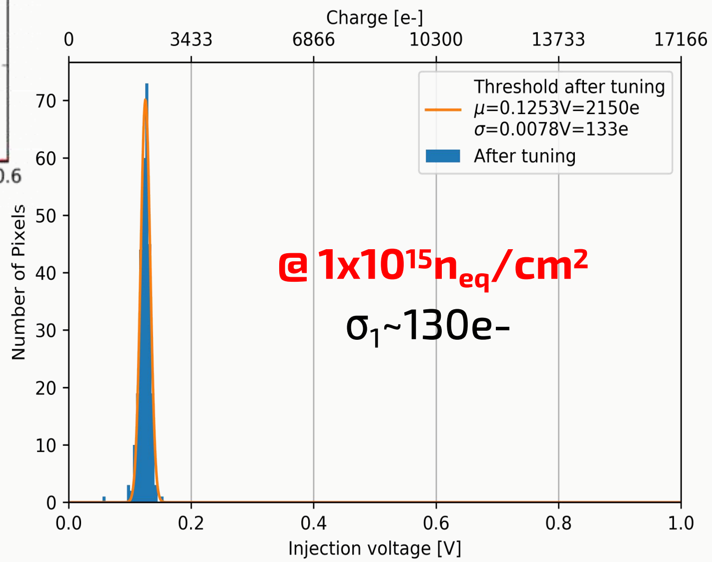
TUNING OF THRESHOLD DISTRIBUTIONS

Injection tuning: *Fix global threshold*
+ *Binary search for optimal local threshold tuning*

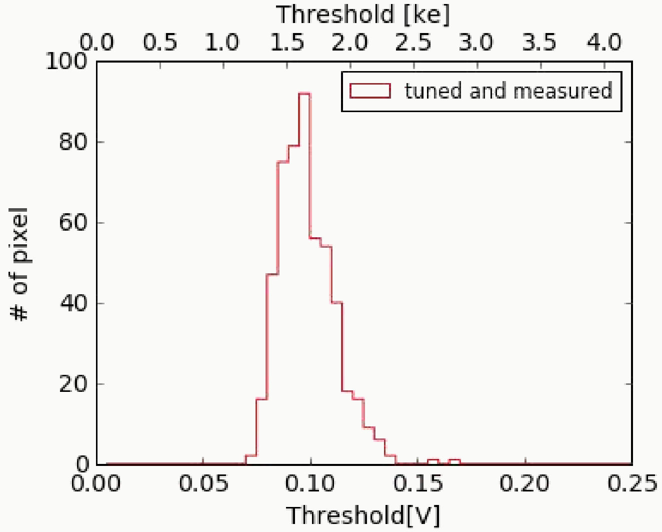


Before tuning:
$\sigma_2 >> \sigma_1$ (~600e-)
After tuning:
$\sigma 2 \sim \sigma_1$ (~100e-)

Threshold still tuneable after irradiation



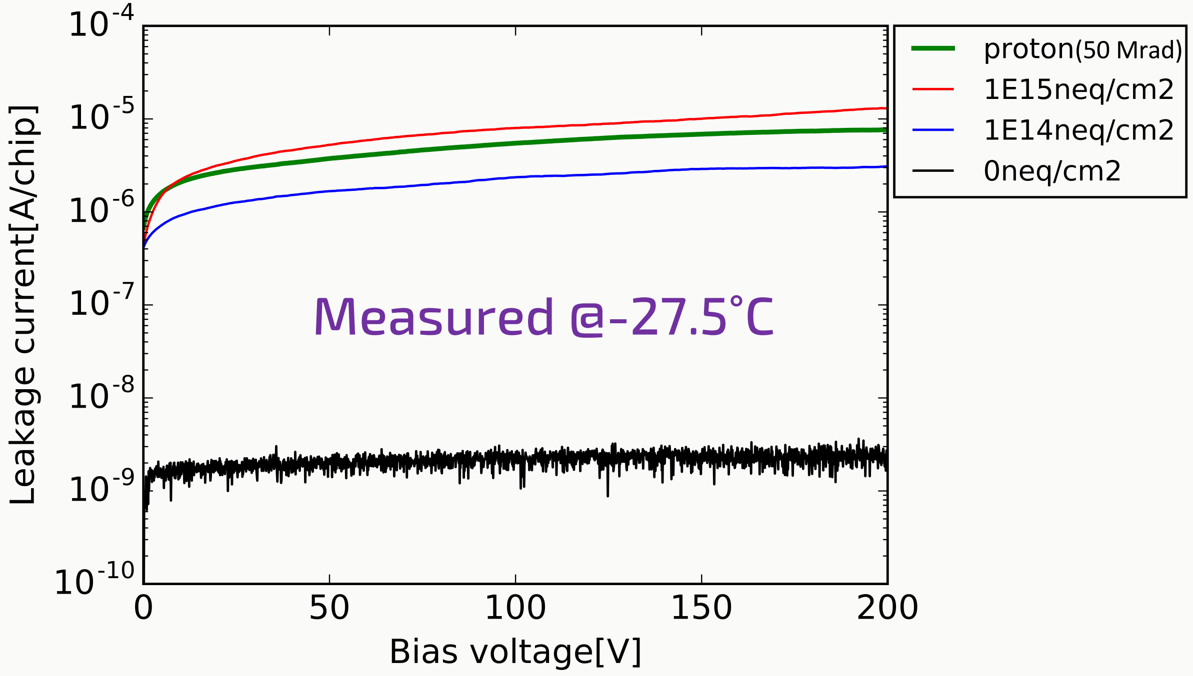
Baseline tuning: Lower global threshold close to baseline
+ *Tune local threshold according to noise hits*



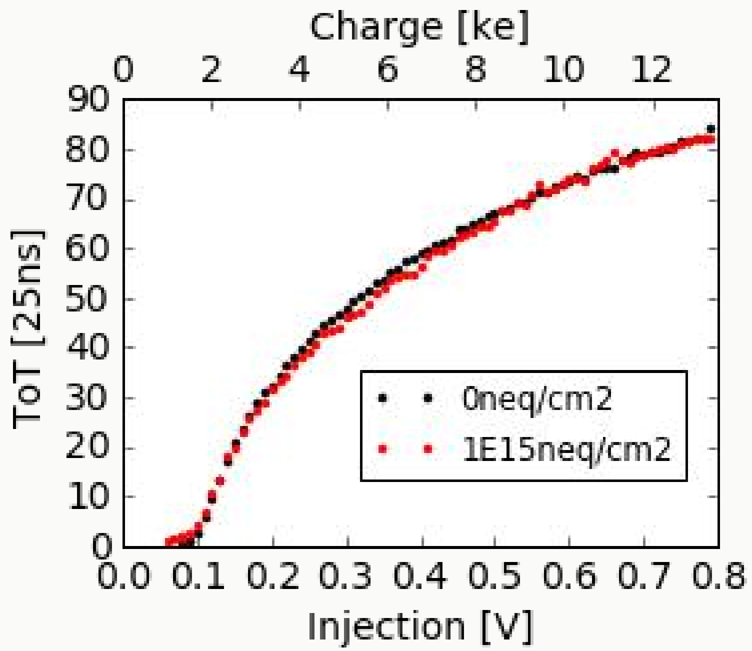
- **Threshold tunable** down to **~1400e-** (Noise occ. < 10^{-7} hits/BX)
- Tuned threshold **dispersion** **~100e-**

LEAKAGE CURRENT AND TOT RESPONSE

Leakage current



ToT response

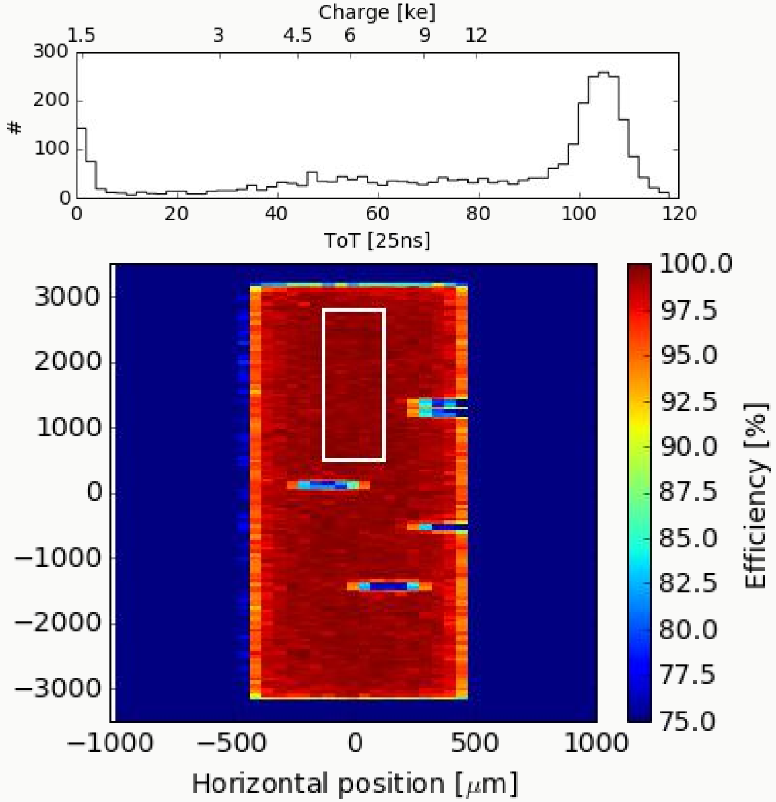


Bias: -200V @ -27.5˚C

- **Breakdown voltage still > 200V** after 1 x $10^{15} n_{eq}/cm^2$ NIEL
- **ToT response not affected**

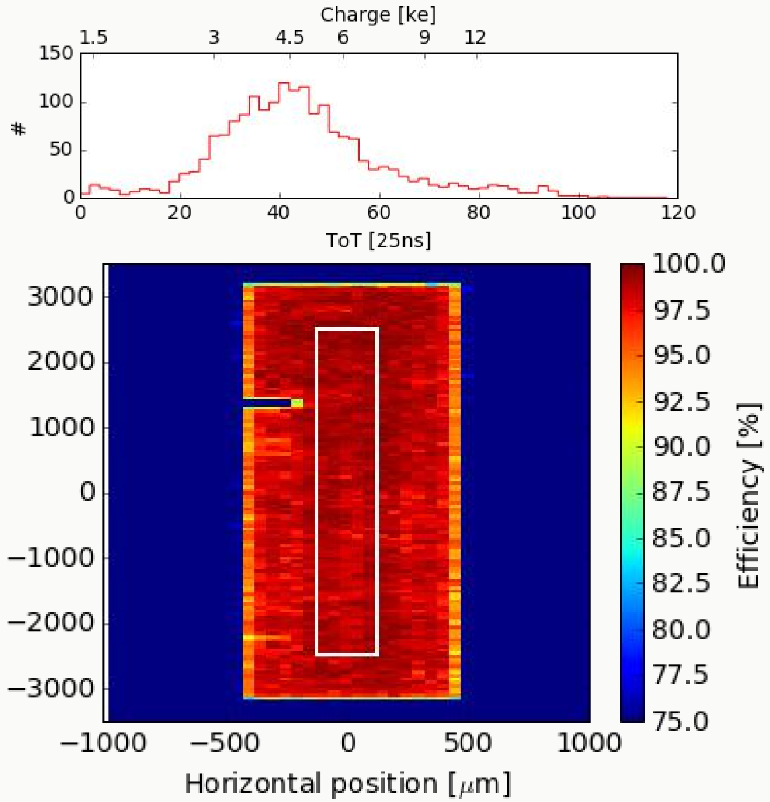
TB WITH 2.5 GEV ELECTRONS: HIT EFFICIENCY

- **Non-irradiated**
  - Hit efficiency **@ Noise occ. << 10^{-7} , TH~1700e- (<10^{-7} @ 1400e-)**
  - 1% masked pixels from noise tuning (not broken).



99.6% @ -200V

- **Neutron irradiated (1 x $10^{15} n_{eq}/cm^2$)**
  - Hit efficiency **@ Noise occ. < 10^{-8}, TH~1700e-**
  - < 0.2% masked pixels from noise tuning.
  - Efficiency loss between pixels, as expected.

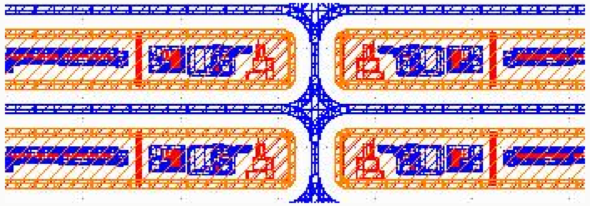


98.9% @-130V

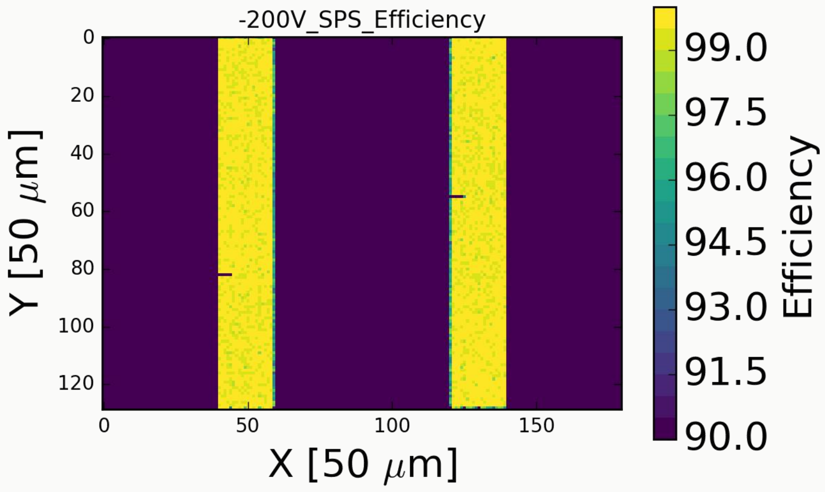
(Voltage limited due to technical issues)

TB WITH 180 GEV PIONS: IN-PIXEL EFFICIENCY

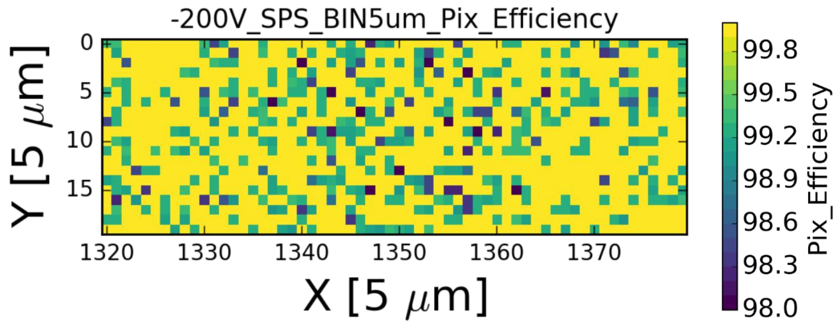
- Deep N-well (Collecting electrode…)
- P-well (Inter-pixel region, isolation of electronics…)
- N-well (R/O electronics…)



5 µm*5 µm bins

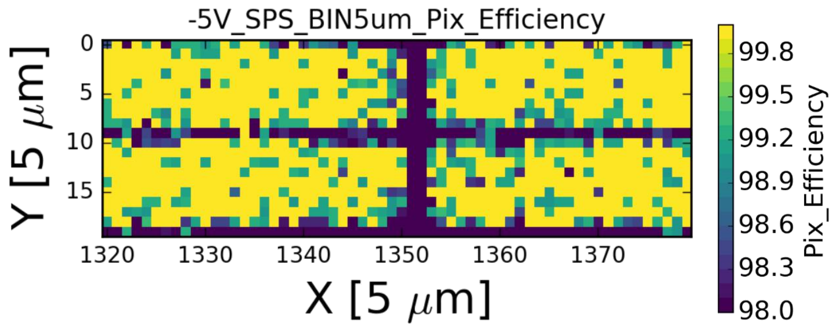


99.7% @ -200V



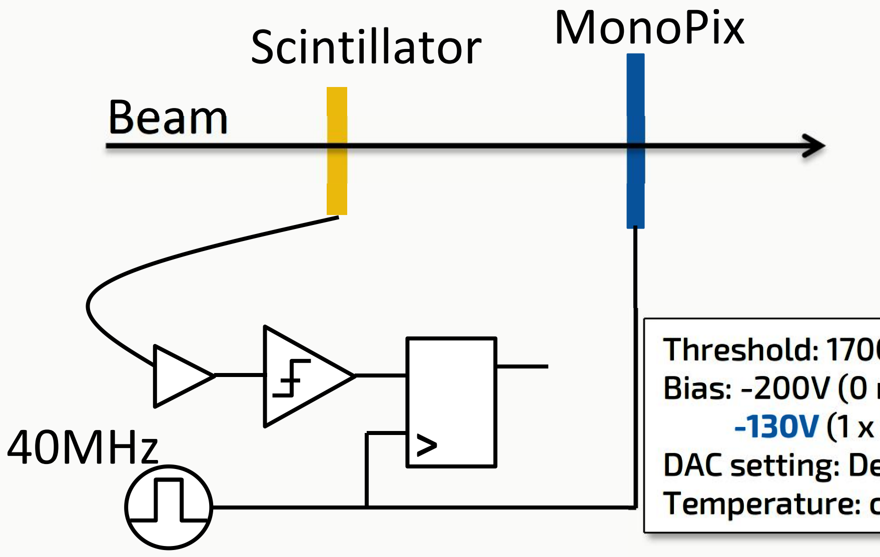
Uniform efficiency

98.8% @ -5V



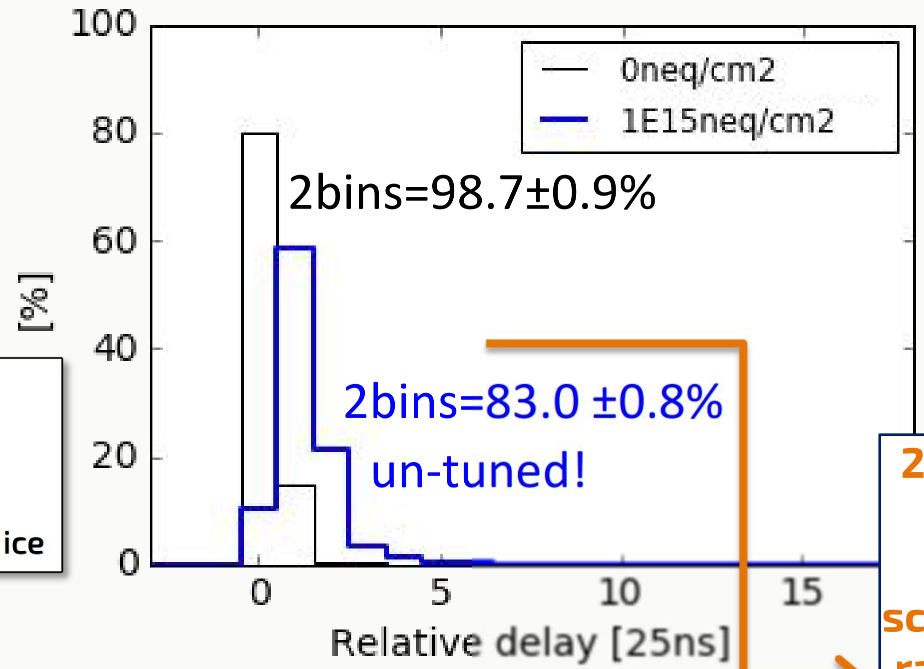
Efficiency drop only between pixels at VERY low bias V

TIMING PERFORMANCE (AT DEFAULT SETTINGS)



Threshold: 1700 e-
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
DAC setting: Default
Temperature: cooled by dry ice

Delay = (Scintillator LE) – (MonoPix LE)

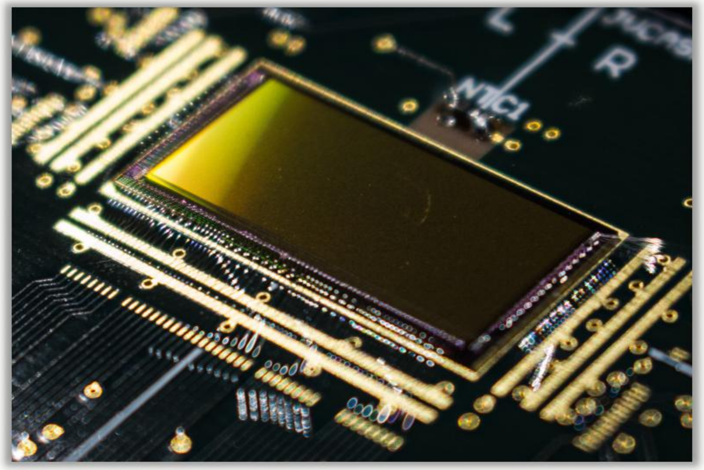


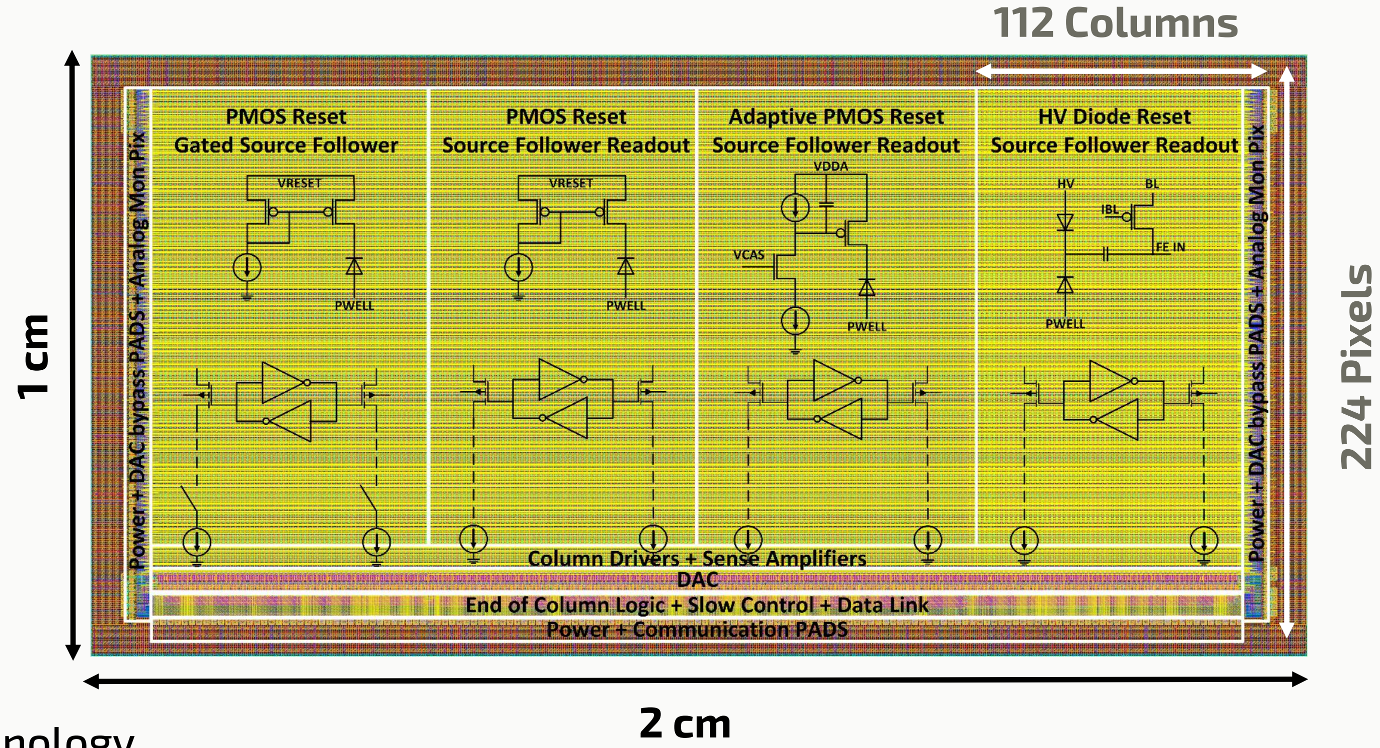
2 bins considered, as the absolute position of the scintillator signal is random relative to the clock edge

- **>80% of events are within 2 bins after neutron irradiation** up to 1 x $10^{15} n_{eq}/cm^2$.
  <u>Remarkable</u> for a C_d~400fF and promising for new designs with smaller C_d (Optimized Fill-Factor).
- **There is still room for improvement:**
  Optimization of parameters (current of CSA, discriminator, etc.), higher bias voltage, back side process.

Measurements with thinned chips and higher resolution ongoing.

TJ-MONOPIX01





- **<u>Small fill-factor</u>** design in **TJ 180 nm CMOS** technology
- Highly resistive p-epitaxial layer(**1 kOhm-cm**) with a process modification (additional n-type planar layer)
- Large **36 x 40 µm²** pixel array (**224 x 448**)
- Bunch-crossing clock frequency (**40MHz clock**)
- 40 MHz CMOS serial output per flavour
- Charge sampling: **6-bit LE/TE time stamps (ToT)**
- Power: **3 µW/pixel (~0.18 W/cm²)**

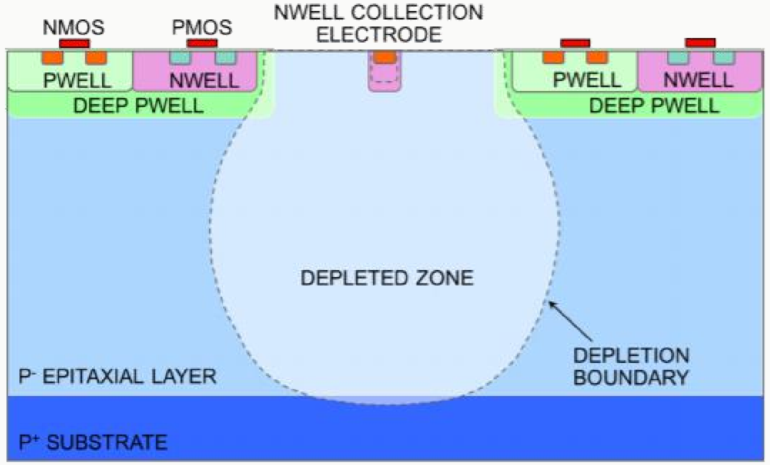
Fully integrated electronics in a small pixel volume ☑

Increased radiation tolerance with a modified process ☑

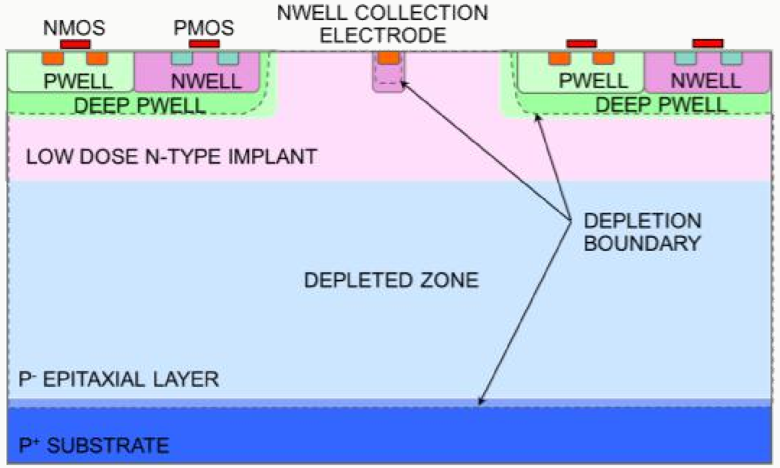
Low-noise and low-power analog front-end ☑

PROCESS MODIFICATION IN TOWERJAZZ 180NM

Standard Process



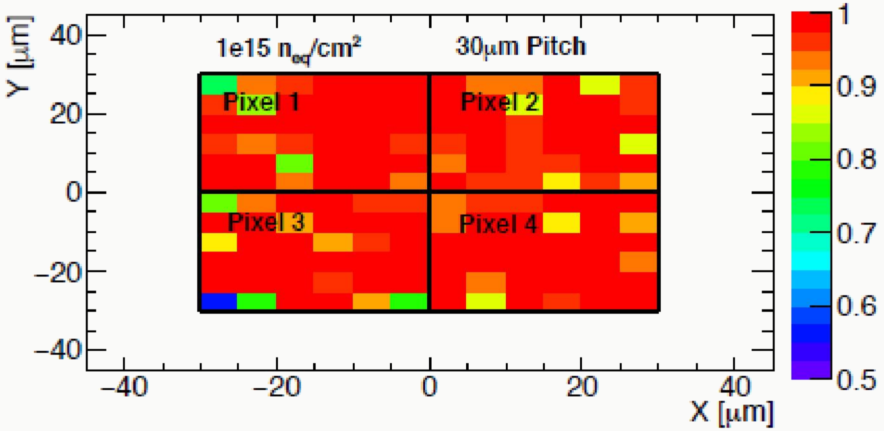
Modified Process

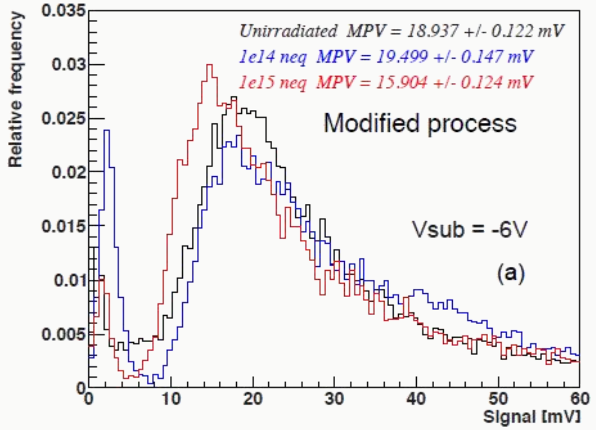


W. Snoeys et al.

DOI: 10.1016/j.nima.2017.07.046

Rad-hard modified process tested on an “Investigator” chip





97% efficiency after 1x10^{15} n$_{eq}$/cm^2

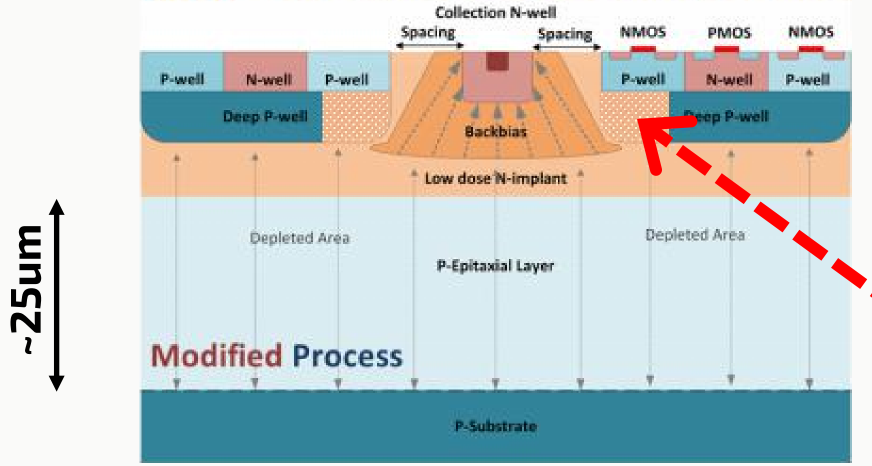
(100e- threshold, 30 µm square pixel)

H. Pernegger, et al.

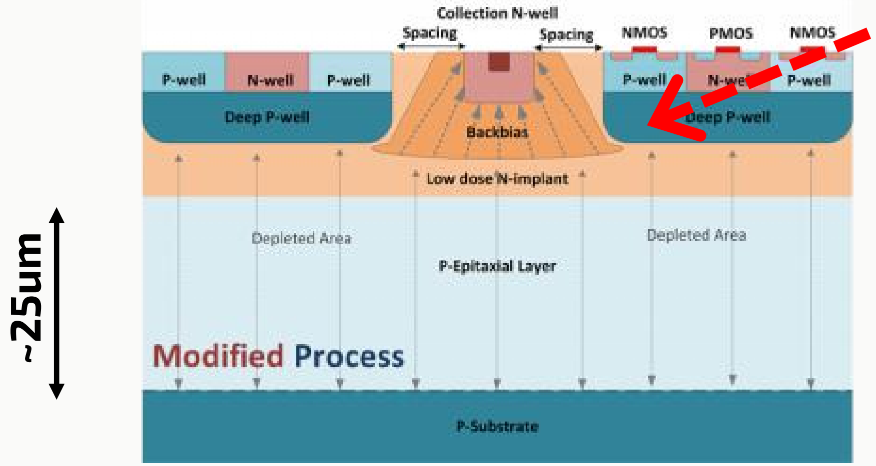
DOI: 10.1088/1748-0221/12/06/P06008

PIXEL LAYOUT AND P-WELL COVERAGE

REM DPW – top half of each column (112 pixels)

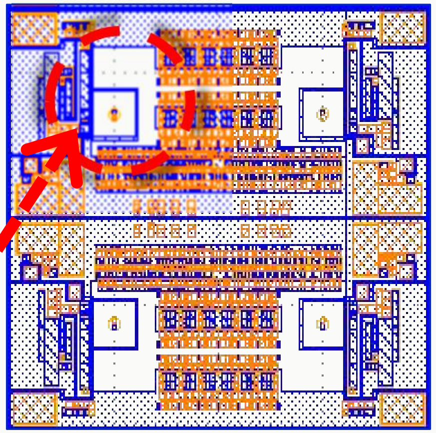


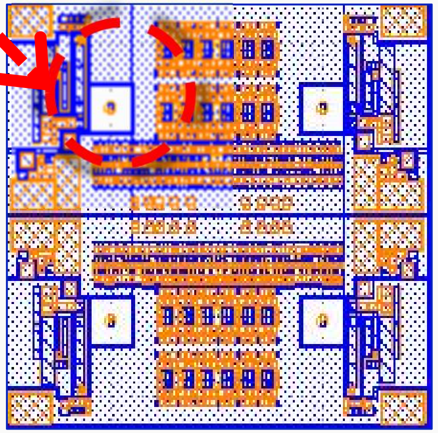
FULL DPW – bot half of each column (112 pixels)



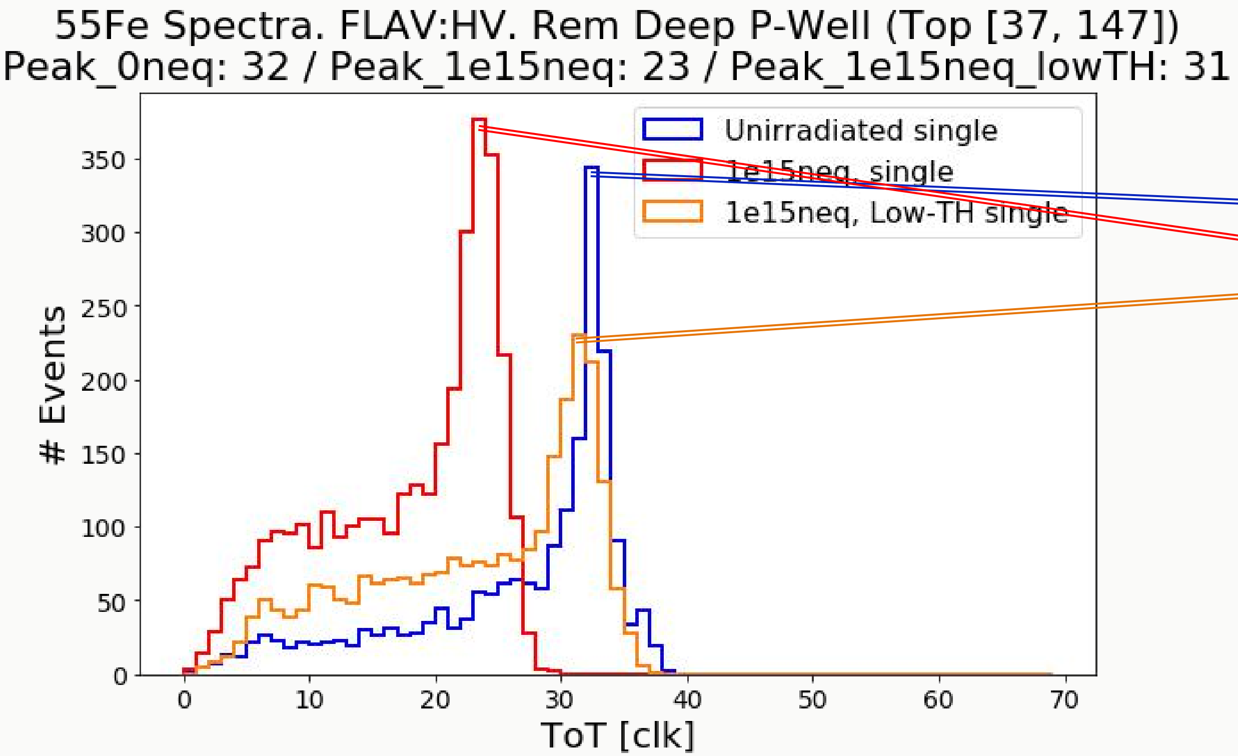
Different P-well coverage on top and bottom column regions

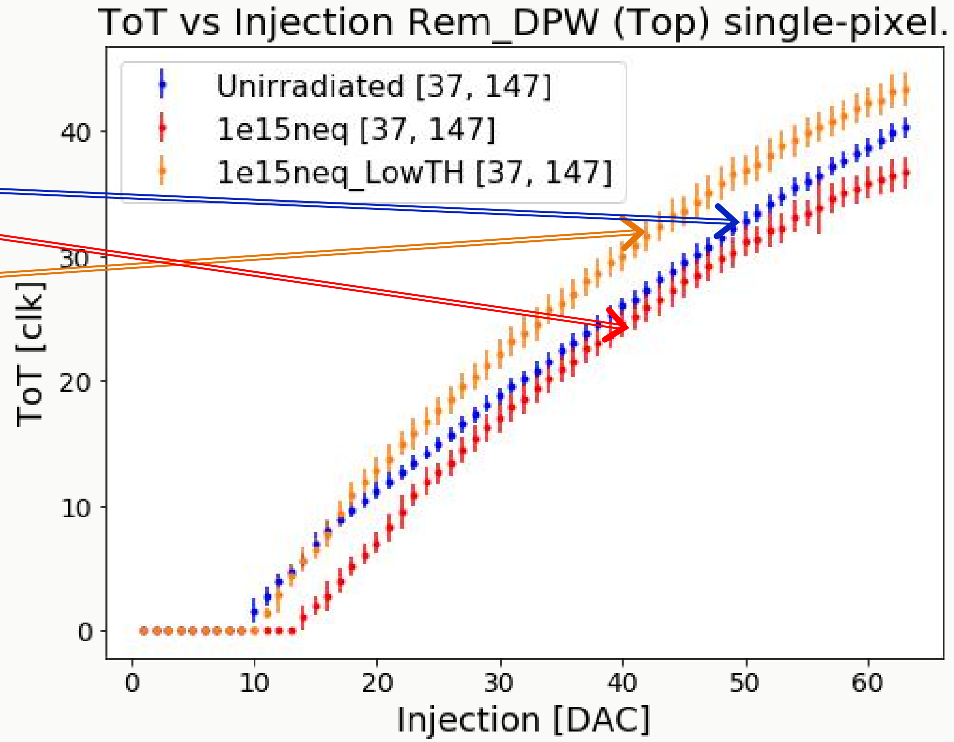
2x2 pixel array (Top view)





CALIBRATION OF THE INJECTION CIRCUIT



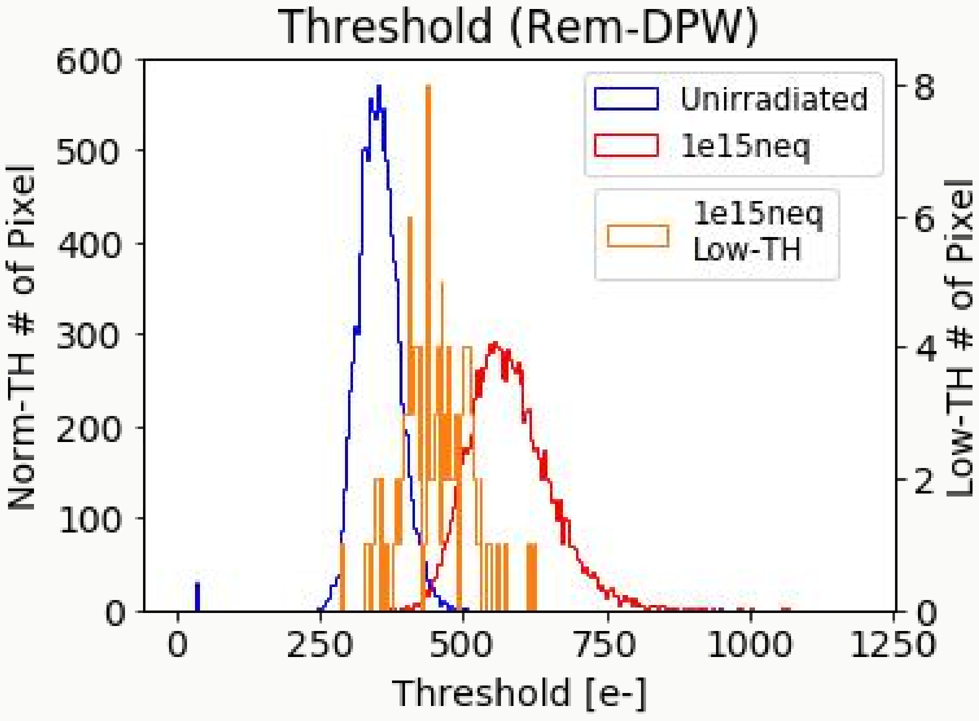


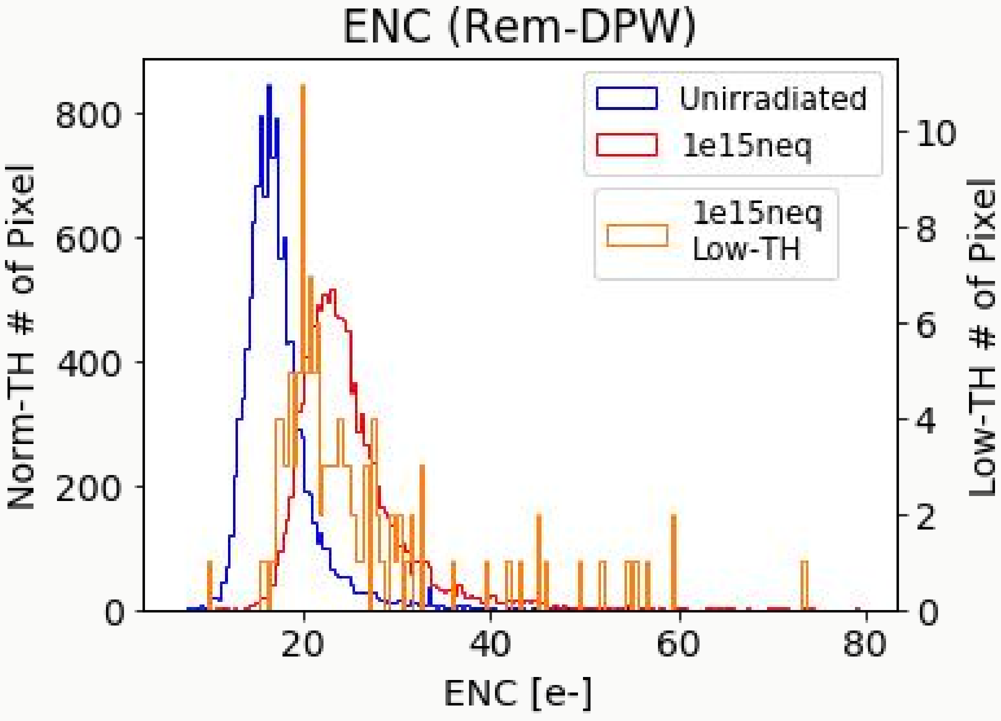
- Calibration values are similar in "Top" and "Bottom", but different for unirradiated and irradiated samples:

Unirradiated: ~33e-/DAC **$1x10^{15}$ Irradiated:** ~42e-/DAC

THRESHOLD AND NOISE

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*



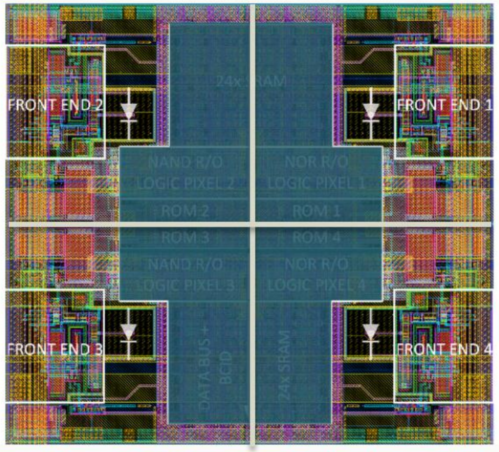


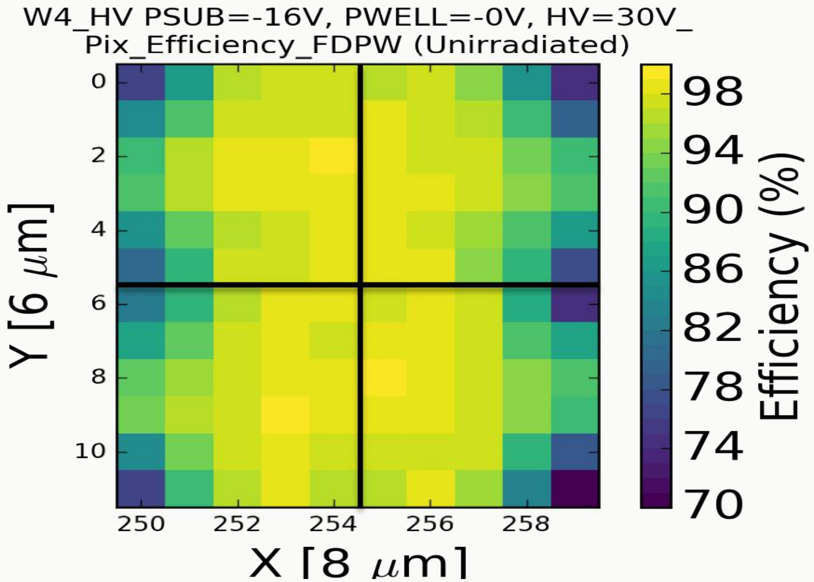
Unirradiated: μ= 349e-, σ=34e-
$1x10^{15}$ Irradiated: μ= 569e-, σ=66e-

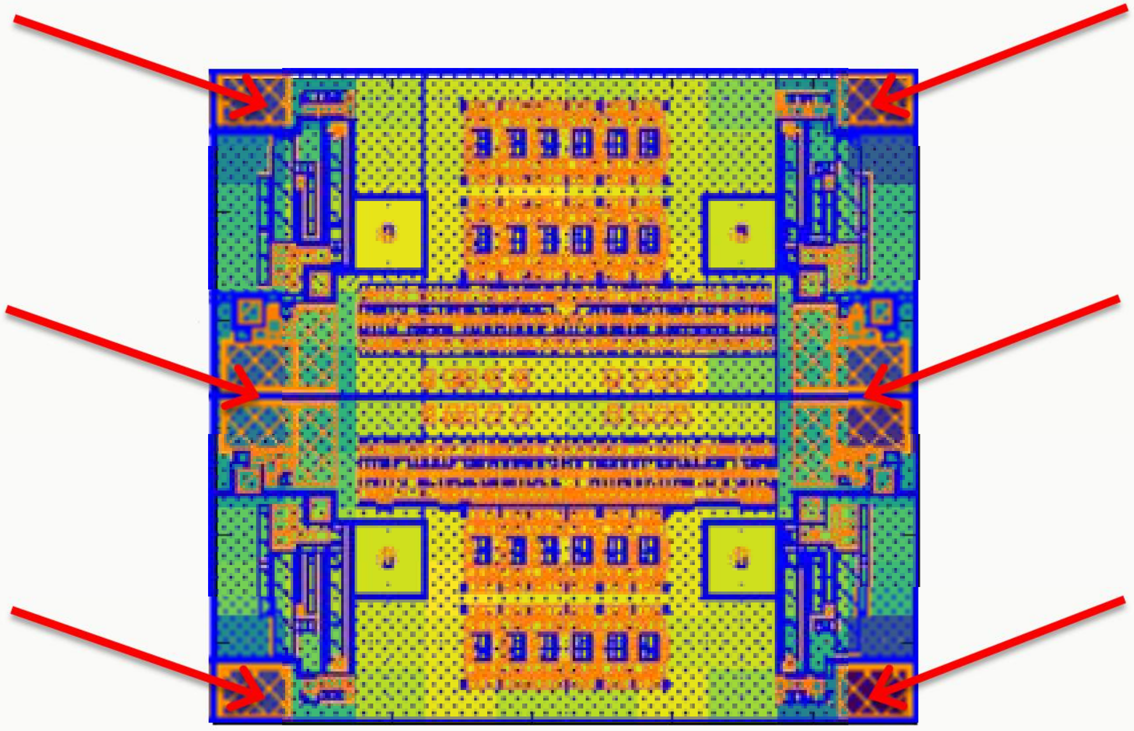
ENC increased by ~10e- after $1x10^{15}$ n_{eq}/cm^2
(Probably due to TID bckg)

IN-PIXEL EFFICIENCY (UNIRRADIATED)

2x2 Pixel Array







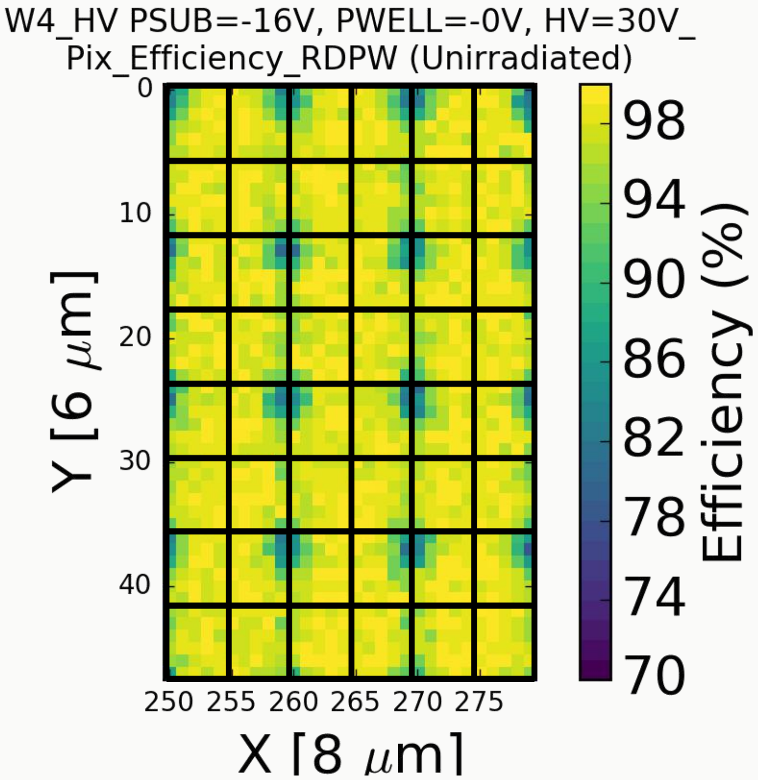
Low efficiency "corners" correlated with **large active areas** used for decoupling capacitors

---> Design layout to be optimized in future designs

MEAN HIT EFFICIENCY VS DEEP P-WELL COVERAGE

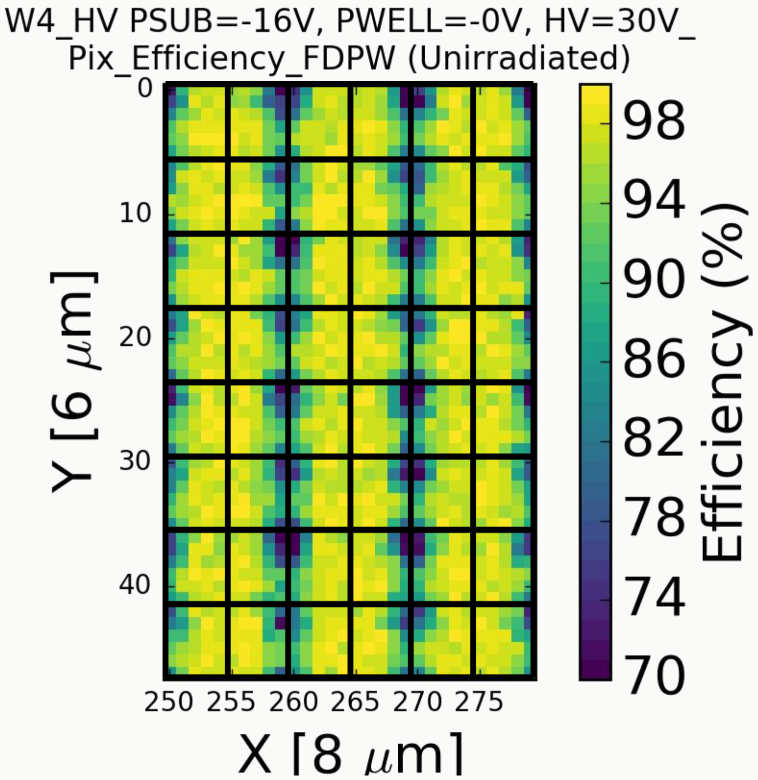
Removed Deep P-Well Coverage

97.1%



Full Deep P-Well Coverage

93.7%



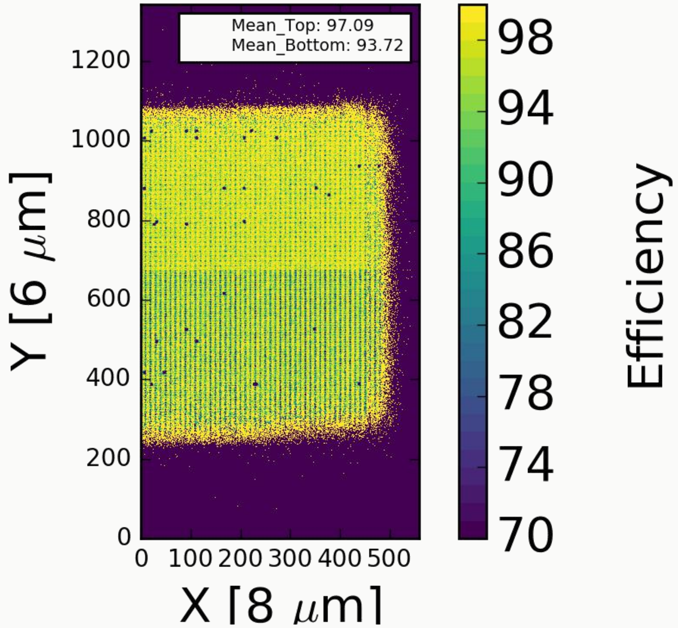
- Lower efficiencies in Full DP-Well regions (Bottom) than in Removed DP-Well (Top) ones.

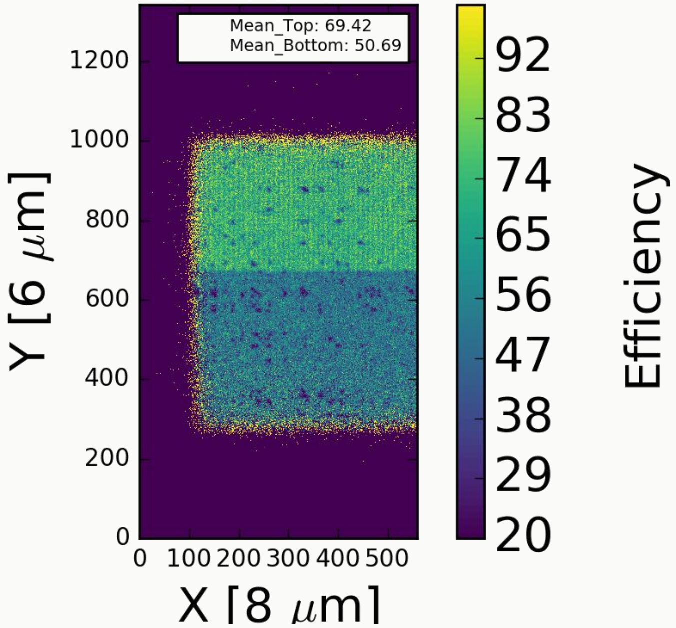
MEAN HIT EFFICIENCY AFTER IRRADIATION

UNIRRADIATED | **$1x10^{15}\,n_{eq}/cm^2$**

R-DPW

F-DPW



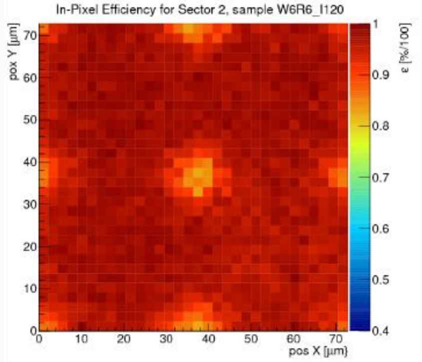


Large efficiency drop (30-50%) after $1x10^{15}\,n_{eq}/cm^2$ neutron irradiation.

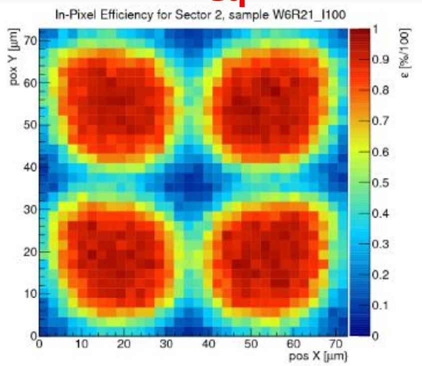
In MALTA

(very similar front-end and pixel pitch)

UNIRRADIATED



$5x10^{14}\,n_{eq}/cm^2$



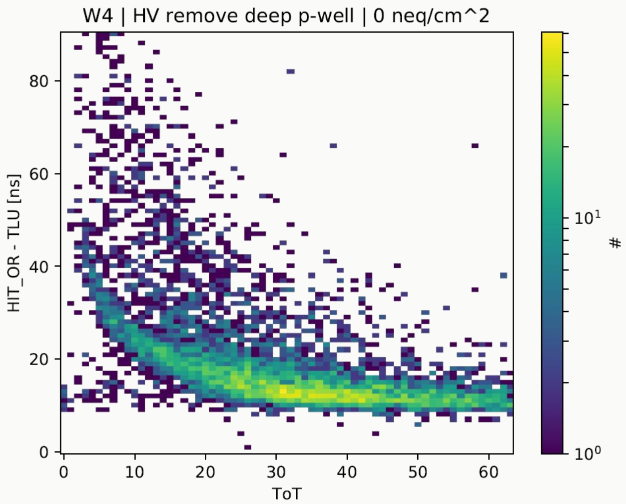
R. Cardella's presentation
(PIXEL 2018 / Talk 55)

---> Fixes to the TJ modified process in pixel corners to enhance E-Field (M. Munker, PIXEL 2018 / Talk 53)

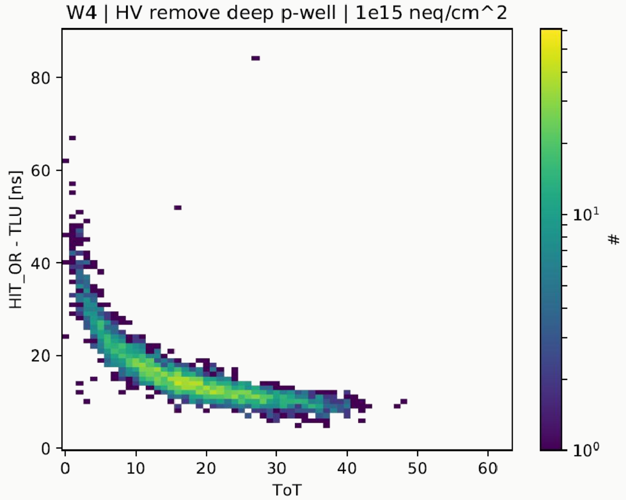
TIMING PERFORMANCE

HIT_OR -Trig vs ToT

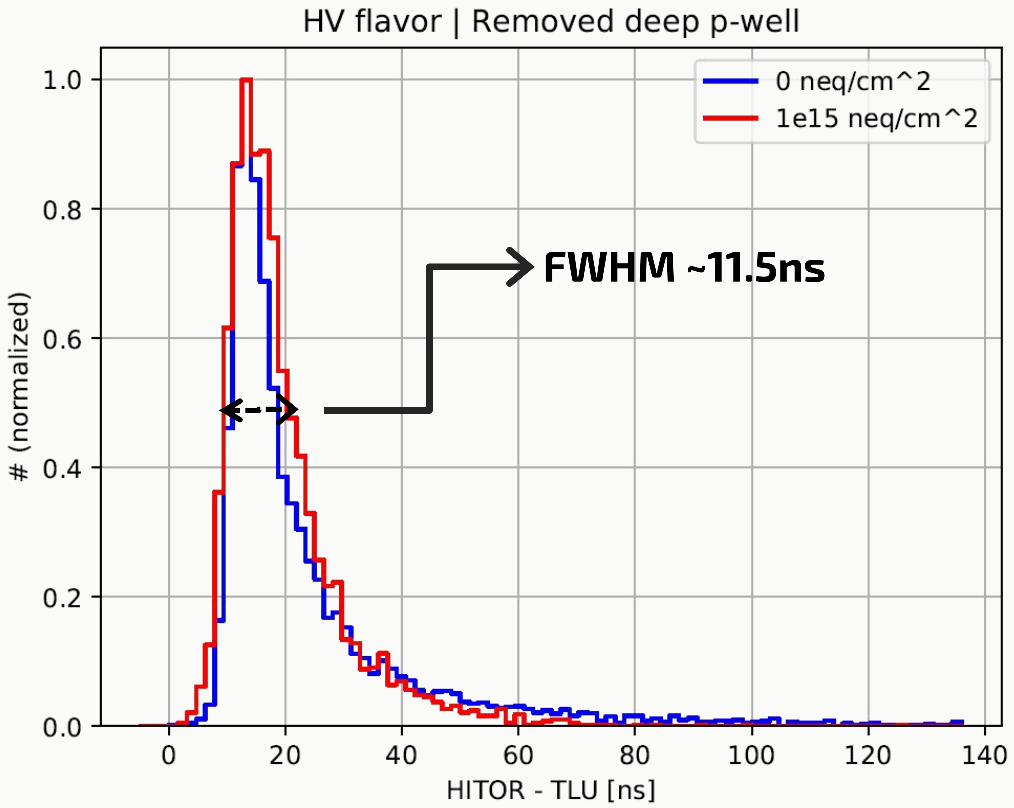
Unirradiated



$1\mathrm{x}10^{15}\,n_{eq}/cm^2$



Distributions of "HIT_OR signal - External trigger timestamp" in seed pixels from test beam (640 MHz sampling)



93% | 98% (hits within 50 ns)

CONCLUSIONS

Operational column-drain read-out on fully monolithic CMOS pixel detectors in both small and large fill factor designs on a large pixel matrix

	LF-MONOPIX01		TJ-MONOPIX01	
DMAPS type	*Large FF (150nm CMOS | LFoundry)*		*Small FF (180nm CMOS, mod. | Towerjazz)*	
	Non-Irrad	$10^{15} n_{eq}/cm^2$	Non-Irrad	$10^{15} n_{eq}/cm^2$
Signal MPV	~16ke- (@60V)	~5.6ke (@200V)	~1.6ke-	~1.4ke-
ENC	~200±50e	~350±50e	~15±2e	~25±3e
Threshold	>1400±100e	>1700e±130e	>350e±35e	>570e±65e
Mean Effic.	99.6%	98.9%	97.1%	69.4%
Hits in 50ns	98.7% (*)	83% (*)	93%	98%

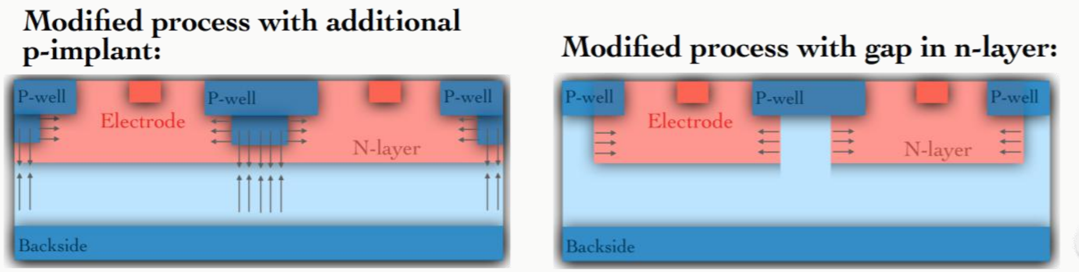
(*) Still r

WHAT'S NEXT?

- **LF-MONOPIX02 (end 2019)**
  - Next iteration with CSA and discriminators with the best performance.
  - Smaller pixel size (150x50) to reduce detector capacitance.

	LF-Monopix02	RD53 outer layer
Pixel size	50 × 150 µm²	50 × 50 µm²
Analog power	16 - 20 µA/pixel	3 - 4 µA/pixel
Digital power	4 - 5 µA/pixel	2 - 3 µA/pixel
In-time thres.	1500 - 2000 e-	1500 e-
Min. detectable charge	1000 - 1500 e-	1000 e-

- **TJ-MONOPIX02 (end 2019)**
  - Pixel layout according to the best performing fix to the TJ modified process in miniMALTA.
  - Threshold tuning and reduction.
  - Optimize active area layout in pixels.



M. Munkers's presentation
(PIXEL 2018 / Talk 53)

- **CMOS-1 (mid-2020)**

  RD-53 like, full size chip in a selected CMOS process and fill-factor approach.

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STREAM

European Commission

Thank you for your attention.

Q&A Time!

This research project received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

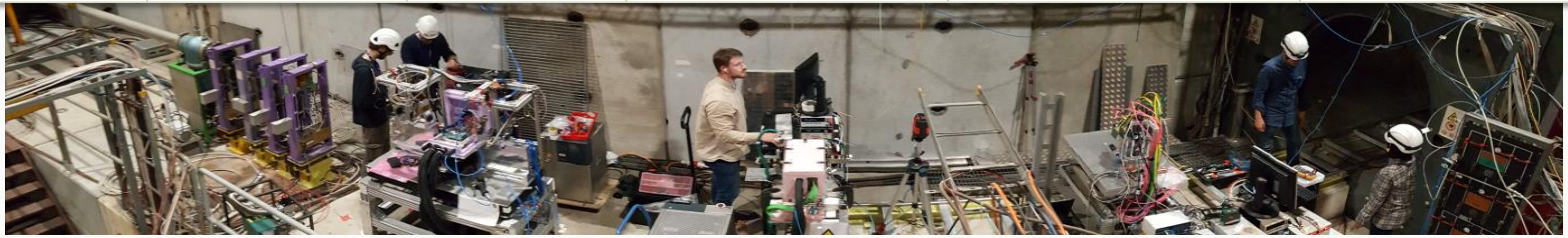
Moreover, it has been supported by a Marie Skłodowska-Curie Innovative Training Network Fellowship of the European Union's Horizon 2020 Research and Innovation Programme under grant agreement 675587-STREAM.

CMOS DEMONSTRATOR PROGRAM

A collaborative R&D effort within ATLAS focused on DMAPS prototypes with fast read-out architectures in different CMOS processes.

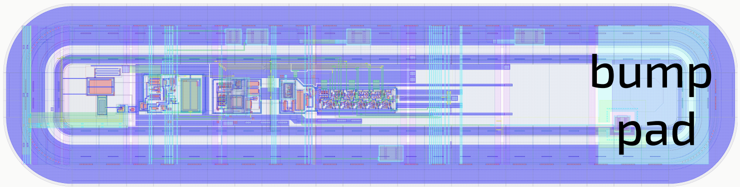
Previous iterations of these prototypes (passive sensors, or active ones with a first stage of the Front-End within the pixel) allowed to optimize the designs and improve radiation-hardness.

Chip name	Technology	Fill factor	Pixel size [μm²]	R/O architecture	Status
ATLASpix	Foundry 1 180nm	Large	56 x 56	Asynchronous	Measurements
MALTA	Foundry 2 180nm	Small	36 x 36	Asynchronous	Measurements
TJ Monopix		Small	36 x 40	Synchronous	
Coolpix		Large	50 x 250	Synchronous	
LF Monopix	Foundry 3 150 nm	Large	50 x 250	Synchronous	Measurements
LF2		Large	50 x 50	Synchronous	



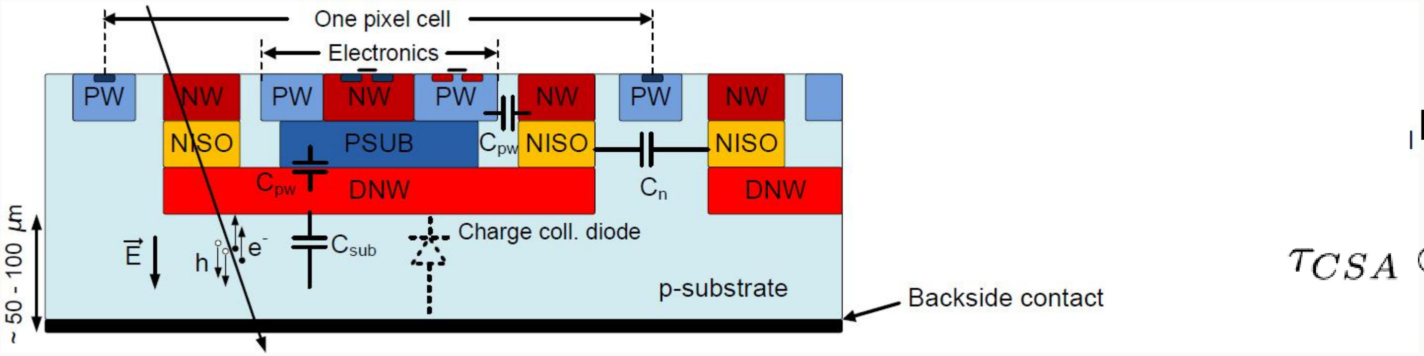
FROM LF-CPIX TO LF-MONOPIX

LF-CPIX Demonstrator (50 x 250 μm²)



LF-MONOPIX01 (50 x 250 μm²)

Large fill factor design. C_d~ **400fF**



An increase in detector capacitance has implications on **timing** and **noise**

$$\tau_{CSA} \propto \frac{1}{g_m} \frac{C_d}{C_f} \qquad ENC^2_{thermal} \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_d^2}{\tau}$$

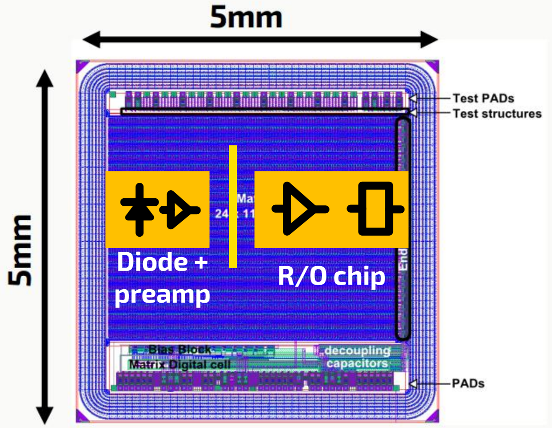
Electronics are directly coupled to the collecting node through C_{pw}

- Special efforts on design to minimize cross-talk with digital signals
- Increase of minimum operational threshold

PROTOTYPE DEVELOPMENT LINE

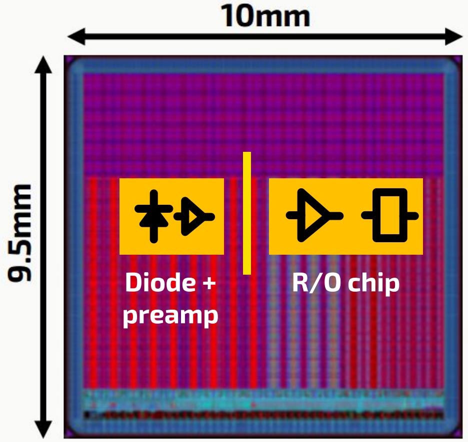
CCPD_LF

- Subm. in Sep. 2014
- 33 x 125 µm² pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test



LF-CPIX (DEMO)

- Subm. in Mar. 2016
- **CPIX Demonstrator in LF**
- 50 x 250 µm² pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test



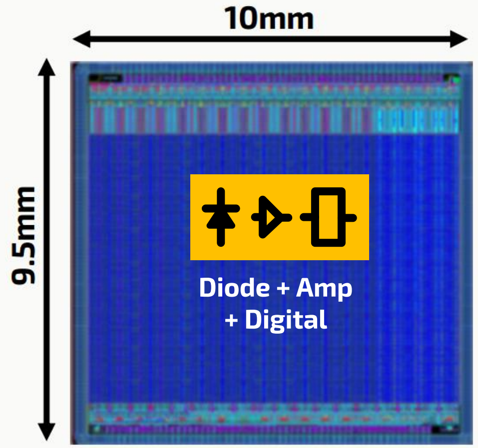
Irradiated without substantial performance loss

LF-MONOPIX01 (Monolithic)

- Subm. in Aug. 2016

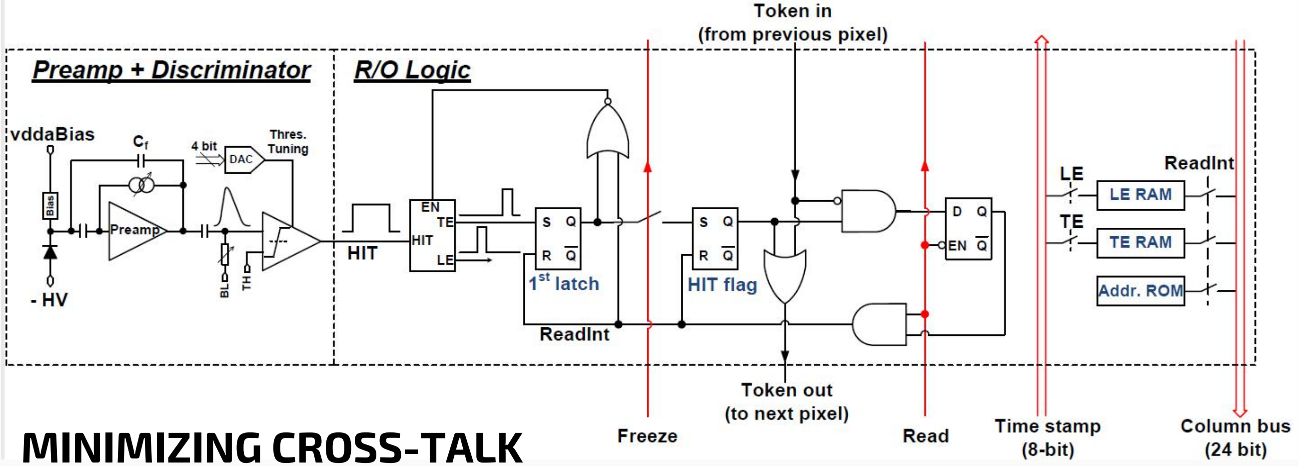
(Back: End of Mar. 2017)

- "Demonstrator size"
- 50 x 250 µm² pixels
- 150 nm CMOS
- **Fast (Col. Drain) standalone R/O**

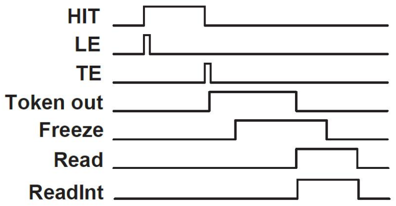


Fully integrated Speed and digital R/O

DESIGN CHALLENGES



Column-drain R/O logic

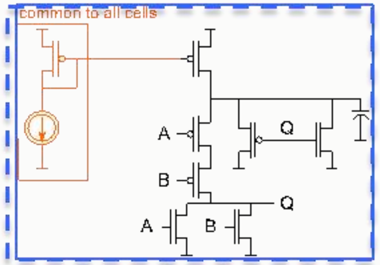


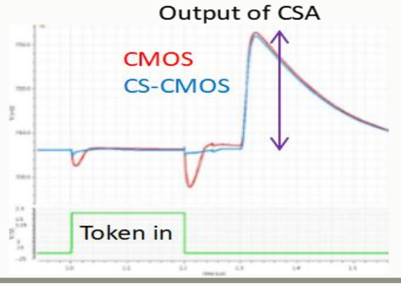
8-bit LE/TE time-stamps (ToT) + Address

MINIMIZING CROSS-TALK

In Token propagation:

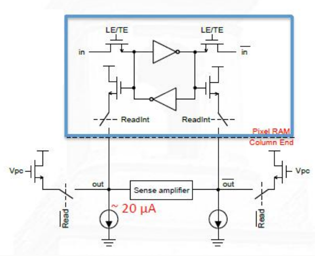
“Current steering logic”
-> Limit the current to avoid glitches

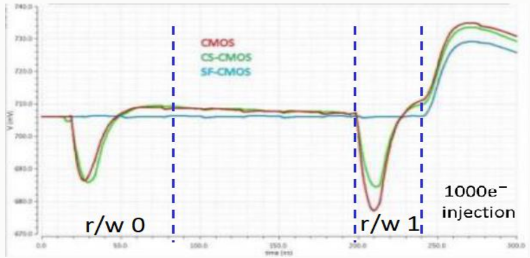




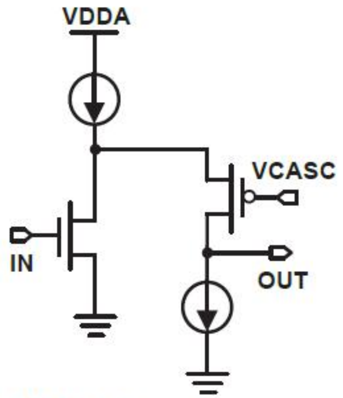
In Data R/O (LE/TE, address):

Differential lines + Source followers
-> Avoids current injection into the PW when switching from high to low





PREAMPLIFIERS AND DISCRIMINATORS



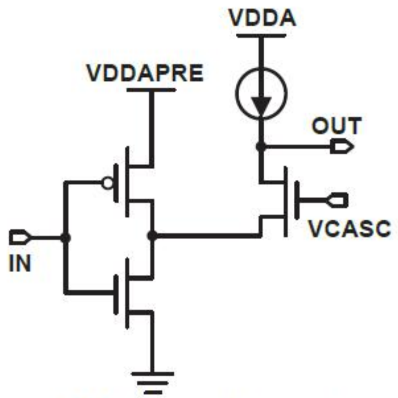
NMOS input pre-amp.

Bias I ~ 17 µA

Peak time ~20 ns (4ke- signal)

ENC (Simulation) ~ 170 e-

Faster



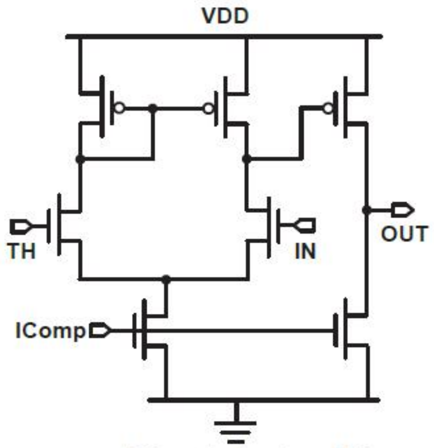
CMOS input pre-amp.

Bias I ~ 15 µA

Peak time ~25 ns (4ke- signal)

ENC (Simulation)~ 135 e-

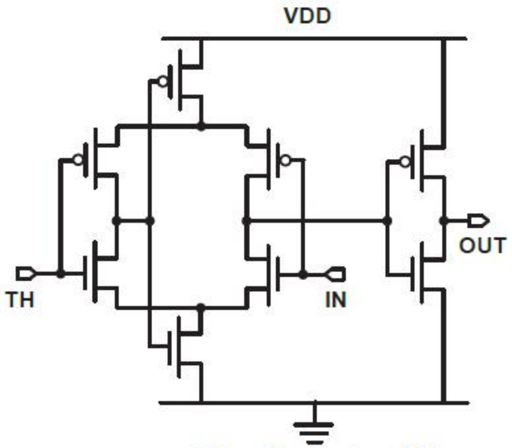
(Analog power from periphery)



Discriminator V1

Bias I ~ 4.5 µA

Two-stage open loop structure

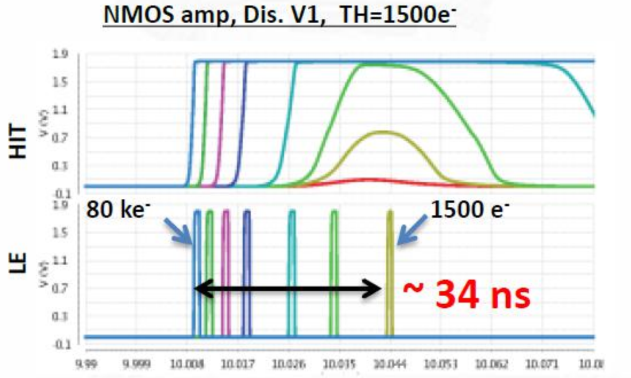


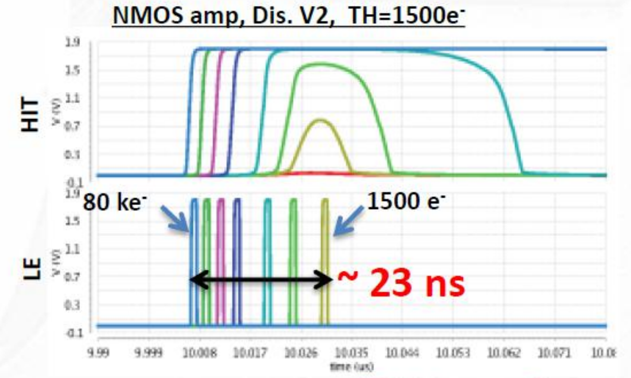
Discriminator V2

Self-bias < 4 µA

Self-biased differential amplifier + CMOS inverter

Faster

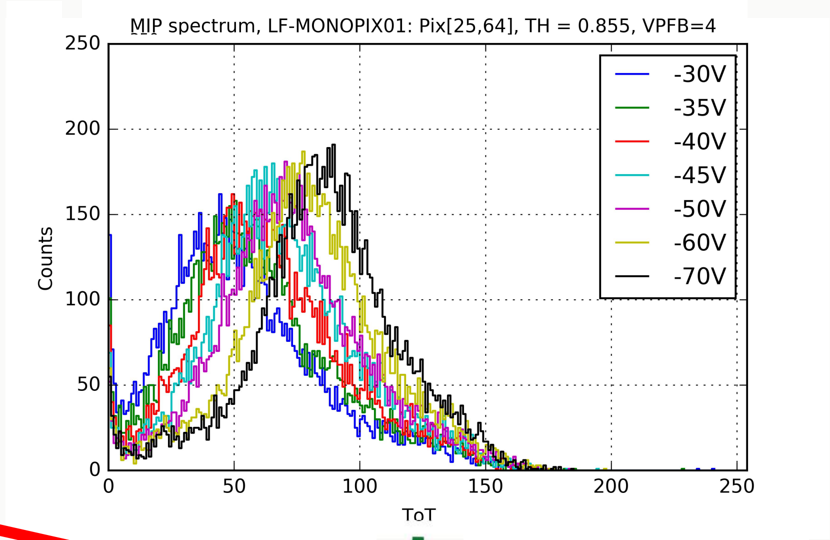




T. Wang, Bonn

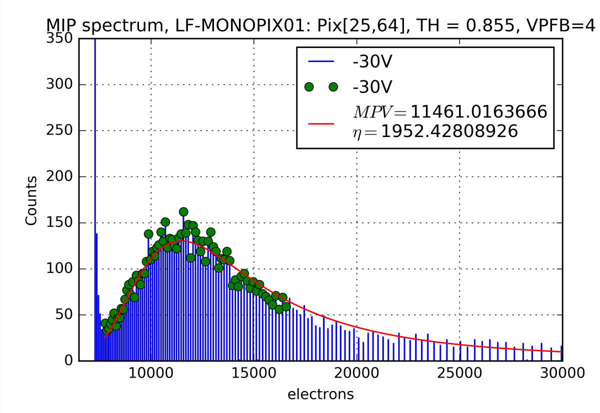
TOT RESPONSE AND CALIBRATION

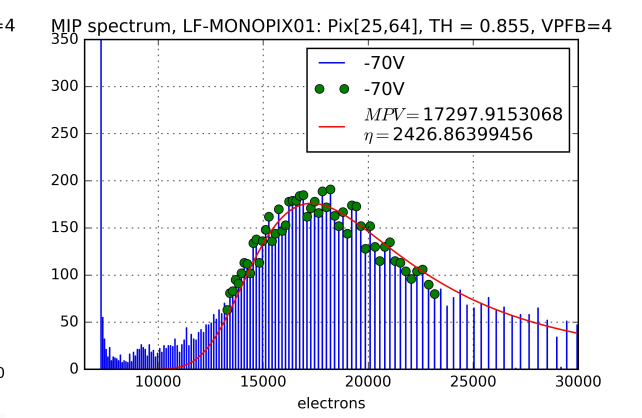
Data from energy loss by 2.5 GeV electrons (MIPs) in silicon for different bias voltages (without cluster size selection)

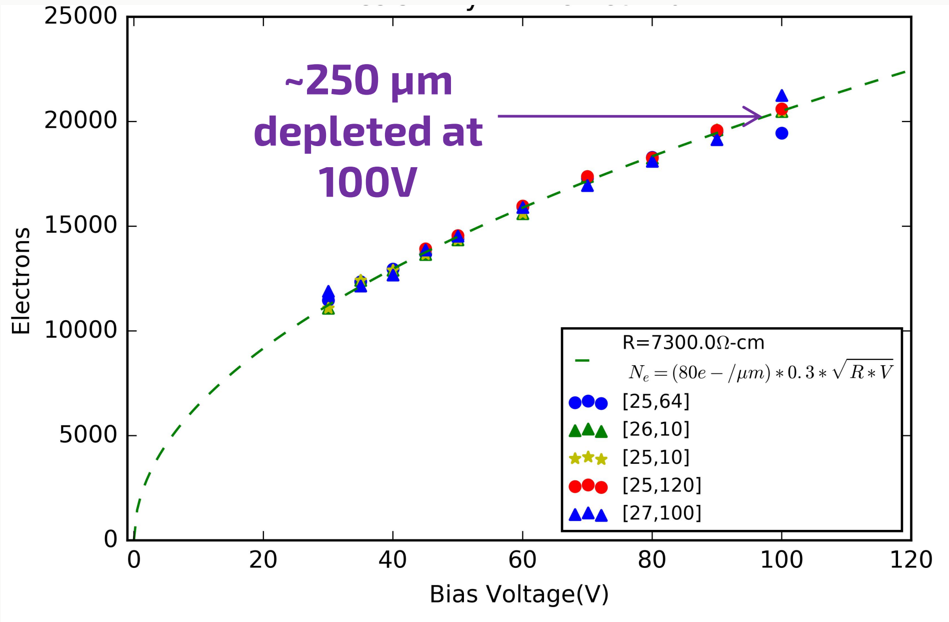


Landau+Gaussian convolution fit to describe every calibrated distribution.

Applying per-pixel calibration



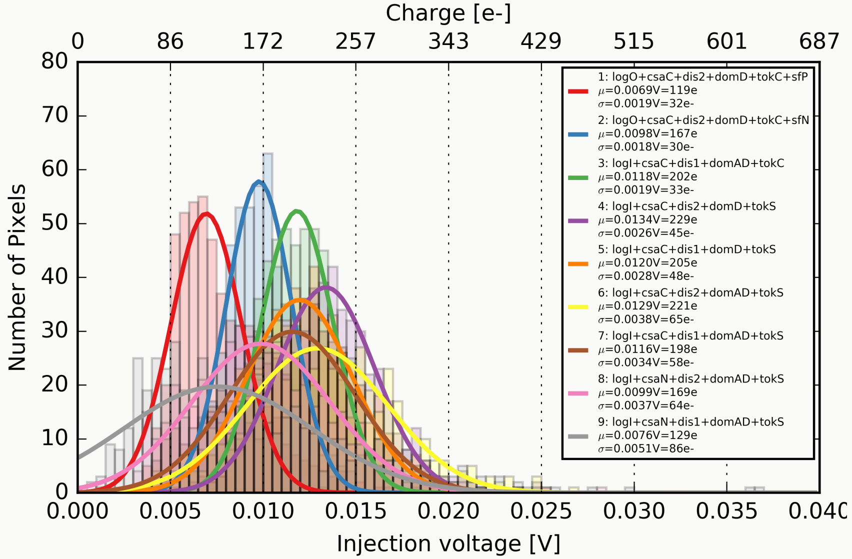


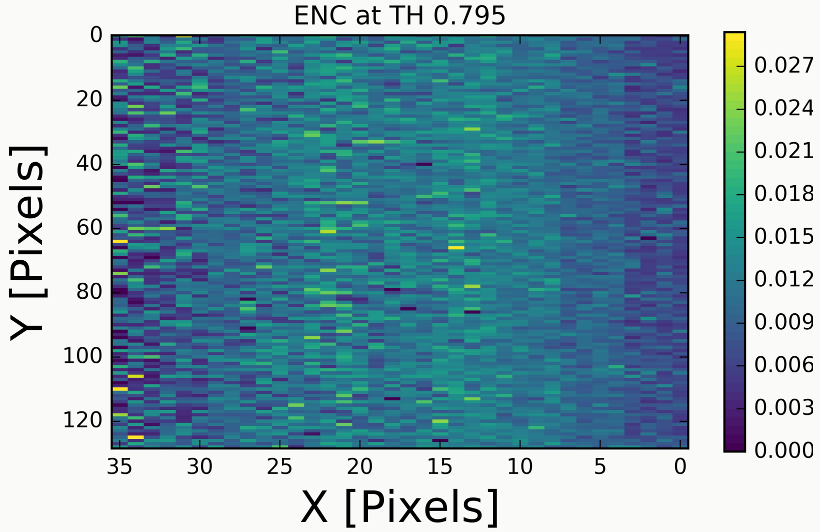


R ~ 7.3 kOhm-cm

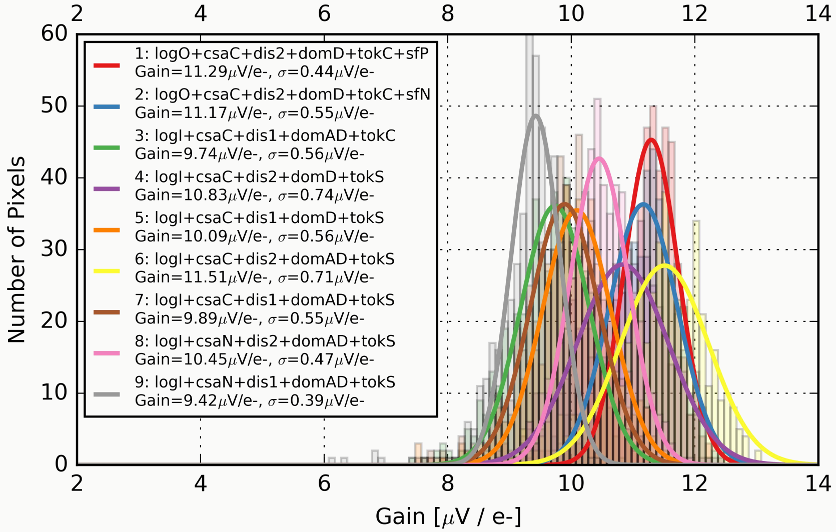
> 2 kOhm-cm, but also higher than previous measurements in other wafers from the same foundry (3.5 and 5.5 kOhm-cm)

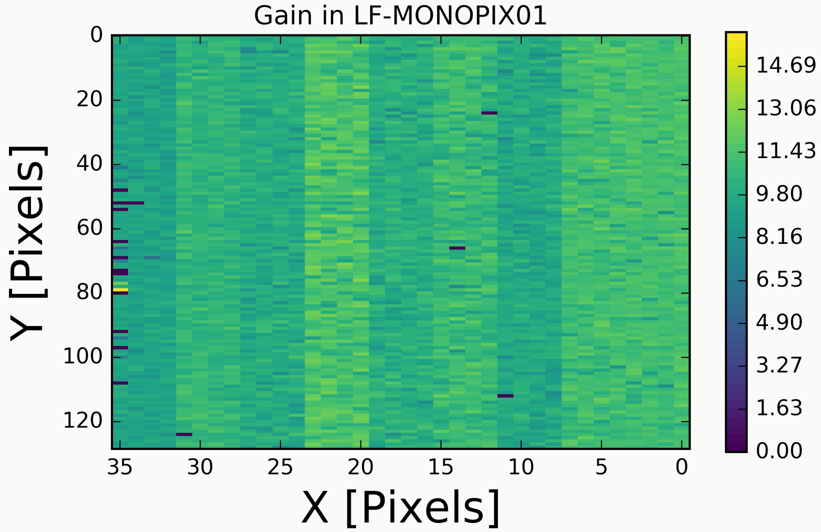
NOISE AND GAIN





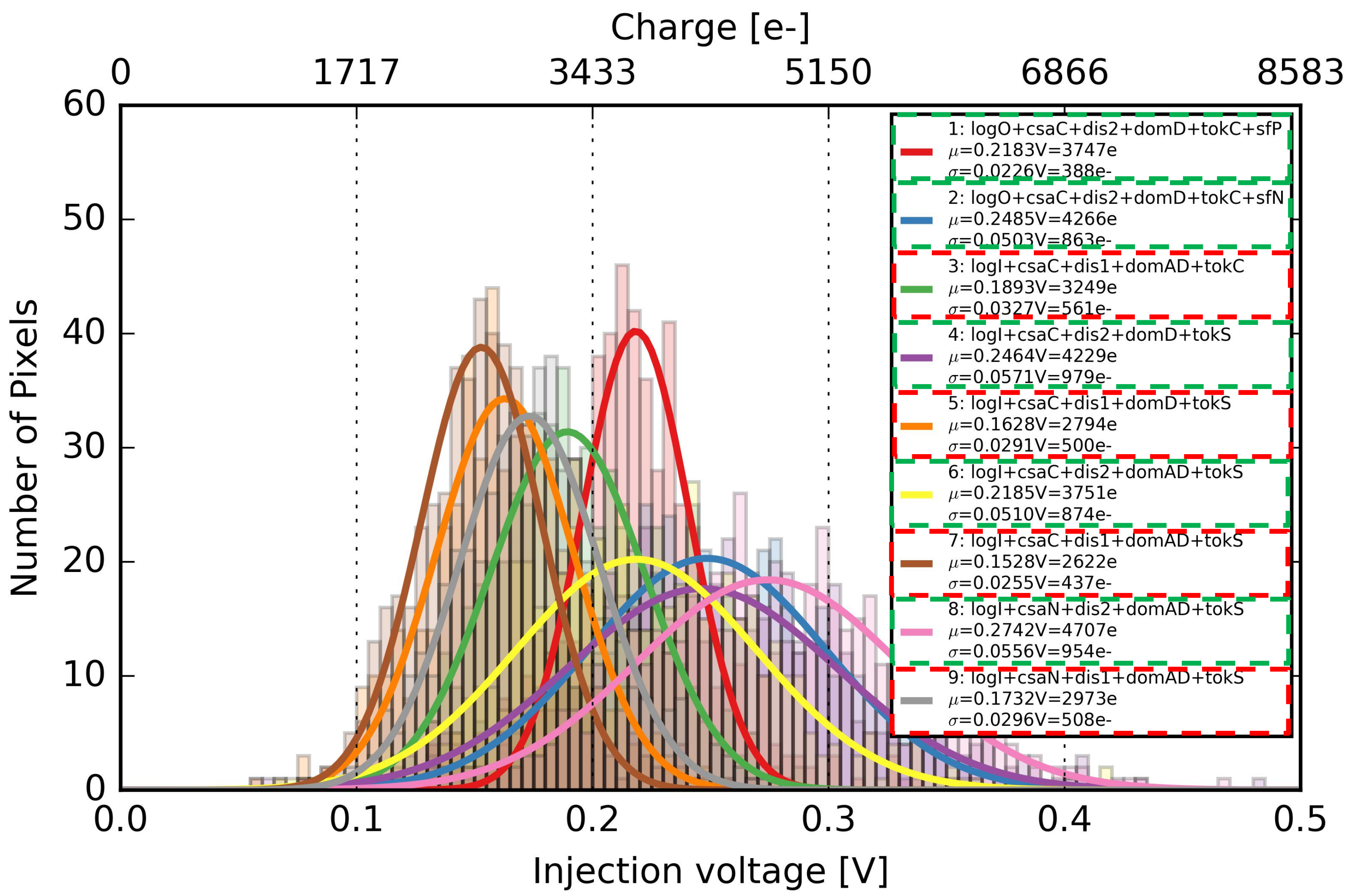
ENC within 120 to 240 e-, with a dispersion between 30 to 70 e-.



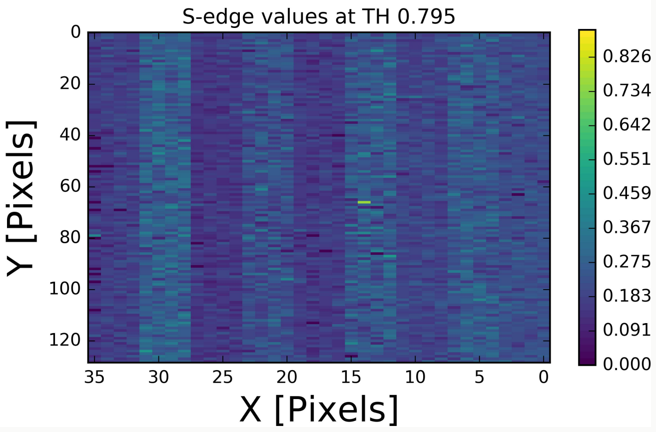


Gain within 10-12 µV / e-

UNTUNED THRESHOLD DISTRIBUTIONS

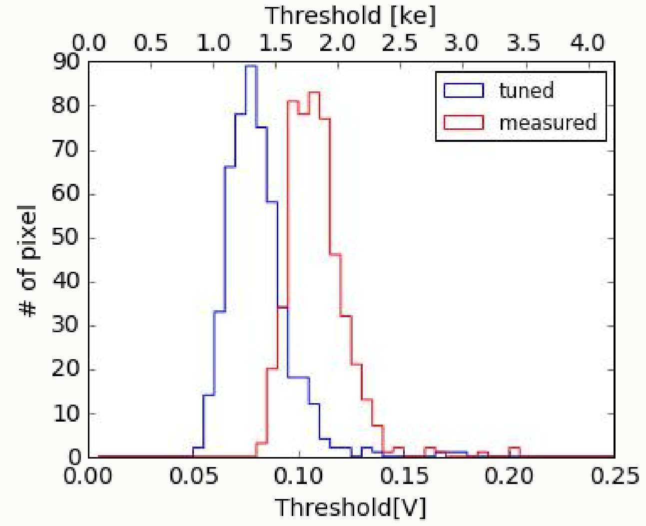


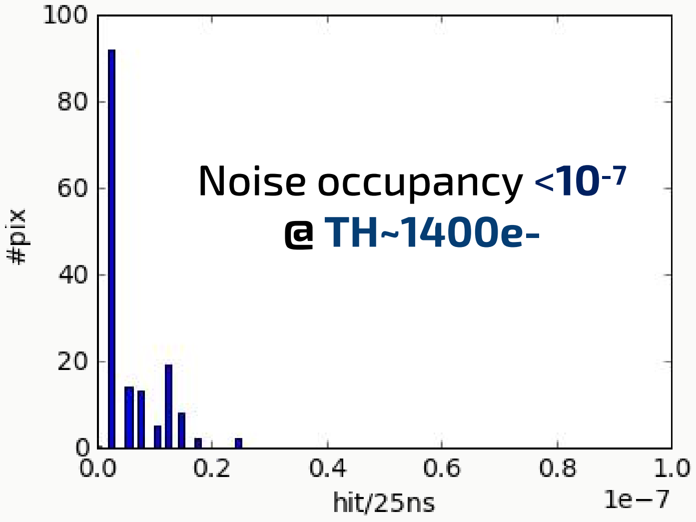
Untuned threshold dispersion for flavours with the **V1** discriminator **~400-600 e-** (**plus 350-400 e-** for those with integrated pixel R/O logic and the **V2** discriminator)



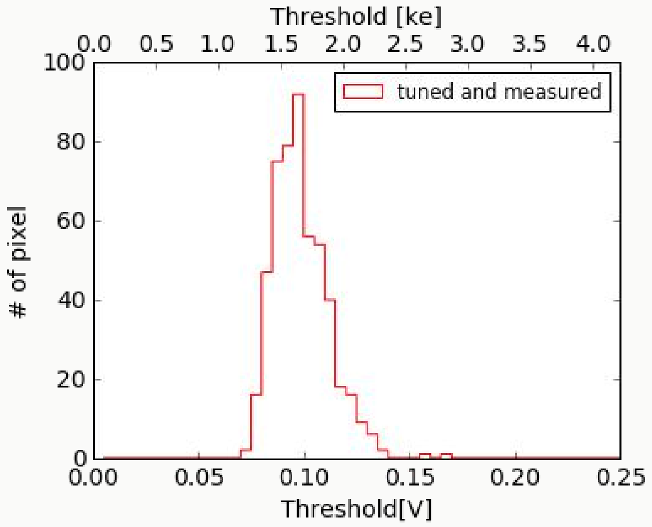
NOISE OCCUPANCY AT LOW THRESHOLD

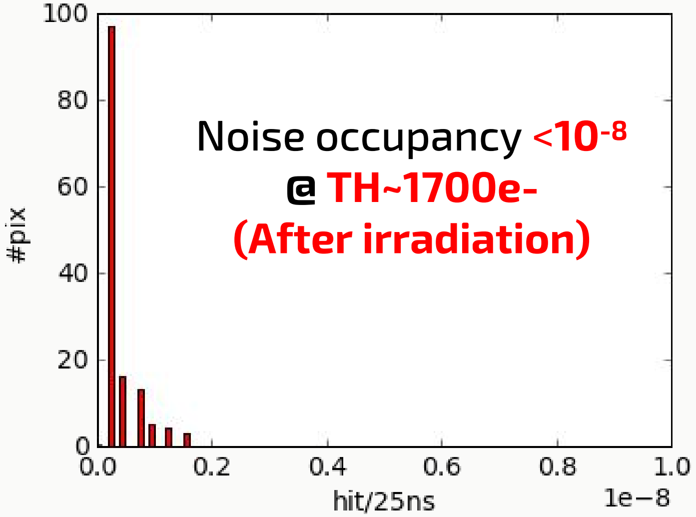
- **Non-irradiated**
  - Threshold: **1400 e-**
  - Dispersion due to noise baseline tuning
  - Bias V: -200V
  - Cooled with dry ice.



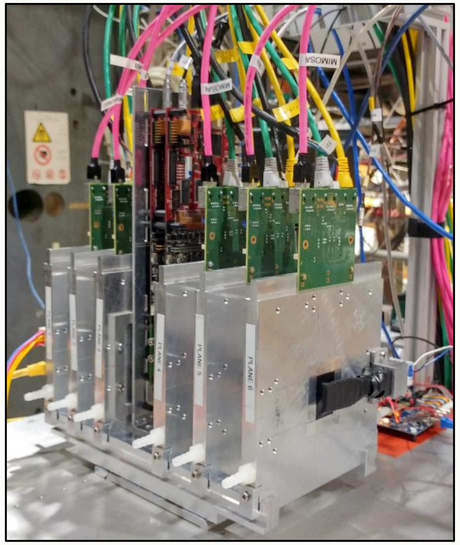


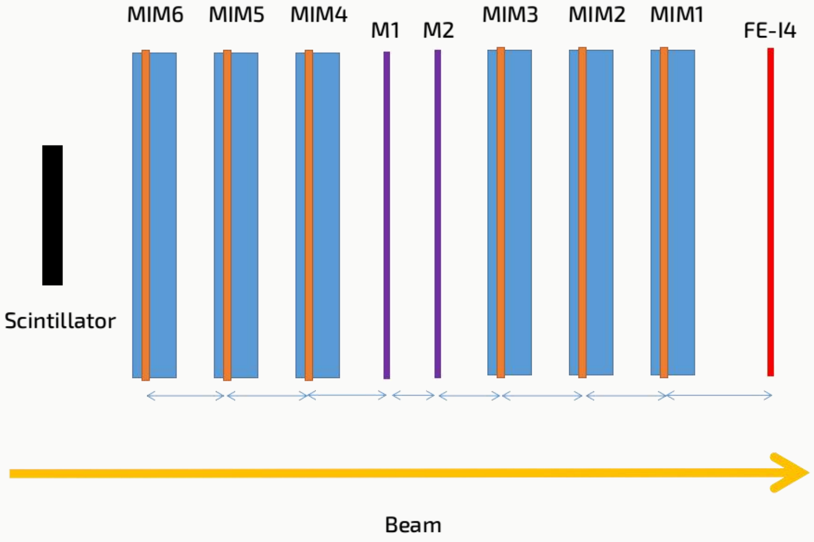
- **Neutron irradiated (1 x $10^{15} n_{eq}/cm^2$)**
  - Threshold: **1700 e-**
  - Bias V: -130V (due to technical issues)
  - Cooled with dry ice.





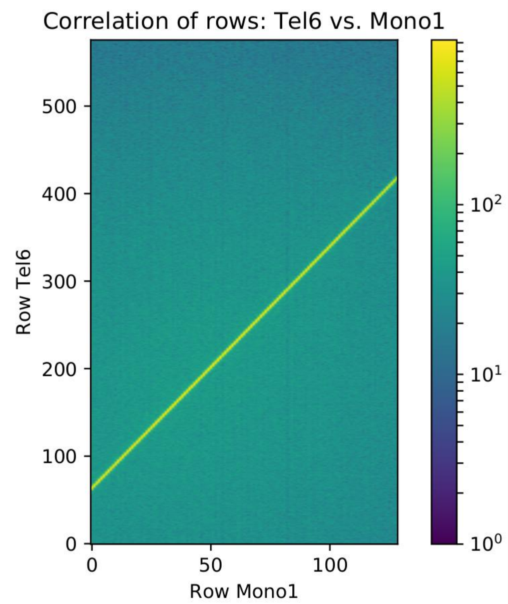
TEST BEAM CAMPAIGNS

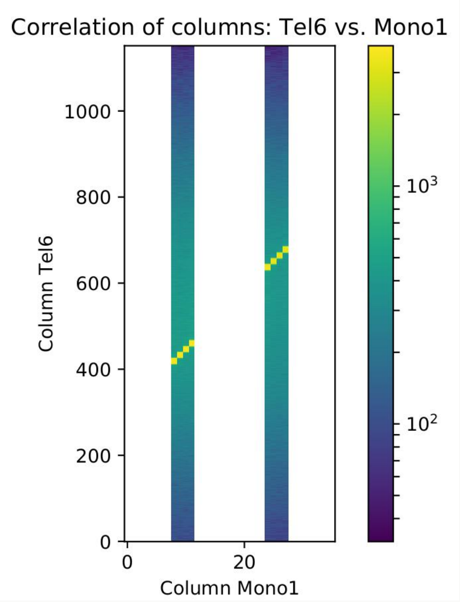




LF-MONOPIX (unirradiated and neutron-irradiated samples) exposed to MIPs at ELSA (2.5 GeV e-) and the H8 line of CERN's SPS (180 GeV pions)

Sample of event correlation (@SPS) MONOPIX <-> MIM26 (6)



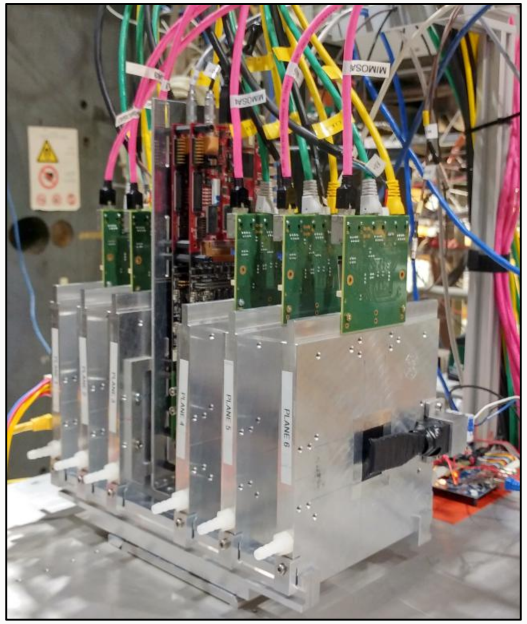


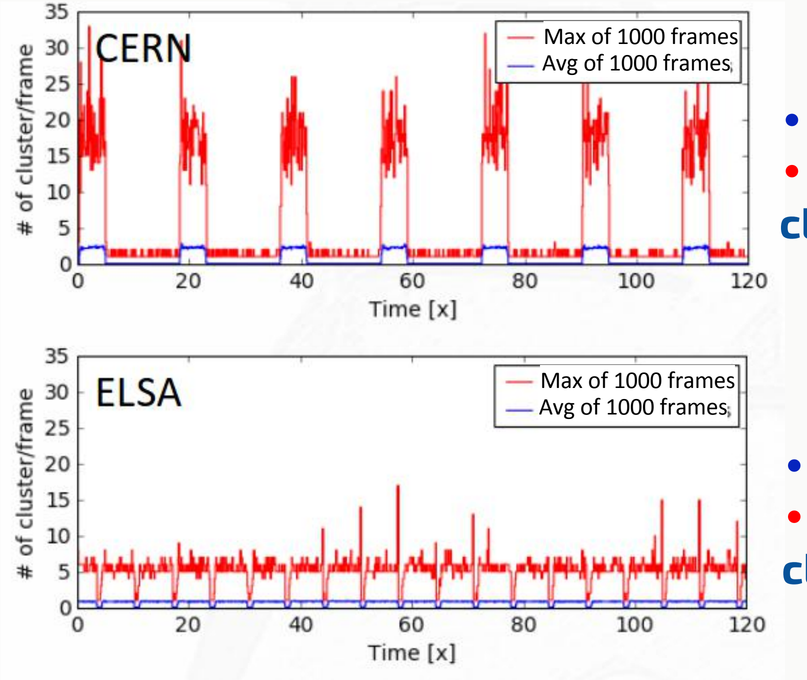
- **MIMOSA26 x 6**
  - Pixel size: 18.2 μm x 18.2μm
  - 1152 μs/frame (rolling shutter)
- **FE-I4 x 1**
  - Pixel size: 250 μm x 50 μm
  - Timing resolution: 25ns (trig. by scintillator + TLU)

TEST BEAM CAMPAIGNS

MONOPIX planes (unirradiated and neutron-irradiated samples) exposed to MIPs at ELSA (2.5 GeV e-) and the H8 line of CERN's SPS (180 GeV pions):

Measurements for different bias and threshold settings.





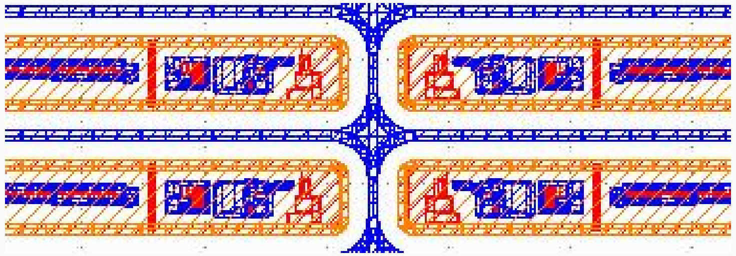
- Avg: 2.2
- Max: ~20

clust/frame

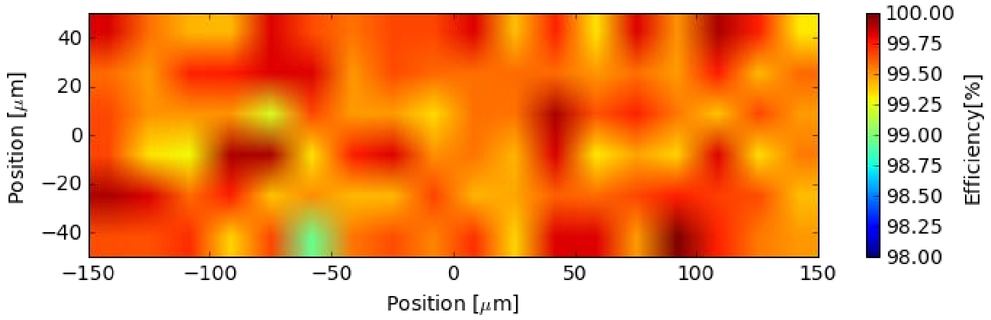
- Avg: 0.8
- Max: ~6

clust/frame

TB @ ELSA: IN-PIXEL EFFICIENCY

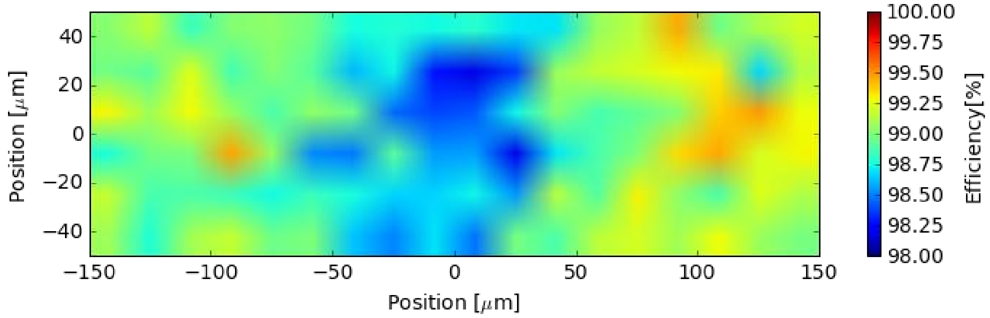


Deep N-well (Collecting electrode…)
P-well (Inter-pixel region, isolation of electronics…)
N-well (R/O electronics…)



Non-irradiated @ -200V:

Uniform efficiency

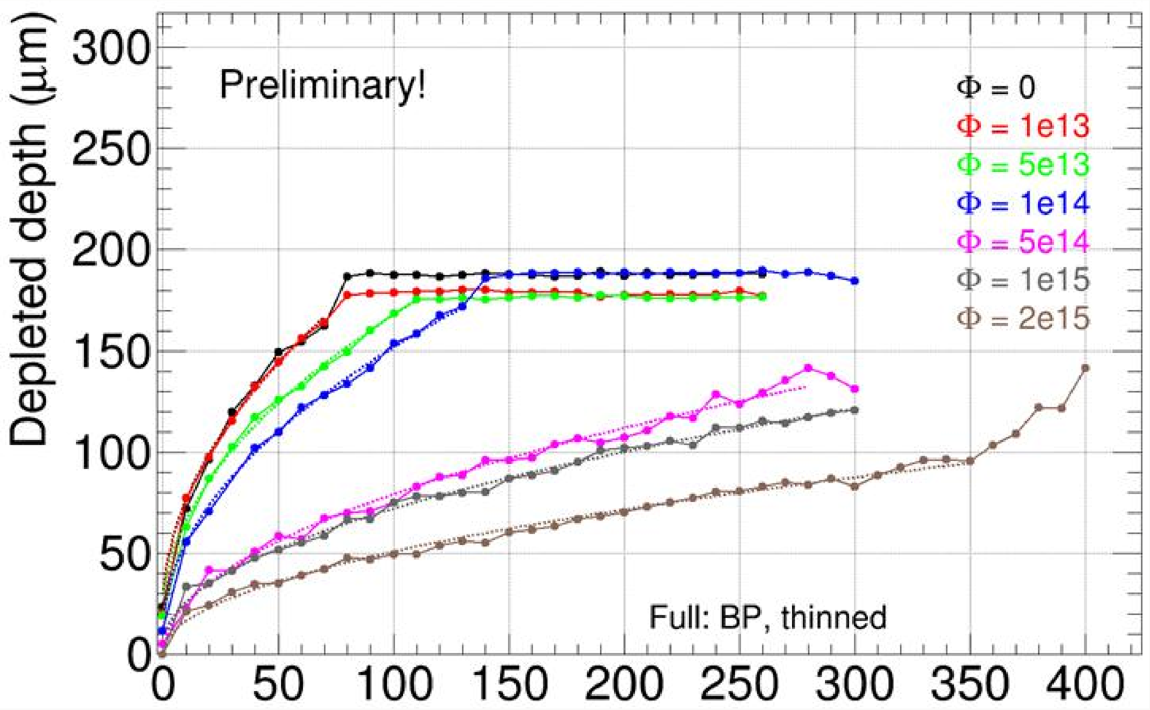


Neutron irradiated (1 x $10^{15} n_{eq}/cm^2$) @-130V

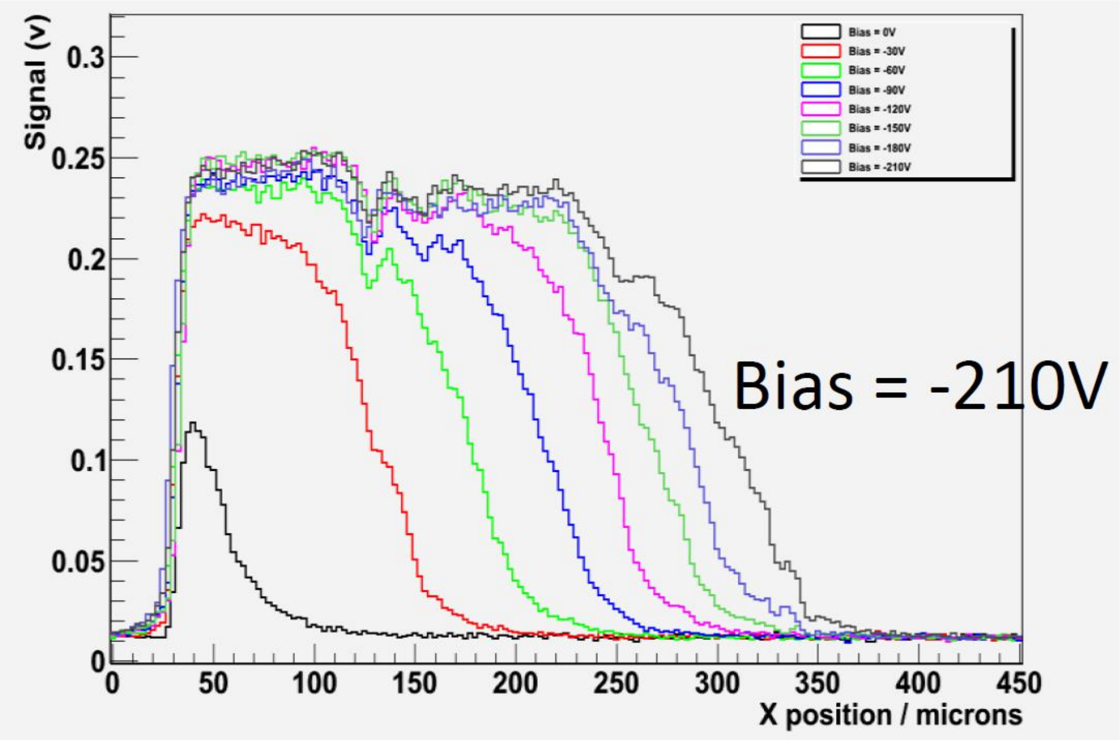
Observed efficiency loss between pixels

E-TCT MEASUREMENTS

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*



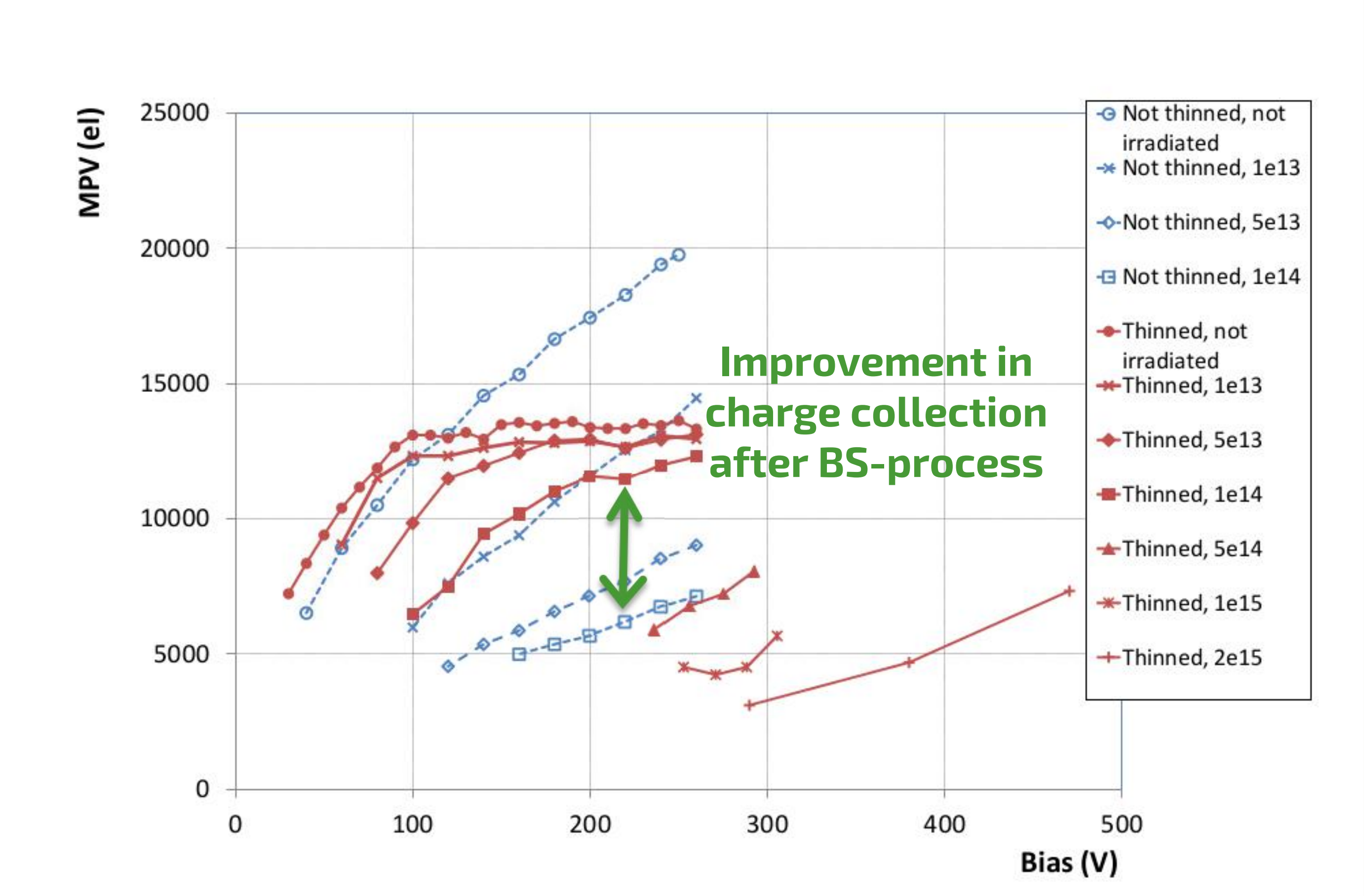
E-TCT measurement on LF test structures thinned to 200µm
I. Mandić, RD50 workshop 2017



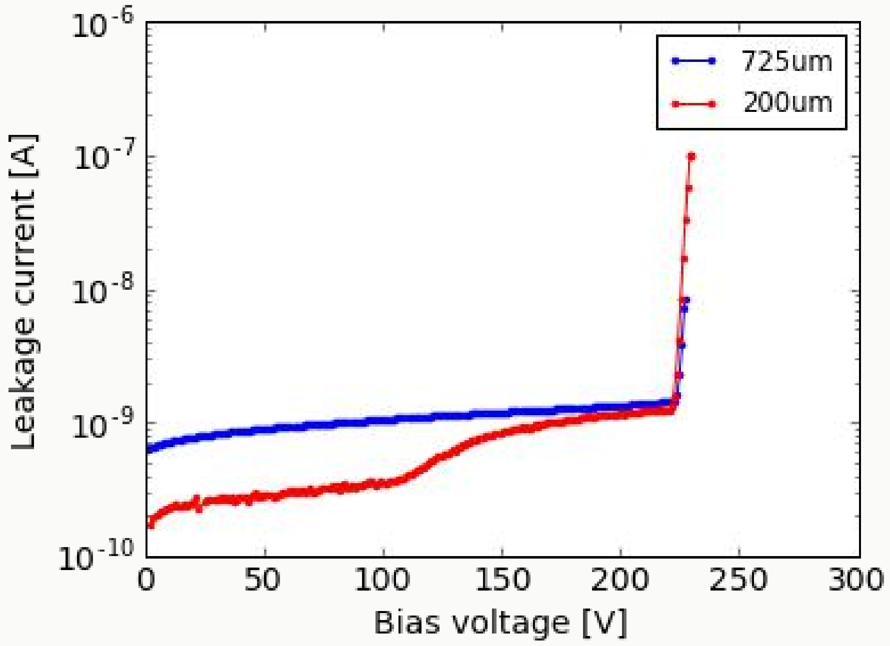
E-TCT measurement on LF-MONOPIX (775µm thick)
L. Vigani. University of Oxford.

IMPROVEMENT AFTER BACKSIDE-PROCESS

* *Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*

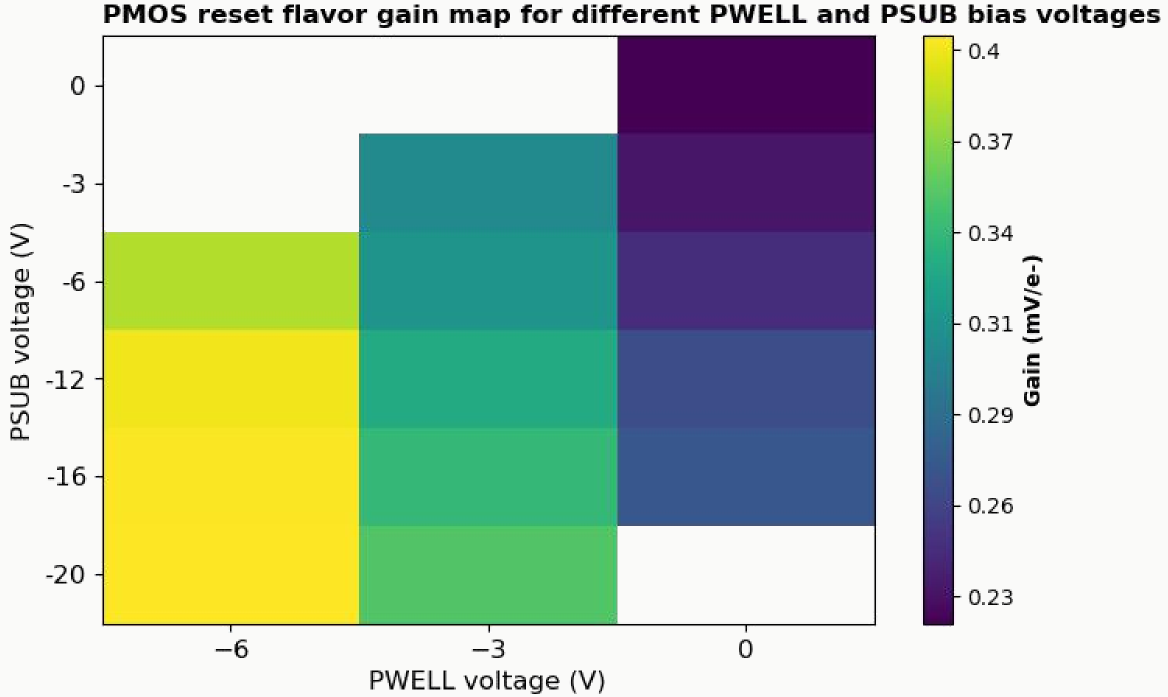


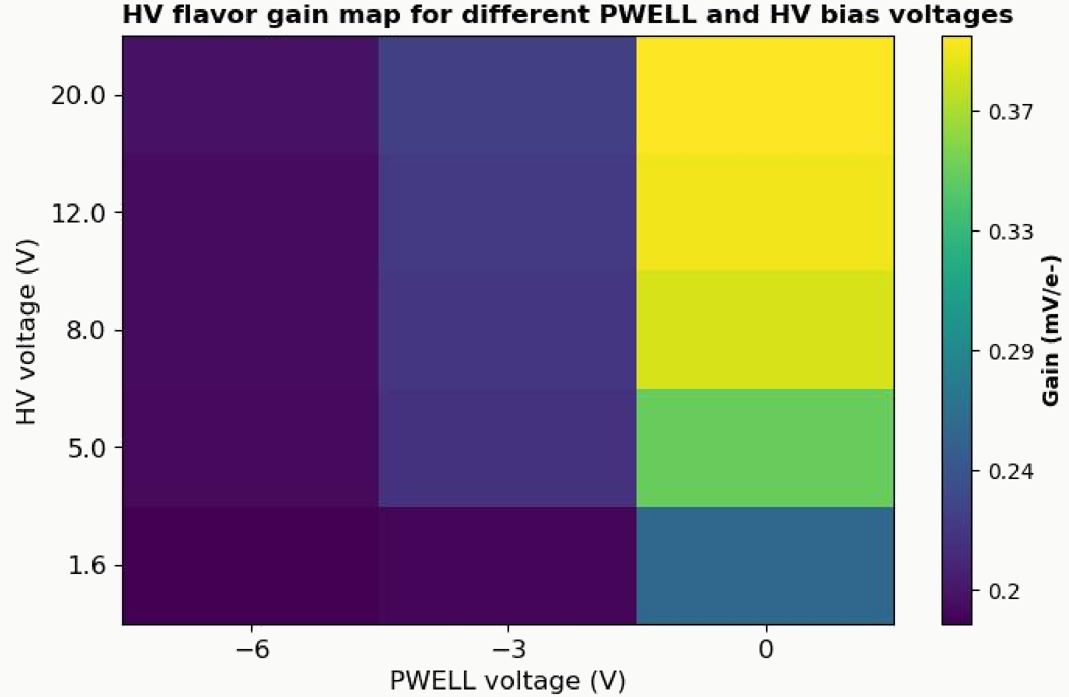
E-TCT measurement on LF test structures thinned and Backside-processsed to 200µm
I. Mandić, RD50 workshop 2017



Reduction in leakage current after thinning and BS-process

TJ-MONOPIX01 GAIN

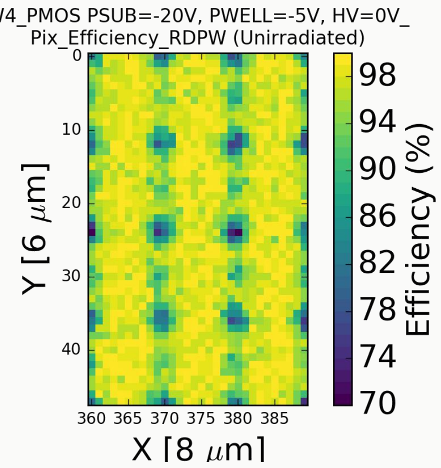




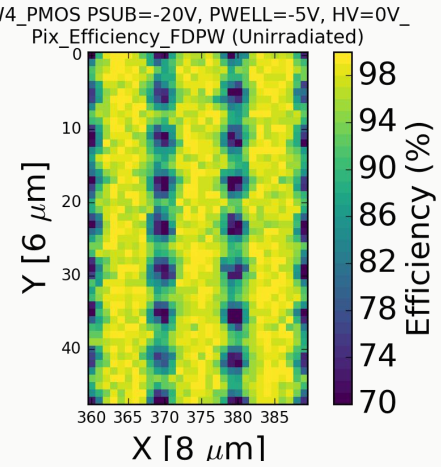
Gain of ~400 uV/e- (or larger) achieved under different bias schemes

IN-PIXEL EFFICIENCY (UNIRRADIATED PMOS VS HV)

PMOS

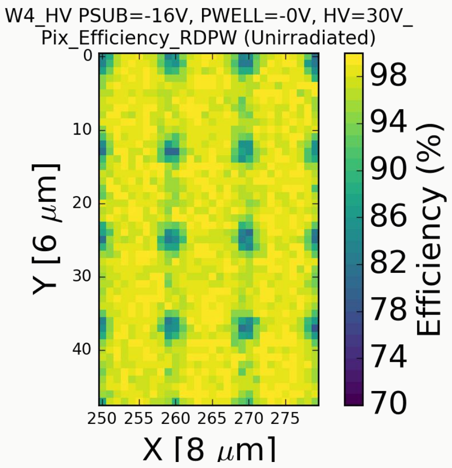


95.9%

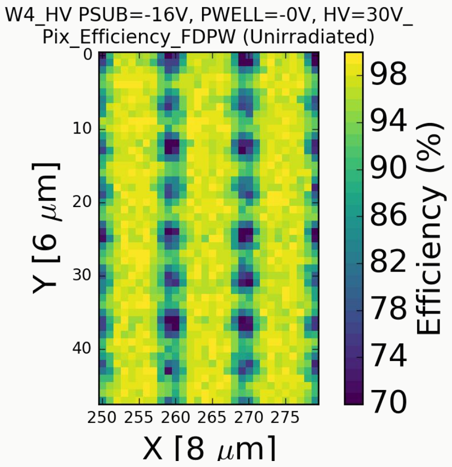


93.5%

HV

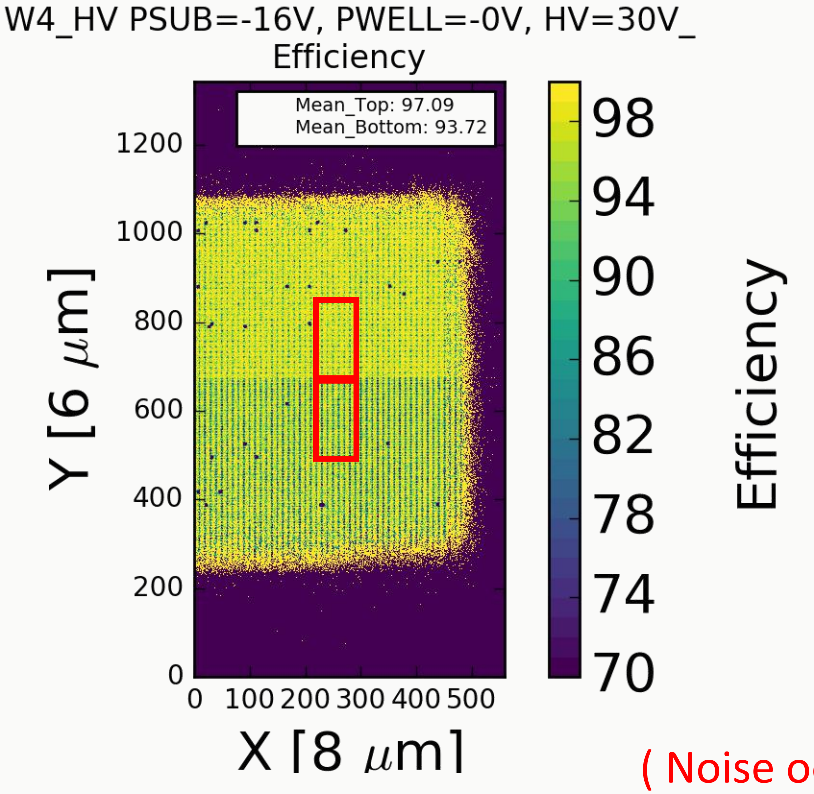


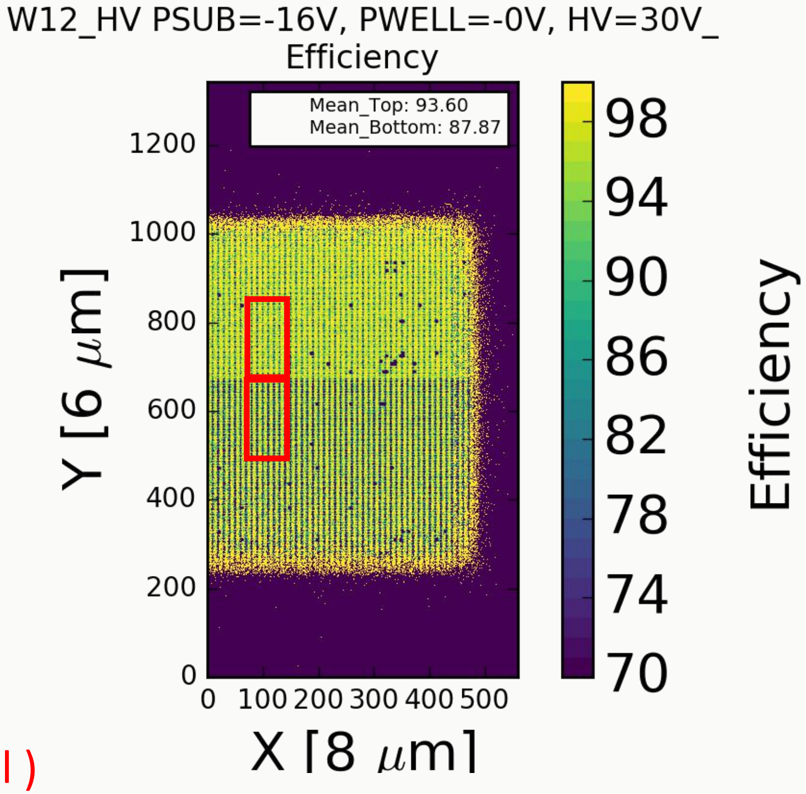
97.1%



93.7%

DIFFERENCES DUE TO N-LAYER DOPING





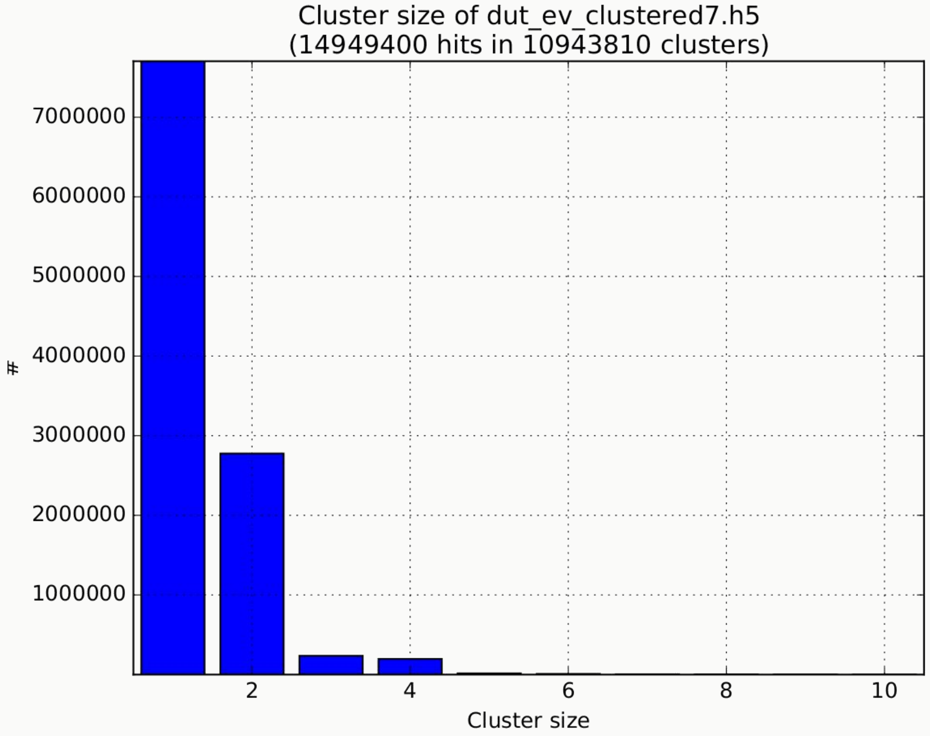
(Noise occupancy < 10 Hz/pixel)

W04 (HV): UNIRRADIATED

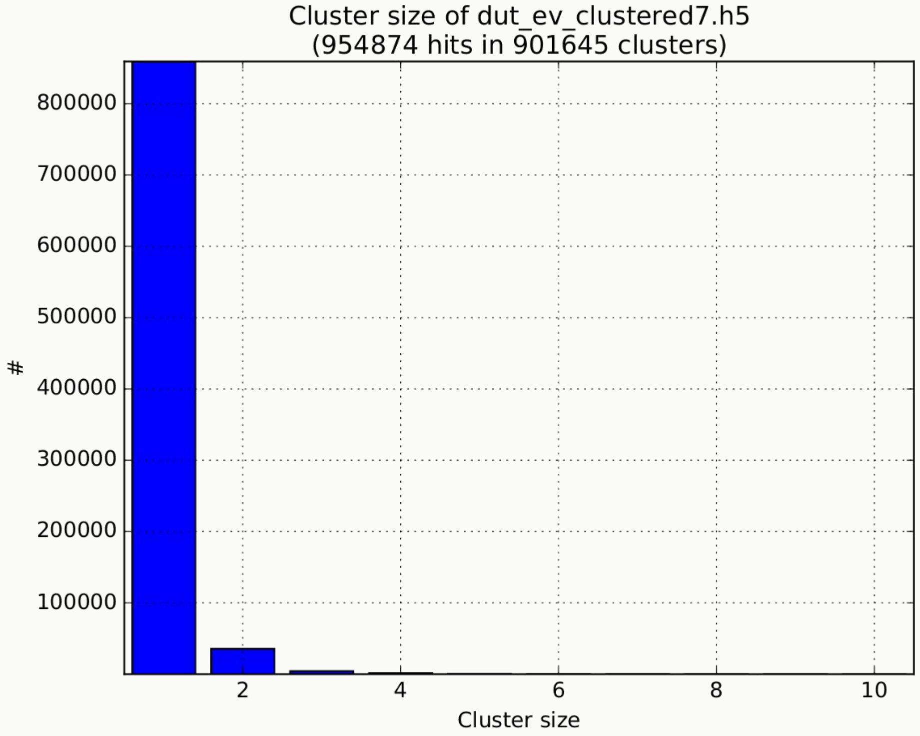
W12 (HV): UNIRRADIATED

- Mean efficiency larger for unirradiated W4 than for W12

CLUSTER SIZE FROM TEST BEAM (TJ-MONOPIX)



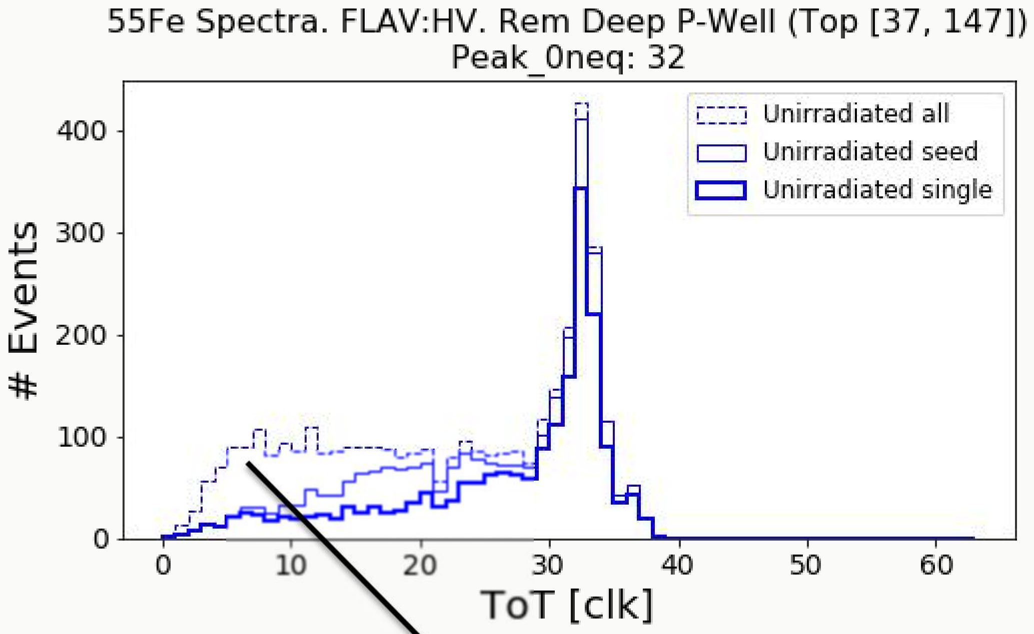
W04 (HV): UNIRRADIATED

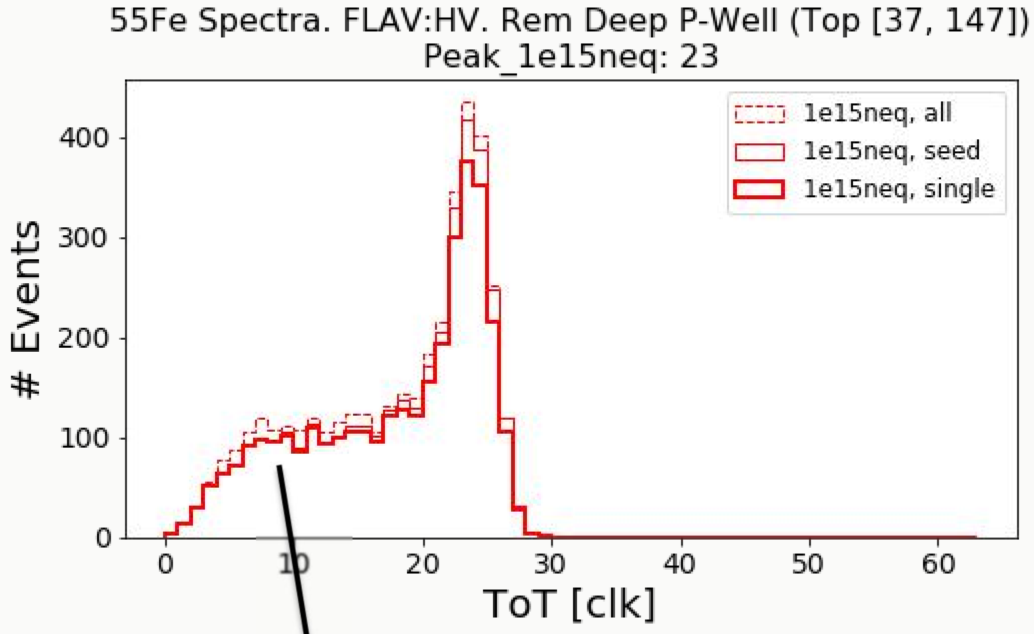


W04 (HV): $1x10^{15}\ n_{eq}/cm^2$

- The cluster size decreases after irradiation ---> Less charge sharing.

55-FE SPECTRA BEFORE AND AFTER IRRADIATION





- We observe charge sharing in the unirradiated sample, but not after irradiation

(This observation agrees with the cluster size measurement during test beam)