Development of CMOS pixel sensor prototypes for the CEPC vertex detector

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On behalf of the CEPC VTX study group

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Outline

- Introduction on the CEPC vertex detector
- CMOS pixel sensor R&D activities
  - Prototype JadePix1/2
  - Prototype MIC4
- Summary and outlook
Reminder about the CEPC – SppC

- **Phase 1:** $e^+ e^-$ Higgs [Z] factory  two detectors, 1M Higgs events in ~10 yrs, at the Z-pole $10^{10}$ Z bosons/yr

  Circular Electron Positron Collider (CEPC)
  - $E_{cm} \approx 240$ GeV, luminosity $\sim 3 \times 10^{34}$ cm$^{-2}$s$^{-1}$, can also run at the Z-pole
  - Precise measurement of the Higgs boson and the Z boson

  Higgs precision 1% or better

- **Phase 2:** a discovery machine for new physics; $pp$ collision with $E_{cm} \approx 50$-100 TeV Supper proton-proton Collider (SppC)

The CDR of CEPC is officially released in November 2018.
# CEPC Beam Timing

<table>
<thead>
<tr>
<th></th>
<th>Higgs</th>
<th>W</th>
<th>Z (3T)</th>
<th>Z (2T)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Center-of-mass energy (GeV)</strong></td>
<td>240</td>
<td>160</td>
<td>91</td>
<td></td>
</tr>
<tr>
<td><strong>Number of IPs</strong></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td><strong>Luminosity/IP ((10^{34} \text{ cm}^{-2} \text{ s}^{-1}))</strong></td>
<td>3</td>
<td>10</td>
<td>16</td>
<td>32</td>
</tr>
<tr>
<td><strong>Number of years</strong></td>
<td>7</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td><strong>Total Integrated Luminosity ((\text{ab}^{-1}) - 2 \text{ IP})</strong></td>
<td>5.6</td>
<td>2.6</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td><strong>Total number of particles</strong></td>
<td>(1 \times 10^6)</td>
<td>(2 \times 10^7)</td>
<td>(3 \times 10^{11})</td>
<td>(7 \times 10^{11})</td>
</tr>
<tr>
<td><strong>Bunch numbers</strong></td>
<td>242 (680 ns)</td>
<td>1524 (210 ns)</td>
<td>12000 (25ns + 10% gap)</td>
<td></td>
</tr>
</tbody>
</table>

- **Continuous colliding mode**
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z

- **General requirement on the detector development:**
  - Precise measurement, Low power, Fast readout, Radiation-hard

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### Vertex Detector Requirements

**Table 2.1** Required performance of the CEPC sub-detectors for critical benchmark Higgs processes.

<table>
<thead>
<tr>
<th>Physics Process</th>
<th>Measured Quantity</th>
<th>Critical Detector</th>
<th>Required Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$ZH \rightarrow \ell^+\ell^-X$</td>
<td>Higgs mass, cross section</td>
<td>Tracker</td>
<td>$\Delta(1/p_T) \sim 2 \times 10^{-5}$</td>
</tr>
<tr>
<td>$H \rightarrow \mu^+\mu^-$</td>
<td>$\text{BR}(H \rightarrow \mu^+\mu^-)$</td>
<td></td>
<td>$\oplus 1 \times 10^{-3}/(p_T \sin\theta)$</td>
</tr>
<tr>
<td>$H \rightarrow b\bar{b}, c\bar{c}, gg$</td>
<td>$\text{BR}(H \rightarrow b\bar{b}, c\bar{c}, gg)$</td>
<td>Vertex</td>
<td>$\sigma_{r\phi} \sim 5 \oplus 10/(p \sin^3/2\theta) \mu m$</td>
</tr>
<tr>
<td>$H \rightarrow q\bar{q}, VV$</td>
<td>$\text{BR}(H \rightarrow q\bar{q}, VV)$</td>
<td></td>
<td>$\sigma_{E}/E \sim 3 - 4%$</td>
</tr>
<tr>
<td>$H \rightarrow \gamma\gamma$</td>
<td>$\text{BR}(H \rightarrow \gamma\gamma)$</td>
<td></td>
<td>$\sigma_{E} \sim 16%/\sqrt{E} \oplus 1% (\text{GeV})$</td>
</tr>
</tbody>
</table>

- Efficient tagging of heavy quarks (b/c) and $\tau$ leptons
  - Impact parameter resolution, $\sigma_{r\phi} = a \oplus \frac{b}{(p \cdot \sin^3/2\theta)} \mu m$

- Design constrains on the vertex (to achieve $a=5$ and $b=10$, $B=3T$)
  - Spatial resolution near the interaction point $\sigma_{sp} \leq 3 \mu m$
  - Material budget $\leq 0.15\% X_0/$layer
  - First layer located at a radius: $\sim 1.6 \text{ cm}$
  - Detector occupancy $\leq 1\%$
Baseline Vertex Detector Layout

**VTX: B= 3T**

- 3 layers of double-sided pixels
- $\sigma_{SP} = 2.8 \, \mu m$ in L1
- Faster pixel sensor in L2, to provide time-stamp
- Polar angle $\theta \sim 15$ degrees
- Total number of pixels: 690M

**Baseline design of VTX**

| Layer | $R$ (mm) | $|z|$ (mm) | $|\cos \theta|$ | $\sigma$ ($\mu$m) |
|-------|----------|------------|----------------|-----------------|
| Layer 1 | 16       | 62.5       | 0.97           | 2.8             |
| Layer 2 | 18       | 62.5       | 0.96           | 6               |
| Layer 3 | 37       | 125.0      | 0.96           | 4               |
| Layer 4 | 39       | 125.0      | 0.95           | 4               |
| Layer 5 | 58       | 125.0      | 0.91           | 4               |
| Layer 6 | 60       | 125.0      | 0.90           | 4               |
Beam-induced Radiation Backgrounds

- Radiation level for VTX first layer

<table>
<thead>
<tr>
<th></th>
<th>H (240)</th>
<th>W (160)</th>
<th>Z (91)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hit Density [hits/cm²·BX]</td>
<td>2.4</td>
<td>2.3</td>
<td>0.25</td>
</tr>
<tr>
<td>TID [MRad/year]</td>
<td>0.93</td>
<td>2.9</td>
<td>3.4</td>
</tr>
<tr>
<td>NIEL [10¹² 1 MeV nₑq/cm²·year]</td>
<td>2.1</td>
<td>5.5</td>
<td>6.2</td>
</tr>
</tbody>
</table>

Table 9.4: Summary of hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) with combined contributions from pair production and off-energy beam particles, at the first vertex detector layer \( r = 1.6 \) cm at different machine operation energies of \( \sqrt{s} = 240, 160 \) and 91 GeV, respectively.

- Vertex detector occupancy

<table>
<thead>
<tr>
<th>Operation mode</th>
<th>H (240)</th>
<th>W (160)</th>
<th>Z (91)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hit density (hits · cm⁻² · BX⁻¹)</td>
<td>2.4</td>
<td>2.3</td>
<td>0.25</td>
</tr>
<tr>
<td>Bunching spacing (µs)</td>
<td>0.68</td>
<td>0.21</td>
<td>0.025</td>
</tr>
<tr>
<td>Occupancy (%)</td>
<td>0.08</td>
<td>0.25</td>
<td>0.23</td>
</tr>
</tbody>
</table>

Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for \(ZH\) production, 160 GeV near \(W\)-pair threshold and 91 GeV for \(Z\)-pole.

Detector **occupancy < 1%**, assuming 10 µs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit.

Pixel Sensor Specifications

■ To achieve single point resolution
   Binary pixel ~ 16 µm
   Analog pixel ~ 20 µm (higher power than binary pixel)

■ To lower the material budget
   Sensor thickness ~ 50 µm
   Air cooling, heat load < 50 mW / cm²

■ To tackle beam-related background
   Fast readout 1 ~ 100 µs/frame
   3.4 Mrad/year & 6.2×10^{12}n_{eq}/(cm^2·year)\?

<table>
<thead>
<tr>
<th>Physics driven requirements</th>
<th>Running constraints</th>
<th>Sensor specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\sigma_{s.p.}) 2.8 µm</td>
<td>(0.15% X_0/\text{layer})</td>
<td>Small pixel 16 µm</td>
</tr>
<tr>
<td>Material budget 16 mm</td>
<td>Air cooling</td>
<td>Thinning 50 µm</td>
</tr>
<tr>
<td>r of Inner most layer</td>
<td></td>
<td>Low power 50 mW / cm²</td>
</tr>
<tr>
<td></td>
<td>beam-related background</td>
<td>Fast readout 1 ~ 100 µs</td>
</tr>
<tr>
<td></td>
<td>radiation damage</td>
<td>Radiation tolerance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4 Mrad / year</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.2×10^{12}n_{eq}/(cm^2·year)</td>
</tr>
</tbody>
</table>

Y. LU, CEPC workshop, Beijing, Nov. 2018.
Sensor Technology Options

- **HR-CMOS pixel sensor**
  - Relatively mature technology
  - Towards compete CMOS & thick sensitive layer, fully depleted substrate
  - More in-pixel functional circuitry → faster read-out & less power, radiation tolerance

- **SOI pixel sensor**
  - Fully depleted HR substrate, potential of 16 μm pixel
  - Full CMOS circuit

- **DEPFET**
  - Possible application for inner most vertex layer
  - Small material budget, low power consumption in sensitive area

- **3D-IC**
  - Ultimate detector, but not mature enough
CMOS pixel sensor

R&D activities
Developed CMOS Pixel Sensor prototypes

<table>
<thead>
<tr>
<th>Prototype</th>
<th>Pixel size (μm²)</th>
<th>Collection diode bias (V)</th>
<th>In-pixel circuit</th>
<th>Matrix size</th>
<th>R/O architecture</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>JadePix1</td>
<td>33 × 33</td>
<td>&lt; 1.8</td>
<td>SF/amplifier</td>
<td>96 × 160</td>
<td>Rolling shutter</td>
<td>JADEPIX1 (IHEP) In measurement</td>
</tr>
<tr>
<td></td>
<td>16 × 16</td>
<td></td>
<td></td>
<td>192 × 128</td>
<td></td>
<td>3.9 × 7.9 mm²</td>
</tr>
<tr>
<td>JadePix2</td>
<td>22 × 22</td>
<td>&lt; 10 V</td>
<td>amp., discriminator</td>
<td>128 × 64</td>
<td>Rolling shutter</td>
<td>JADEPIX2 (IHEP) In measurement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3 × 3.3 mm²</td>
</tr>
<tr>
<td>MIC4</td>
<td>25 × 25</td>
<td>reverse bias</td>
<td>amp., discriminator</td>
<td>112 × 96</td>
<td>Asynchronous</td>
<td>MIC4 (CCNU &amp; IHEP) In measurement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.2 × 3.7 mm²</td>
</tr>
</tbody>
</table>

All prototypes in TowerJazz 180 nm process
Prototype JadePix-1 — design

- **Design goals:** sensor optimization and radiation study
- **A variety of sensor geometries**
  - Matrix-1 with $33 \times 33 \, \mu m^2$ pixels (except one sector SFA20 with $16\times16 \, \mu m^2$ pixels), including 16 variations
  - Matrix-2 with $16\times16 \, \mu m^2$ pixels, including 12 variations
- **Different pixel structures**
  - DC-coupled sensor with source follow: 2T/3T structure
  - Pixel with pre-amplifier
  - AC-coupled pixels
- **Analog readout**
  - Each pixel array has 16 analog outputs in-parallel
  - Each array read out in rolling shutter mode

**JadePix-1 has been fully characterized with radioactive sources and test beam**

*Details will be presented by L. Chen in this session*
Prototype JadePix-2 — design

- **Chip overview:**
  - \(3 \times 3.3 \text{ mm}^2\)
  - \(96 \times 112\) binary pixels with 8 sub-matrix
  - Rolling shutter read out mode
    - 100 ns / row (Version 1), 80 ns / row (Version 2)
    - 3.7 \(\mu\text{A} / \text{pixel}\) (Version 1), 6.5 \(\mu\text{A} / \text{pixel}\) (Version 2)
  - Every 16 columns share one output port
    - through the Parallel-In Serial-Out block
  - LVDS transmitter @160 MHz clock
  - A few columns configured as analog readout
    - For calibration of sensing diode

```
<table>
<thead>
<tr>
<th></th>
<th>D1</th>
<th>A1</th>
<th>A2</th>
<th>D2</th>
<th>D3</th>
<th>A3</th>
<th>A4</th>
<th>D4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode size</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4 (\mu\text{m}^2)</td>
<td></td>
<td></td>
<td></td>
<td>8 (\mu\text{m}^2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Matrix size:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1): 48 row \times 44 col.</td>
<td>①</td>
<td></td>
<td>②</td>
<td></td>
<td></td>
<td>①</td>
<td>②</td>
<td></td>
</tr>
<tr>
<td>(2): 48 row \times 4 col.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(3): 48 row \times 60 col.</td>
<td>③</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

*Floorplan of JadePix2*
Prototype JadePix-2 — design

- **Pixel size**: $22 \times 22 \, \mu m^2$
- **Two versions of front-end**
  - Version 1: differential amplifier + dynamic latch
  - Version 2: single-ended amplifier + dynamic latch
- **Offset cancellation and high precision comparator**
  - FPN (Fix Pattern Noise) $\sim 20 \, e^{-}$
  - TN (Temporal Noise) $\sim 7 \, e^{-}$

![Version 1: differential amplifier + latch](image1)

![Version 2: two stage common source amplifiers + latch](image2)
Prototype JadePix-2 — test results

- S-curve measured on Version 1 pixels (differential)
- ENC = 31 e-
  - TN ~ 11 e-
  - FPN ~ 29 e-

**FPN:** 1.08mV @ input node
Equivalent 29.1 e⁻

**TN:** 0.4mV @ input node
Equivalent 10.8 e⁻

Test with radioactive sources in progress
Prototype MIC4 — design

Overview:
- Die size: $3.1 \times 4.6 \text{ mm}^2$
- Matrix of 128 rows $\times$ 64 columns binary pixels
- Pixel size $25 \mu\text{m} \times 25 \mu\text{m}$
- Readout speed: 25 ns/pixel
- Matrix power $< 20 \text{ mW/cm}^2$
- Two versions of pixel front-end
  - Low power, compact layout, active continuously
- Data driven readout
  - No memory in this version
  - High speed data link of 1.2 Gbps
- Possible to apply a reverse bias voltage to the substrate
  - Larger depletion volume
  - Lower sensor capacitance
  - Increase S/N
Two versions of the in-pixel front-end:

**Version 1:**
- Same structure as ALPIDE chip (for ALICE ITS upgrade)*, with different parameters
- Peaking time < 1 μs, pulse duration < 3 μs, with power cons. of 110 nW/pixel
- ENC: ~ 10 e-
- Area: ~ 25 × 9.3 μm²

**Version 2:**
- CSA based front-end, with a very low feedback capacitance
- Peaking time < 1 μs, with power cons. of 50 nW/pixel
- ENC: ~ 24 e-
- Area: ~ 25 × 9.3 μm²

*Ref: D. Kim et al., 2016 JINST 11 C02042
Prototype MIC4 — design

- **Matrix read-out:**
  - **Data driven** $\rightarrow$ very low power consumption
  - **Zero-suppression** readout architecture: OR-gate chain & Address Encoder and Reset Decoder (AERD) combination $\rightarrow$ for highly compact pixel & fast readout & low power
  - **OR-gate chain inside a super pixel** (8×8 pixels) to do the zero-suppression, two dimension projection (ADDRX & ADDRY) to identify the hit pixel $\rightarrow$ save pixel logic and address lines area
  - **AERD between one column of the super pixels** $\rightarrow$ save power and readout time
Prototype MIC4 — test results

- Pixels with front-end version 1:
  - Analog power: \(\sim 24 \text{ mW/cm}^2\)
  - Average noise \(\sim 6 \text{ e}^-\)
  - Average threshold dispersion 31 e\(^-\), factor \(\sim 7\) higher than simulation

- Pixels with front-end version 2:
  - Analog power: \(\sim 8 \text{ mW/cm}^2\)
  - Average noise \(\sim 18 \text{ e}^-\)
  - Average threshold dispersion 120 e\(^-\), factor \(\sim 8\) higher than simulation

Increase in threshold spread under investigation

13 December 2018, PIXEL2018, Taipei
Prototype MIC4 — test results

- X-ray source imaging test: using 6 KV, get picture of “ccnu” (ccnu are copper wires)

X-ray test platform

X-ray image of “ccnu”

Test with radioactive sources in progress
Pixel detector with high spatial resolution, low power and fast readout is required for the CEPC vertex detector

Three prototypes have been designed and characterized in lab

- The binary pixels with low-power front-end and small area are implemented
- Two sensor readout architectures are developed in parallel
- Shows promising results in terms of front-end performance and readout capability
  - Improvement in threshold dispersion needed
- Characterization of the JadePix-2 and MIC4 on-going

Optimization study of vertex system needed

Coordination of design team for next submissions

- Design of prototype with large pixel matrix
- Novel readout scheme exploration in progress

Radiation hardness design
ACKNOWLEDGMENTS

IHEP team:

CCNU team:

Thanks for your attention!
Backup slides
• CEPC data-taking starts before the LHC program ends around 2035
• possibly con-current, and complimentary to the ILC

Ref: CEPC workshop, X. LOU, Nov. 2018, Beijing, China.
Performance Studies — IP Resolution

Graph 1: 
- Full simulation ($\theta=85^\circ$)
- Full simulation ($\theta=20^\circ$)
- Fast simulation ($\theta=85^\circ$)
- Fast simulation ($\theta=20^\circ$)
- Requirement ($\theta=85^\circ$)
- Requirement ($\theta=20^\circ$)

Graph 2: 
- Full sim, CEPC baseline, 1 GeV
- Full sim, CEPC baseline, 100 GeV
- Full sim, single point resolution worse by 50%, 1 GeV
- Full sim, single point resolution worse by 50%, 100 GeV
- Fast sim, CEPC baseline, 1 GeV
- Fast sim, CEPC baseline, 100 GeV
- Fast sim, single point resolution worse by 50%, 1 GeV
- Fast sim, single point resolution worse by 50%, 100 GeV

Graph 3: 

Graph 4: 

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Detector Concepts

- **Baseline detector concept**
  - Silicon tracker + TPC
  - or Full Silicon Tracker
  - High granular calorimetry system
  - 3 Tesla solenoid
  - Muon detector

- **Alternative detector concept, IDEA**
  - Silicon pixel + Drift Chamber
  - 2 Tesla solenoid
  - Dual readout calorimeter
  - Muon chamber