Development of CMOS pixel sensor prototypes for the CEPC vertex detector

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On behalf of the CEPC VTX study group

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Outline

- **Introduction on the CEPC vertex detector**
- **CMOS pixel sensor R&D activities**
    - Prototype JadePix1/2
    - Prototype MIC4
- **Summary and outlook**

Reminder about the CEPC – SppC

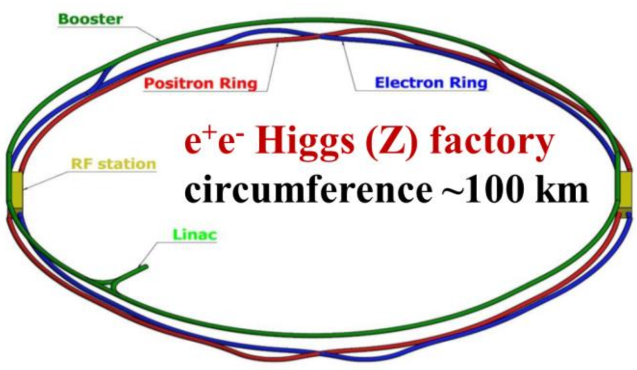
- **Phase 1: e$^+$ e$^-$ Higgs [Z] factory two detectors, 1M Higgs events in ~10 yrs, at the Z-pole 10^{10} Z bosons/yr**

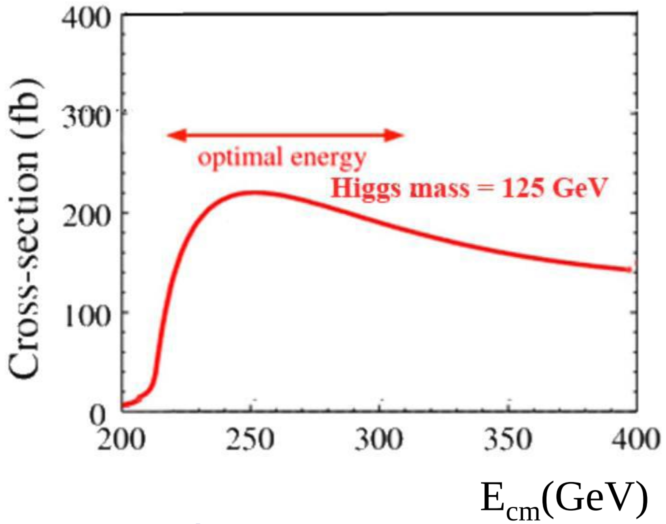
  Higgs precision 1% or better

  Circular Electron Positron Collider (CEPC)

  - **E_{cm} ≈ 240 GeV, luminosity ~3×10^{34} cm^{-2}s^{-1}, can also run at the Z-pole**
  - **Precise measurement of the Higgs boson and the Z boson**

- **Phase 2: a discovery machine for new physics; pp collision with E_{cm} ≈ 50-100 TeV Supper proton-proton Collider (SppC)**





The CDR of CEPC is officially released in November 2018.

CEPC Beam Timing

	Higgs	W	Z (3T)	Z (2T)
Center-of-mass energy (GeV)	240	160	91	
Number of IPs	2			
Luminosity/IP (10^{34} cm^{-2} s^{-1})	3	10	16	32
Number of years	7	1	2	
Total Integrated Luminosity (ab^{-1}) - 2 IP	5.6	2.6	8	16
Total number of particles	1×10^{6}	2×10^{7}	3×10^{11}	7×10^{11}
Bunch numbers (**Bunch spacing**)	242 (**680 ns**)	1524 (**210 ns**)	12000 (**25ns + 10% gap**)	

- Continuous colliding mode
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z
- General requirement on the detector development:
  - Precise measurement, Low power, Fast readout, Radiation-hard

Y. LU, Circular Electron Positron Collider workshop, Beijing, Nov. 2018.

Vertex Detector Requirements

Table 2.1 Required performance of the CEPC sub-detectors for critical benchmark Higgs processes.

Physics Process	Measured Quantity	Critical Detector	Required Performance
$ZH \to \ell^+\ell^- X$	Higgs mass, cross section	Tracker	$\Delta(1/p_T) \sim 2 \times 10^{-5}$
$H \to \mu^+\mu^-$	$\mathrm{BR}(H \to \mu^+\mu^-)$		$\oplus 1 \times 10^{-3}/(p_T \sin\theta)$
$H \to b\bar{b},\ c\bar{c},\ gg$	$\mathrm{BR}(H \to b\bar{b},\ c\bar{c},\ gg)$	Vertex	$\sigma_{r\phi} \sim 5 \oplus 10/(p \sin^{3/2}\theta)\ \mu\mathrm{m}$
$H \to q\bar{q},\ VV$	$\mathrm{BR}(H \to q\bar{q},\ VV)$	ECAL, HCAL	$\sigma_E^{\mathrm{jet}}/E \sim 3-4\%$
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\sigma_E \sim 16\%/\sqrt{E} \oplus 1\%$ (GeV)

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

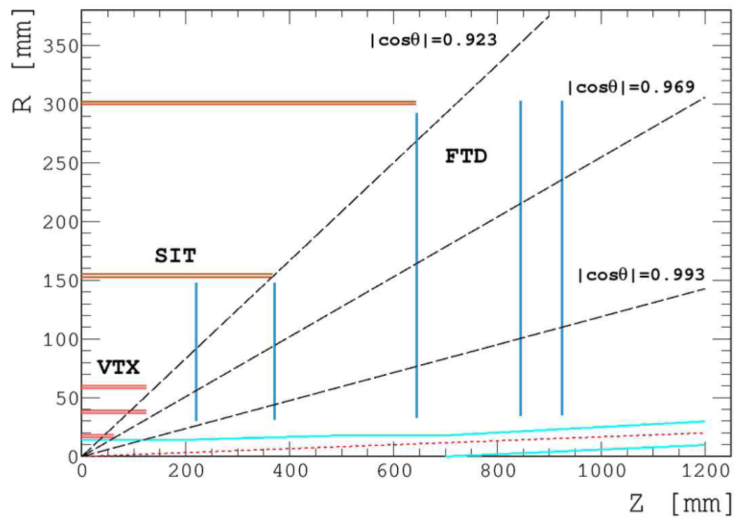
➔ Impact parameter resolution, $\sigma_{r\emptyset} = a \oplus \frac{b}{(p\cdot sin^{3/2}\theta)}\ \mu m$

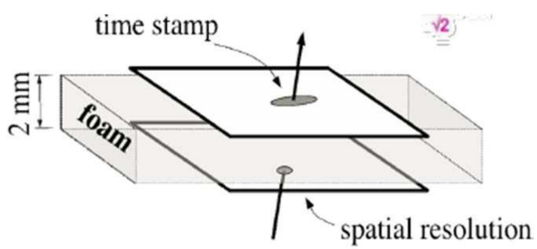
- **Design constrains on the vertex (to achieve a=5 and b=10, B=3T)**
  - spatial resolution near the interaction point $\sigma_{sp} \leq 3$ μm
  - material budget ≤ 0.15% X_0/layer
  - first layer located at a radius: ~1.6 cm
  - Detector occupancy ≤ 1%

Baseline Vertex Detector Layout

VTX: B= 3T

- 3 layers of double-sided pixels
- σ_{SP} = 2.8 μm in L1
- Faster pixel sensor in L2, to provide time-stamp
- Polar angle θ ~15 degrees
- Total number of pixels: 690M





a double-sided ladder concept

Baseline design of VTX

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ(μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Beam-induced Radiation Backgrounds

- **Radiation level for VTX first layer**

	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2·BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2·year]	2.1	5.5	6.2

Table 9.4: Summary of hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) with combined contributions from pair production and off-energy beam particles, at the first vertex detector layer ($r = 1.6$ cm) at different machine operation energies of $\sqrt{s} = 240$, 160 and 91 GeV, respectively.

- **Vertex detector occupancy**

Operation mode	**H (240)**	**W(160)**	**Z (91)**
Hit density (hits $\cdot$ cm^{-2} $\cdot$ BX^{-1})	2.4	2.3	0.25
Bunching spacing (µs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

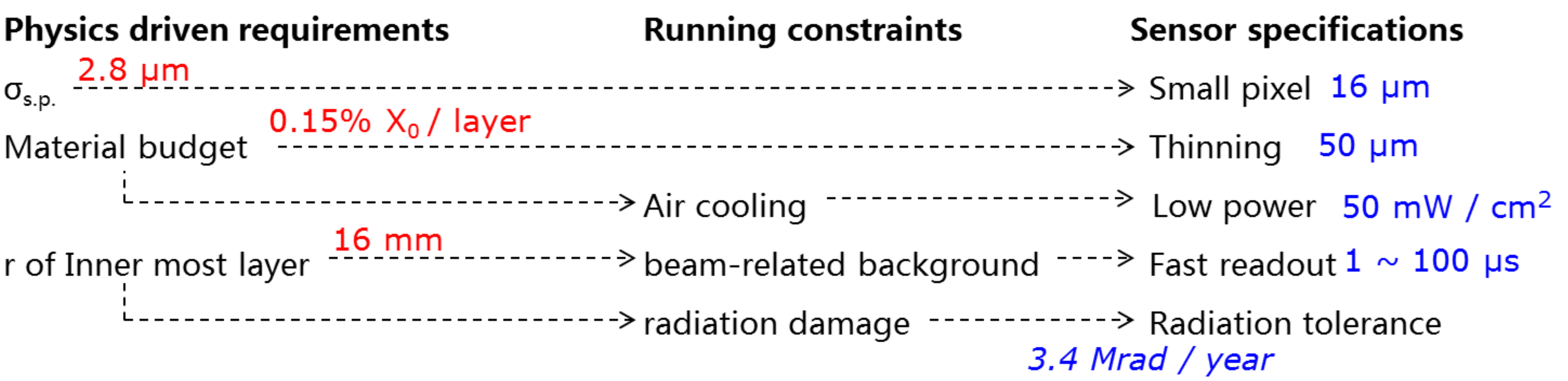
Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for ZH production, 160 GeV near W-pair threshold and 91 GeV for Z-pole.

Detector **occupancy < 1%**, assuming 10 µs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit.

CEPC CDR Volume II- Physics & Detector, IHEP-CEPC-DR-2018-02.

Pixel Sensor Specifications

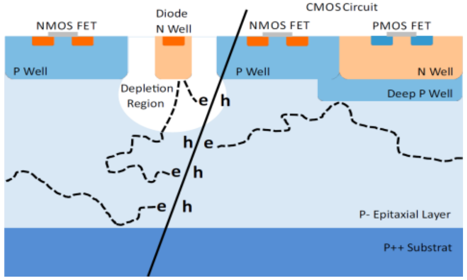
- **To achieve single point resolution**
  - Binary pixel ~ 16 μm
  - Analog pixel ~ 20 μm (higher power than binary pixel)
- **To lower the material budget**
  - Sensor thickness ~ 50 μm
  - Air cooling, heat load < 50 mW / cm^2
- **To tackle beam-related background**
  - Fast readout 1 ~ 100 μs/frame
  - 3.4 Mrad/year & $6.2\times10^{12} n_{eq}$ / (cm^2·year)?



Y. LU, CEPC workshop, Beijing, Nov. 2018.

Sensor Technology Options

- **HR-CMOS pixel sensor**
  - Relatively mature technology
  - Towards compete CMOS & thick sensitive layer, fully depleted substrate
  - More in-pixel functional circuitry → faster read-out & less power, radiation tolerance

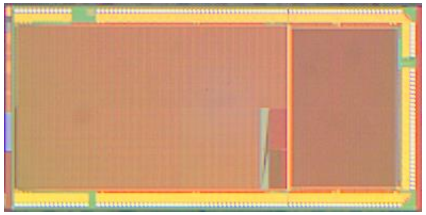


- **SOI pixel sensor**
  - Fully depleted HR substrate, potential of 16 μm pixel
  - Full CMOS circuit
- **DEPFET**
  - Possible application for inner most vertex layer
  - Small material budget, low power consumption in sensitive area
- **3D-IC**
  - Ultimate detector, but not mature enough

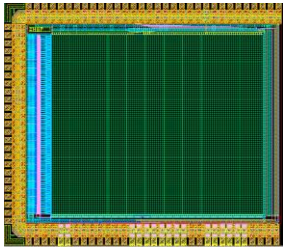
CMOS pixel sensor R&D activities

Developed CMOS Pixel Sensor prototypes

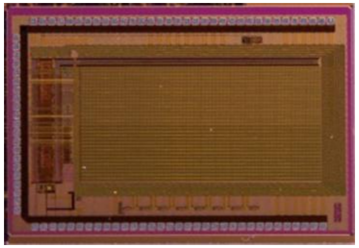
Prototype	Pixel size (μm^2)	Collection diode bias (V)	In-pixel circuit	Matrix size	R/O architecture	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer	96 × 160 192 × 128	Rolling shutter	In measurement
JadePix2	22 × 22	< 10 V	amp., discriminator	128 × 64	Rolling shutter	In measurement
MIC4	25 × 25	reverse bias	amp., discriminator	112 × 96	Asynchronous	In measurement



JadePix1 (IHEP)
3.9×7.9 mm^2



JadePix2 (IHEP)
3×3.3 mm^2



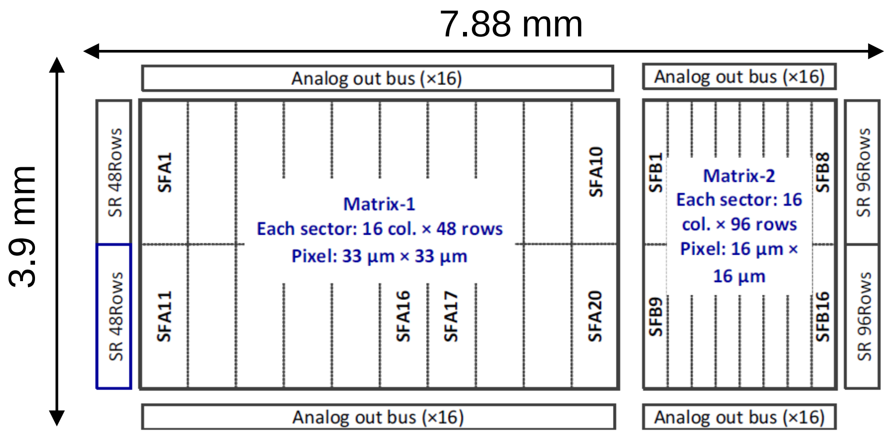
MIC4 (CCNU & IHEP)
3.2×3.7 mm^2

All prototypes in TowerJazz 180 nm process

Prototype JadePix-1 — design

IHEP Team

- **Design goals：sensor optimization and radiation study**
- **A variety of sensor geometries**
  - Matrix-1 with 33 × 33 μm^2 pixels (except one sector SFA20 with 16×16 μm^2 pixels), including 16 variations
  - Matrix-2 with 16×16 μm^2 pixels, including 12 variations
- **Different pixel structures**
  - DC-coupled sensor with source follow: 2T/3T structure
  - Pixel with pre-amplifier
  - AC-coupled pixels
- **Analog readout**
  - Each pixel array has16 analog outputs in-parallel
  - Each array read out in rolling shutter mode



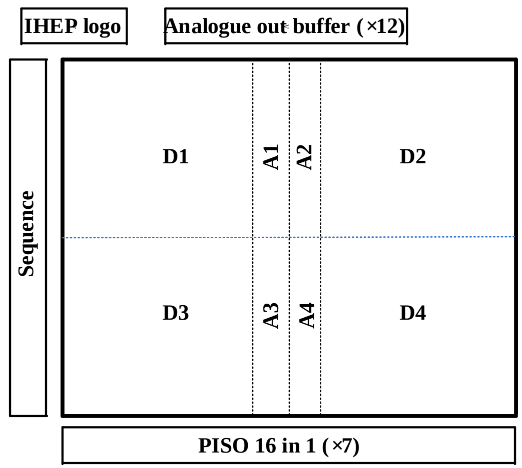
JadePix-1 has been fully characterized with radioactive sources and test beam

Details will be presented by L. Chen in this session

Prototype JadePix-2 — design

IHEP Team

- **Chip overview:**
  - 3 × 3.3 mm^2
  - 96 × 112 binary pixels with 8 sub-matrix
  - Rolling shutter read out mode
    - 100 ns / row (Version 1), 80 ns / row (Version 2)
    - 3.7 μA / pixel (Version 1), 6.5 μA / pixel (Version 2)
  - Every 16 columns share one output port
    - through the Parallel-In Serial-Out block
  - LVDS transmitter @160 MHz clock
  - A few columns configured as analog readout
    - For calibration of sensing diode



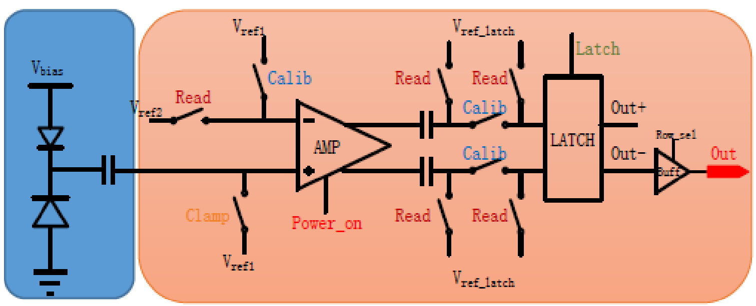
Floorplan of JadePix2

	D1	A1	A2	D2	D3	A3	A4	D4
Diode size	4 μm^2				8 μm^2			
Design Version	2: Single-end		1: Differential		2: Single-end		1: Differential	
Matrix size: ①48 row×44 col. ②48 row×4 col. ③48 row×60 col.	①	②		③	①	②		③

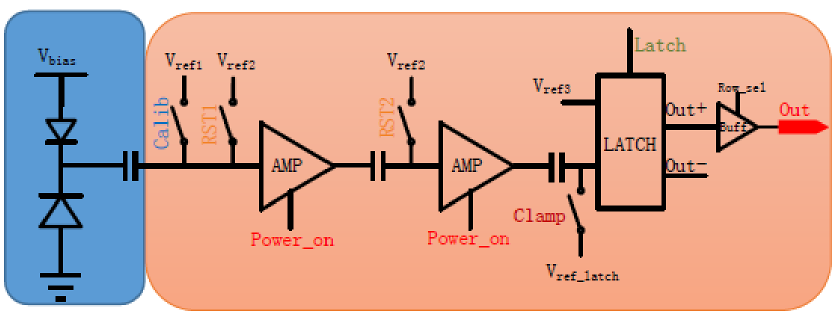
Prototype JadePix-2 — design

IHEP Team

- **Pixel size: 22 × 22 μm²**
- **Two versions of front-end**
  - Version 1: differential amplifier + dynamic latch
  - Version 2: single-ended amplifier + dynamic latch
- **Offset cancellation and high precision comparator**
  - FPN (Fix Pattern Noise) ~ 20 e-
  - TN (Temporal Noise) ~ 7 e-



Version 1: differential amplifier + latch



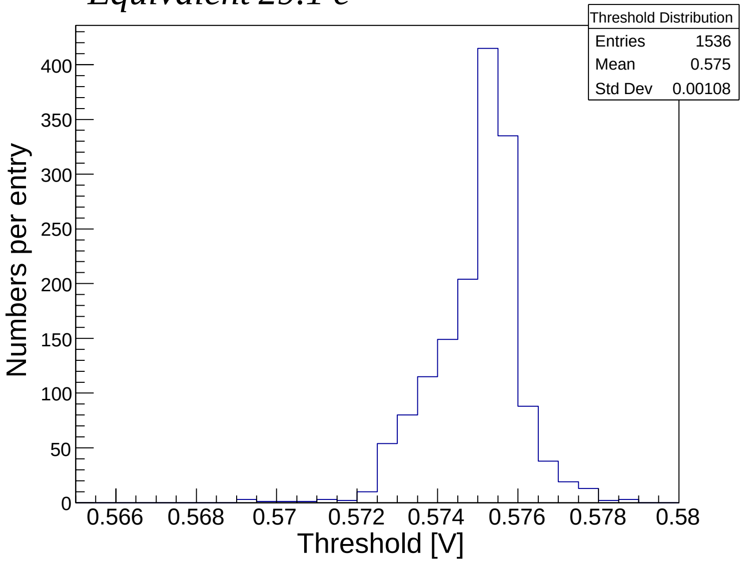
Version 2: two stage common source amplifiers + latch

Prototype JadePix-2 — test results

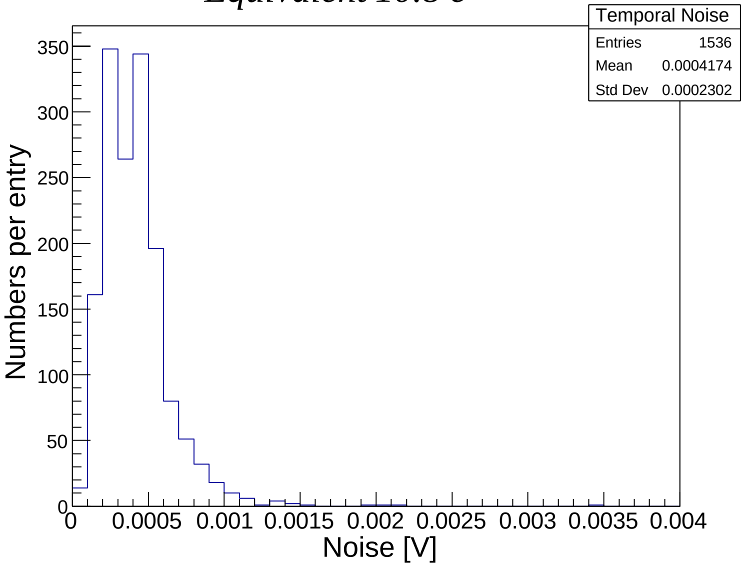
IHEP Team

- **S-curve measured on Version 1 pixels (differential)**
- **ENC = 31 e-**
  - TN ~ 11 e-
  - FPN ~ 29 e-

FPN: 1.08mV @input node
Equivalent 29.1 e⁻



TN: 0.4mV @input node
Equivalent 10.8 e⁻

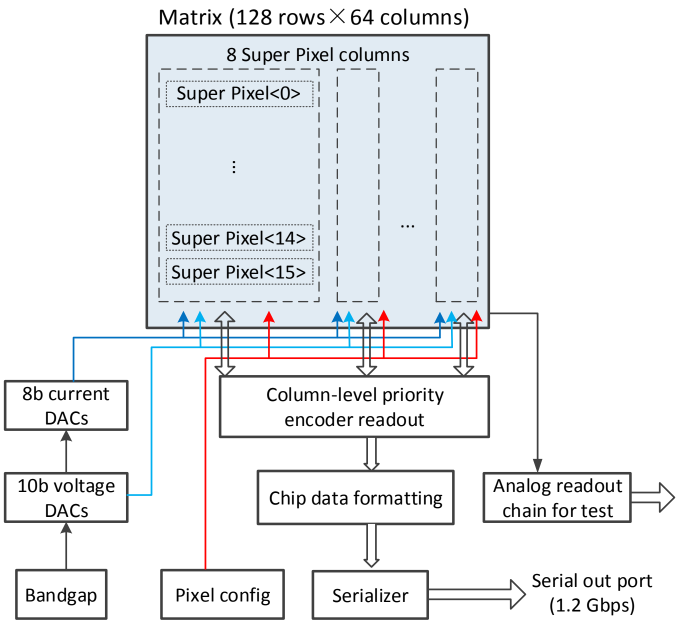


Test with radioactive sources in progress

Prototype MIC4 — design

CCNU Team

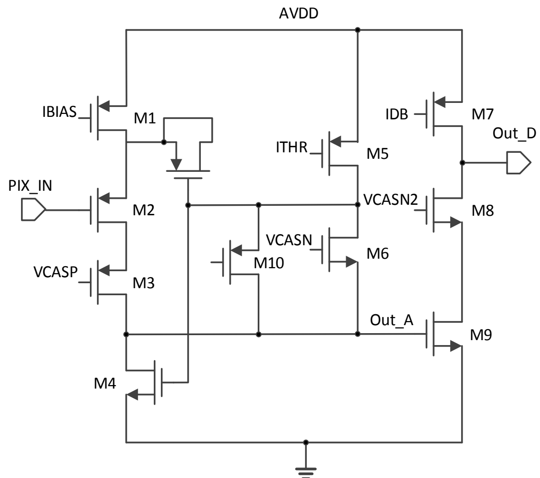
- **Overview:**
  - Die size: 3.1 × 4.6 mm^2 ,
  - Matrix of 128 rows× 64 columns binary pixels
  - Pixel size 25 μm × 25 μm
  - Readout speed: 25 ns/pixel
  - Matrix power < 20 mW/cm^2
  - Two versions of pixel front-end
    - Low power, compact layout, active continuously
  - Data driven readout
    - No memory in this version
    - High speed data link of 1.2 Gbps
  - Possible to apply a reverse bias voltage to the substrate
    - Larger depletion volume
    - Lower sensor capacitance
    - ➔ Increase S/N

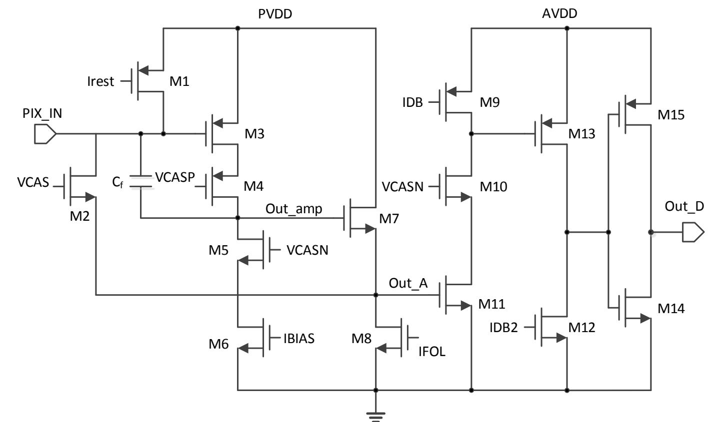


Prototype MIC4 — design

CCNU and IHEP Team

- **Two versions of the in-pixel front-end:**





- **Version 1:**
  - Same structure as ALPIDE chip (for ALICE ITS upgrade)*, with different parameters
  - Peaking time < 1 μs, pulse duration < 3 μs, with power cons. of 110 nW/pixel
  - ENC: ~ 10 e-
  - Area: ~ 25 × 9.3 μm²

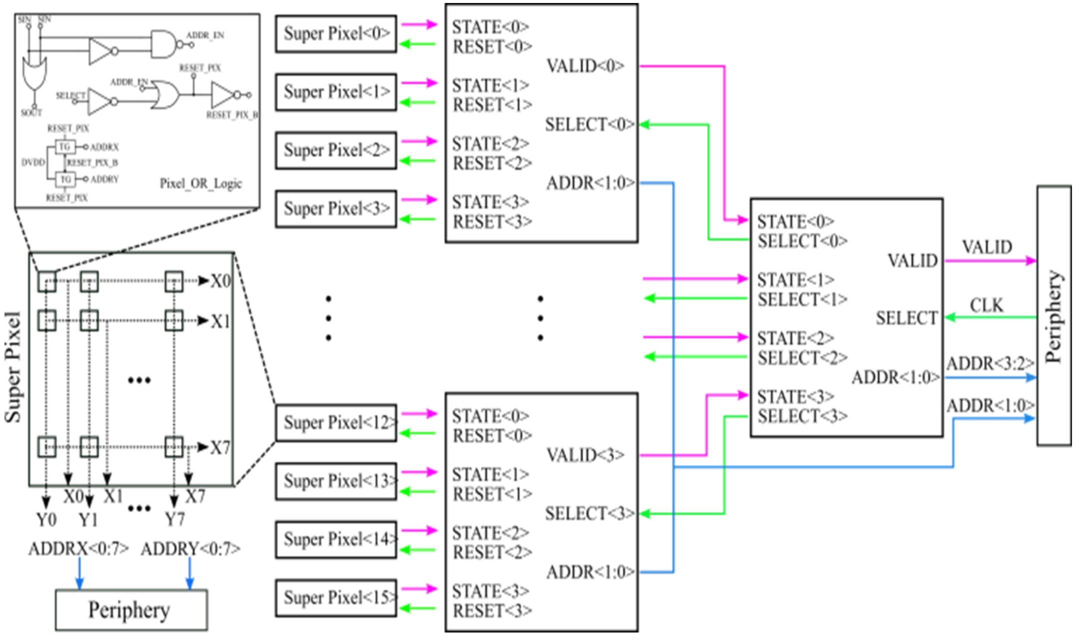
- **Version 2:**
  - CSA based front-end, with a very low feedback capacitance
  - Peaking time < 1 μs, with power cons. of 50 nW/pixel
  - ENC: ~ 24 e-
  - Area: ~ 25 × 9.3 μm²

**Ref: D. Kim et al., 2016 JINST 11 C02042*

Prototype MIC4 — design

CCNU Team

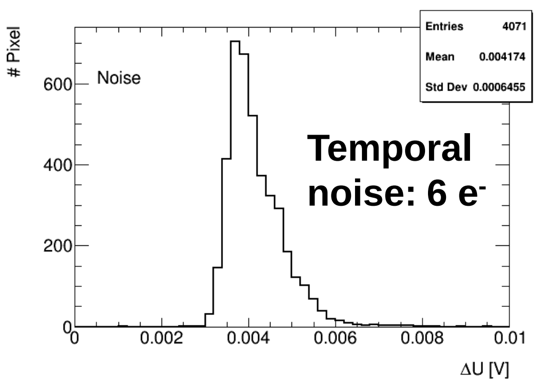
- **Matrix read-out:**
  - **Data driven** ➔ very low power consumption
  - **Zero-suppression** readout architecture: OR-gate chain & Address Encoder and Reset Decoder (AERD) combination ➔ for highly compact pixel & fast readout & low power
  - **OR-gate chain inside a super pixel** (8×8 pixels) to do the zero-suppression, two dimension projection (ADDRX & ADDRY) to identify the hit pixel ➔ save pixel logic and address lines area
  - **AERD between one column of the super pixels** ➔ save power and readout time

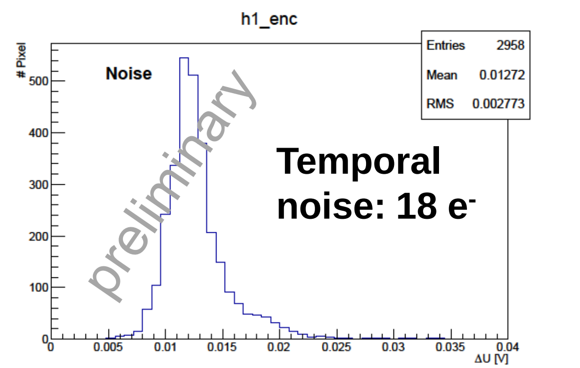


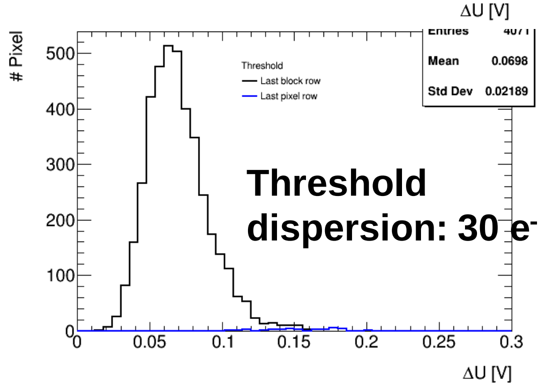
Prototype MIC4 — test results

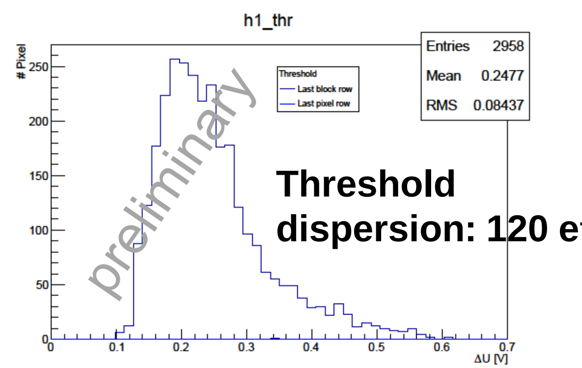
CCNU and IHEP Team

- **Pixels with front-end version 1:**
  - Analog power: ~24 mW/cm^2
  - Average noise ~6 e-
  - Average threshold dispersion 31 e-, factor ~7 higher than simulation
- **Pixels with front-end version 2:**
  - Analog power: ~8 mW/cm^2
  - Average noise ~18 e-
  - Average threshold dispersion 120 e-, factor ~8 higher than simulation







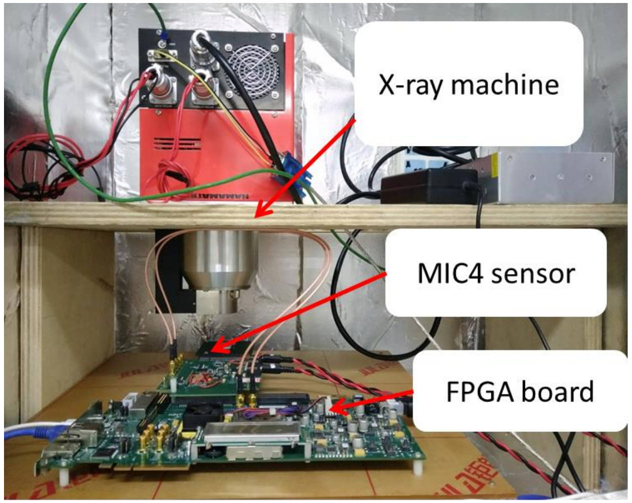


Increase in threshold spread under investigation

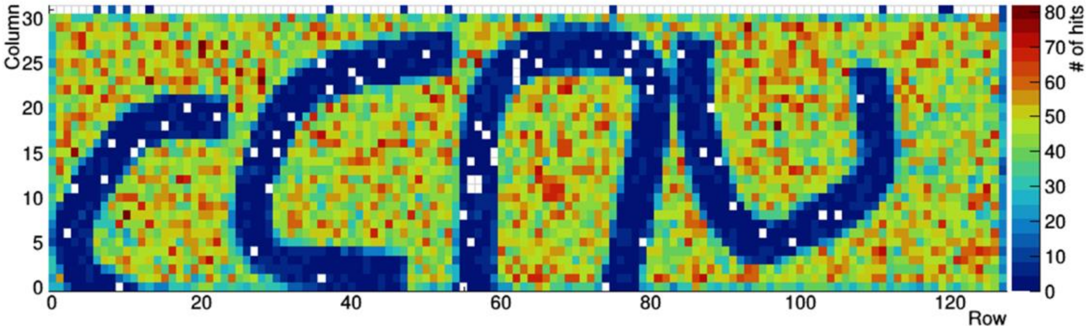
Prototype MIC4 — test results

CCNU Team

- **X-ray source imaging test: using 6 KV, get picture of "ccnu" (ccnu are copper wires)**



X-ray test platform



X-ray image of "ccnu"

Test with radioactive sources in progress

Summary and Outlook

- **Pixel detector with high spatial resolution, low power and fast readout is required for the CEPC vertex detector**
- **Three prototypes have been designed and characterized in lab**
  - The binary pixels with low-power front-end and small area are implemented
  - Two sensor readout architectures are developed in parallel
  - Shows promising results in terms of front-end performance and readout capability
    - Improvement in threshold dispersion needed
  - Characterization of the JadePix-2 and MIC4 on-going
- **Optimization study of vertex system needed**
- **Coordination of design team for next submissions**
  - Design of prototype with large pixel matrix
  - Novel readout scheme exploration in progress
- **Radiation hardness design**

ACKNOWLEGMENTS

IHEP team :

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CCNU team:

C. Gao, X, Huang, Y. Li, J. Liu, W. Ren, X. Sun, B. You, L. Xiao, P. Yang, D. Zhang, L. Zhang, W. Zhou

Thanks for your attention !

Backup slides

CEPC Schedule (ideal)

- design issues
- R&D items
- preCDR

- CDR, funding
- R&D program
- Intl. collaboration
- site study

- seek approval, site decision
- construction during 14th 5-year plan
- commissioning

- CEPC data-taking starts before the LHC program ends around 2035
- possibly con-current, and complimentary to the ILC

Ref: CEPC workshop, X. LOU, Nov. 2018, Beijing, China.

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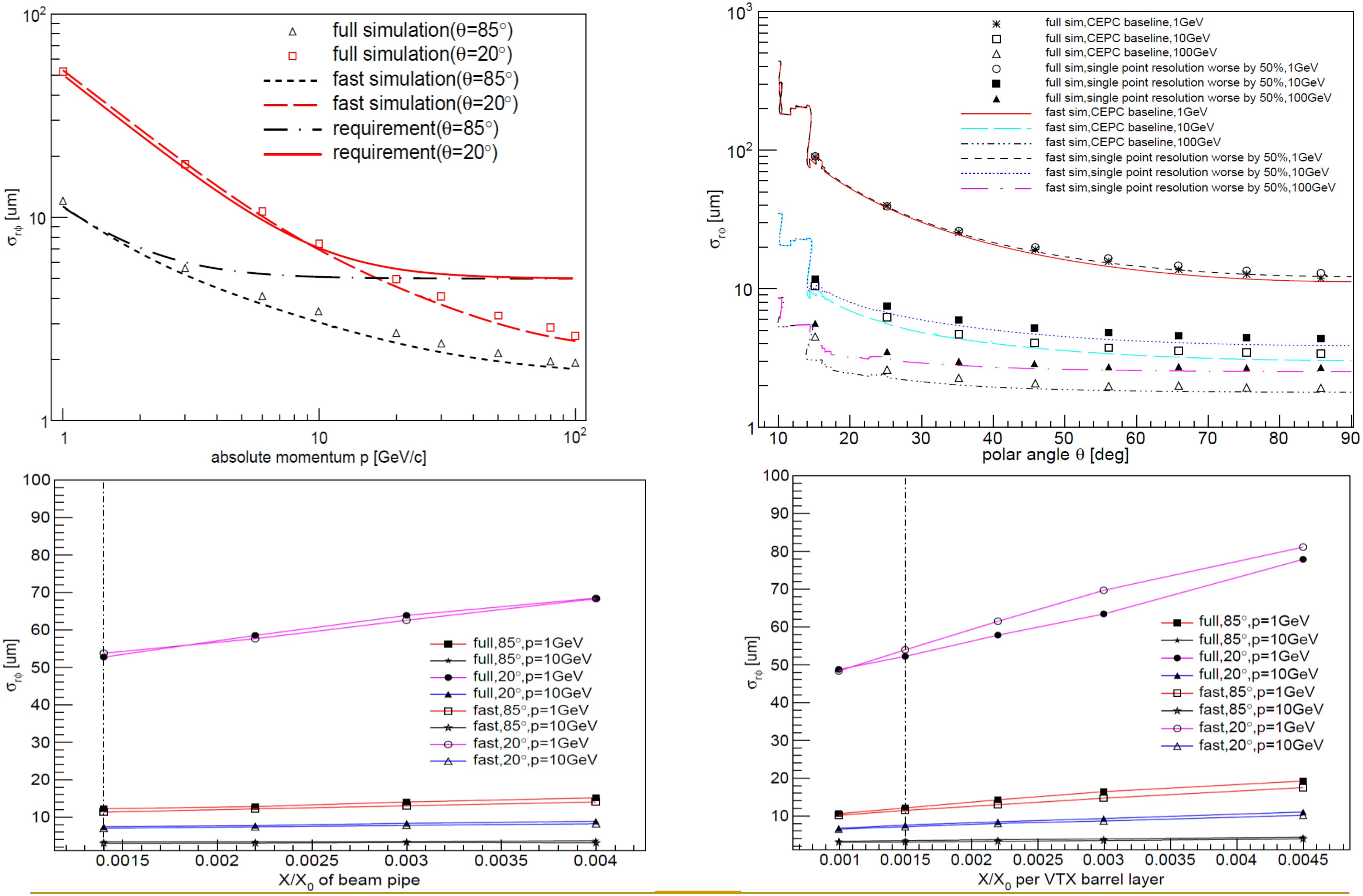
Performance Studies — IP Resolution



Detector Concepts

- **Baseline detector concept**
  - Silicon tracker + TPC
    or Full Silicon Tracker
  - High granular calorimetry system
  - 3 Tesla solenoid
  - Muon detector

- **Alternative detector concept, IDEA**
  - Silicon pixel + Drift Chamber
  - 2 Tesla solenoid
  - Dual readout calorimeter
  - Muon chamber