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Development of CMOS pixel sensor prototypes for the CEPC vertex detector

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The Circular Electron Positron Collider (CEPC) is proposed as a Higgs factory, targeting a high precision study of the properties of the Higgs boson. To achieve the required sensitivity of experiment, the CEPC vertex detector should provide unprecedented position resolution with very low material budget, and low power consumption. CMOS Pixel Sensors (CPS), as one of the promising candidate technologies, has been studied within the R&D activities for the CEPC vertex detector. This talk introduces the development of CPS prototypes in a 180 nm CMOS Image Sensor process. We will present the detailed design of three prototypes: JadePix1, JadePix2 and MIC4. The JadePix1 consists of 36 pixel sub-matrices, each one containing several versions of analog pixel design. The JadePix2 and MIC4 chips both feature digital pixels and differ essentially by their different readout schemes. The JadePix2 employs the rolling shutter readout approach, which allows for small pixels ($22 \times 22 \ \mu m^2$). The MIC4 is based on a data-driven readout architecture, and is particularly suited to the ambitionned readout speed and power consumption. The chip characterizations of JadePix2 and MIC4 will be also reported.

Primary authors: ZHANG, Ying (IHEP); YANG, Ping (CCNU)

Co-authors: ZHOU, Yang (IHEP); LU, yunpeng (IHEP); ZHANG, Dongliang (CCNU); LIANG, Zhijun (Chinese Academy of Sciences (CN))

Presenters: ZHANG, Ying (IHEP); YANG, Ping (CCNU)

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