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Pixel array for 3-D integration with an intra-cortical electrode array.

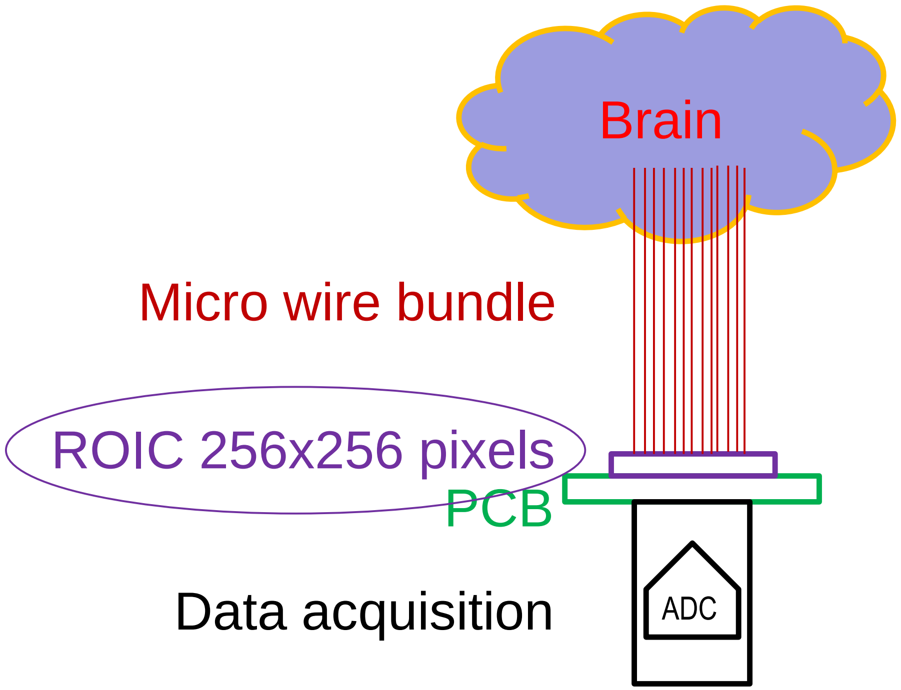
B.Dierickx[1], P.Gao[1], A.Babaiefishani[1], S.Veijalainen[1], W.Wang[1], B.Luyssaert[1], A.Khan[2], R.Edgington[2], K.Sahasrabuddhe[2], M.Angle[2]

[1] Caeleste, Mechelen, Belgium

[2] Paradromics, San Jose, US

Outline

1. Introduction, purpose
   ⇒Direct extracellular neuron signal sensing
   ⇒Our approach
2. Pixel design & performance
   ⇒Sense amplifier design
   ⇒Measured performance
3. Future outlook
   ⇒In-pixel analog domain filtering
   ⇒Prototype results



1. Introduction: purpose

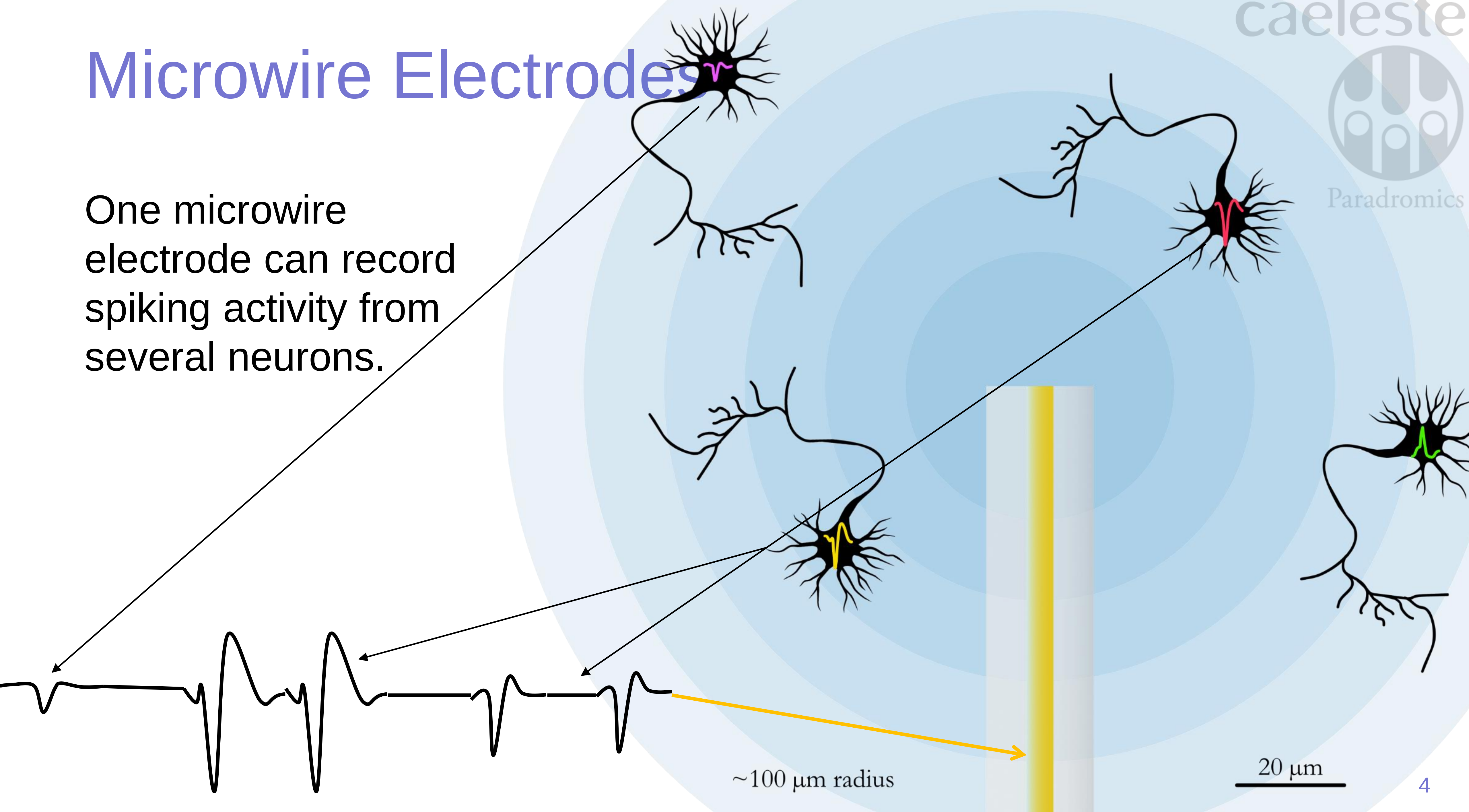
Detecting neural events in the brain

→ **by an array of microelectrodes connected to an array of voltage amplifiers**

→ **like a large channel count oscilloscope with 10µV 20kHz resolution**

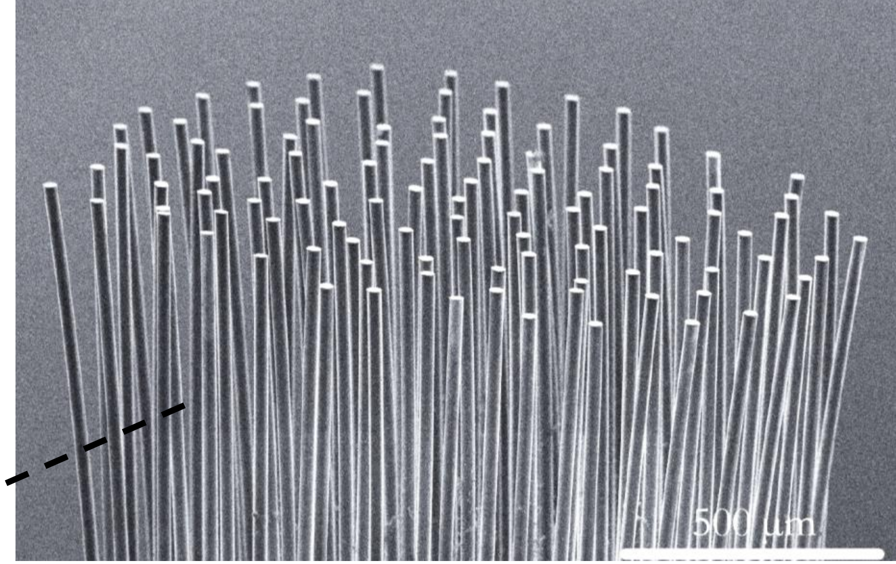
Microwire Electrodes

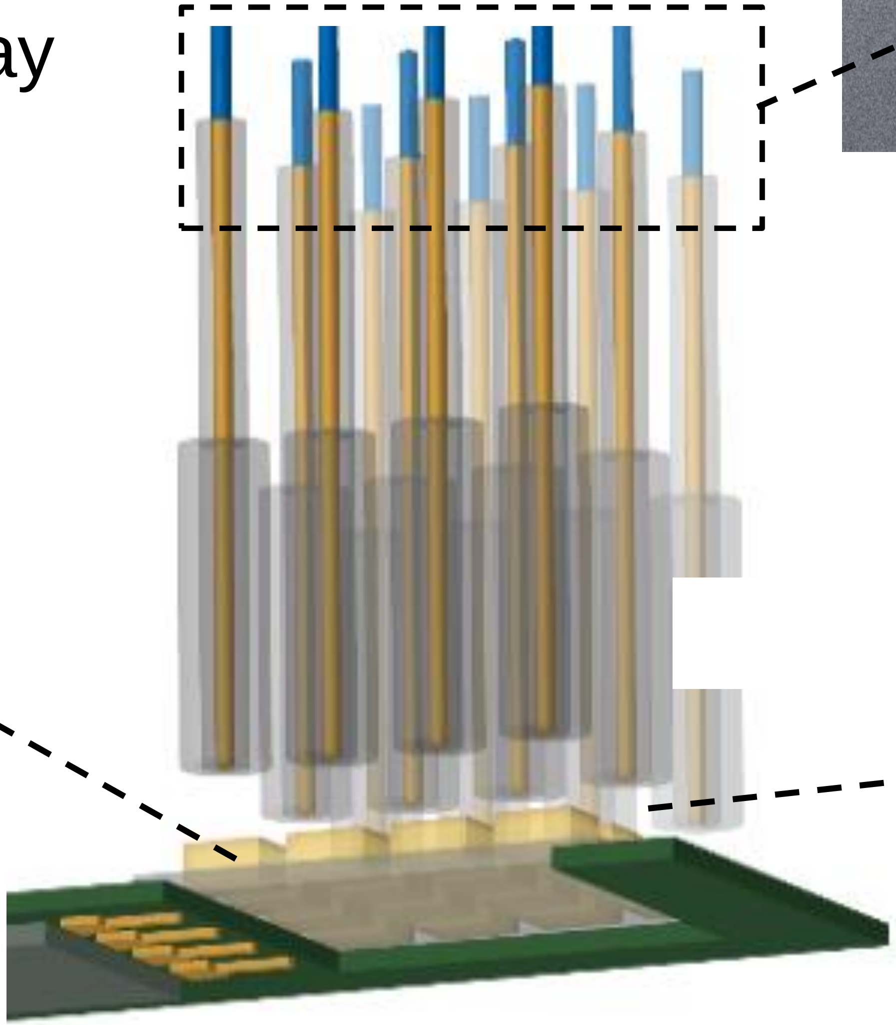
One microwire electrode can record spiking activity from several neurons.

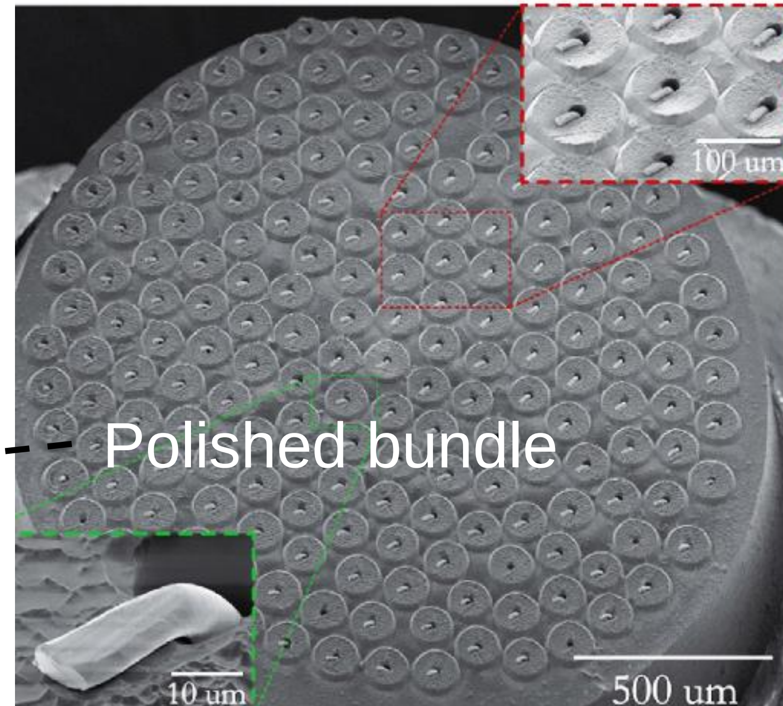


Recording from microwire electrodes

Connecting microwires directly to a CMOS array allows for readout, digitization,
and multiplexing.

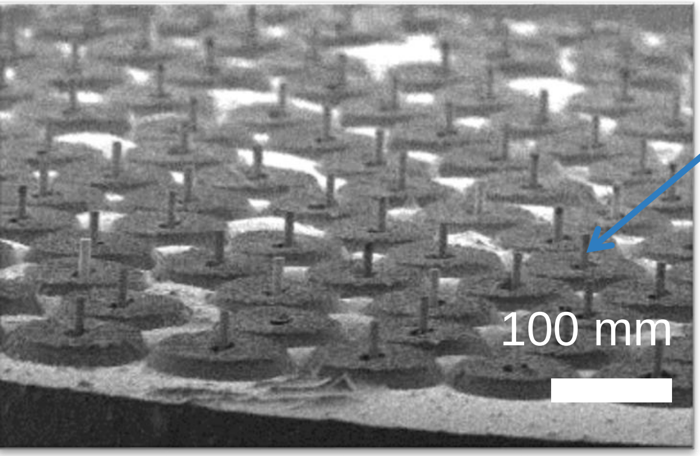


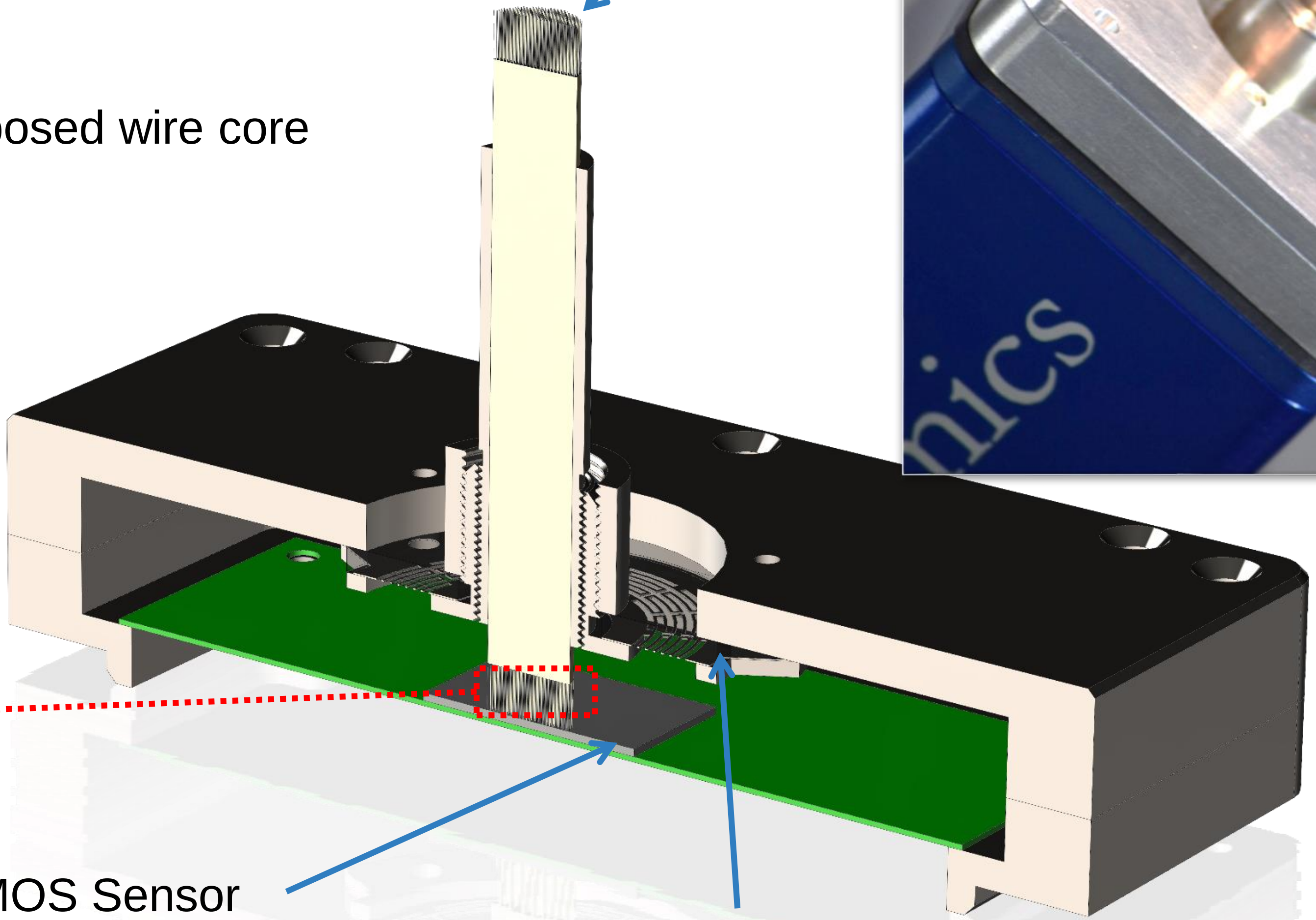


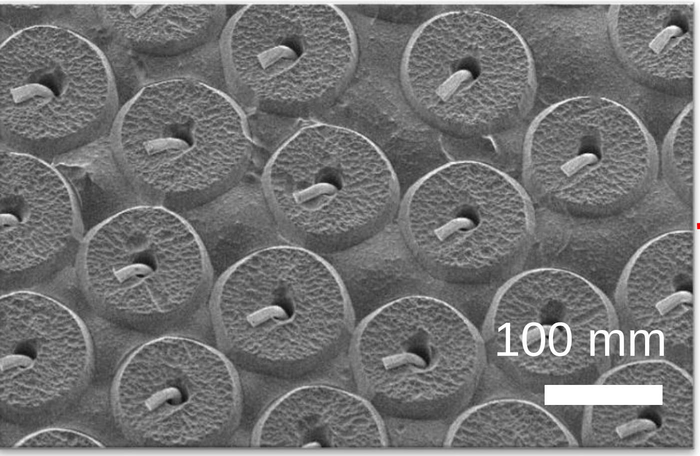


Press the bundles onto CMOS sensor

Bundle before Pressing

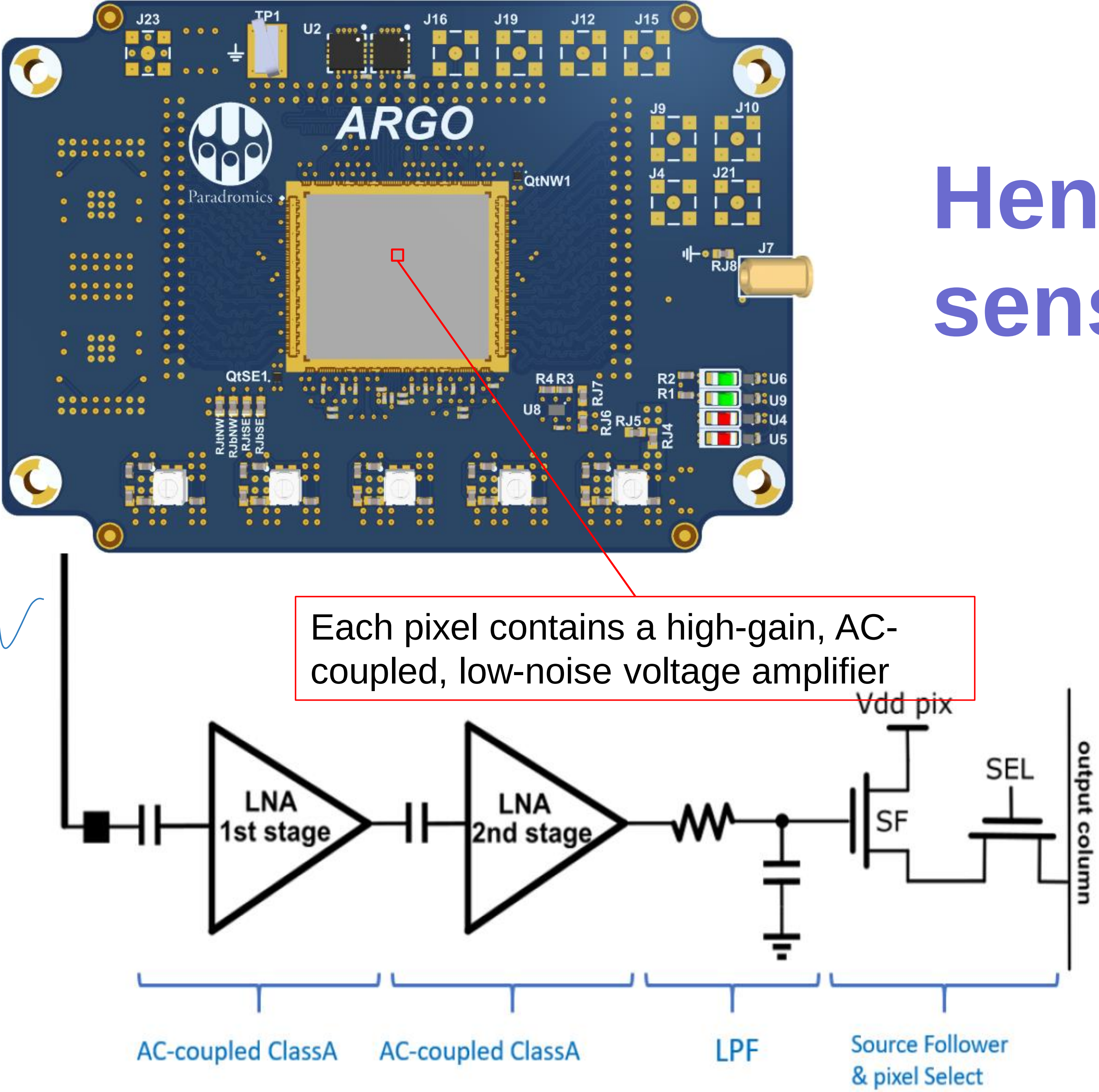






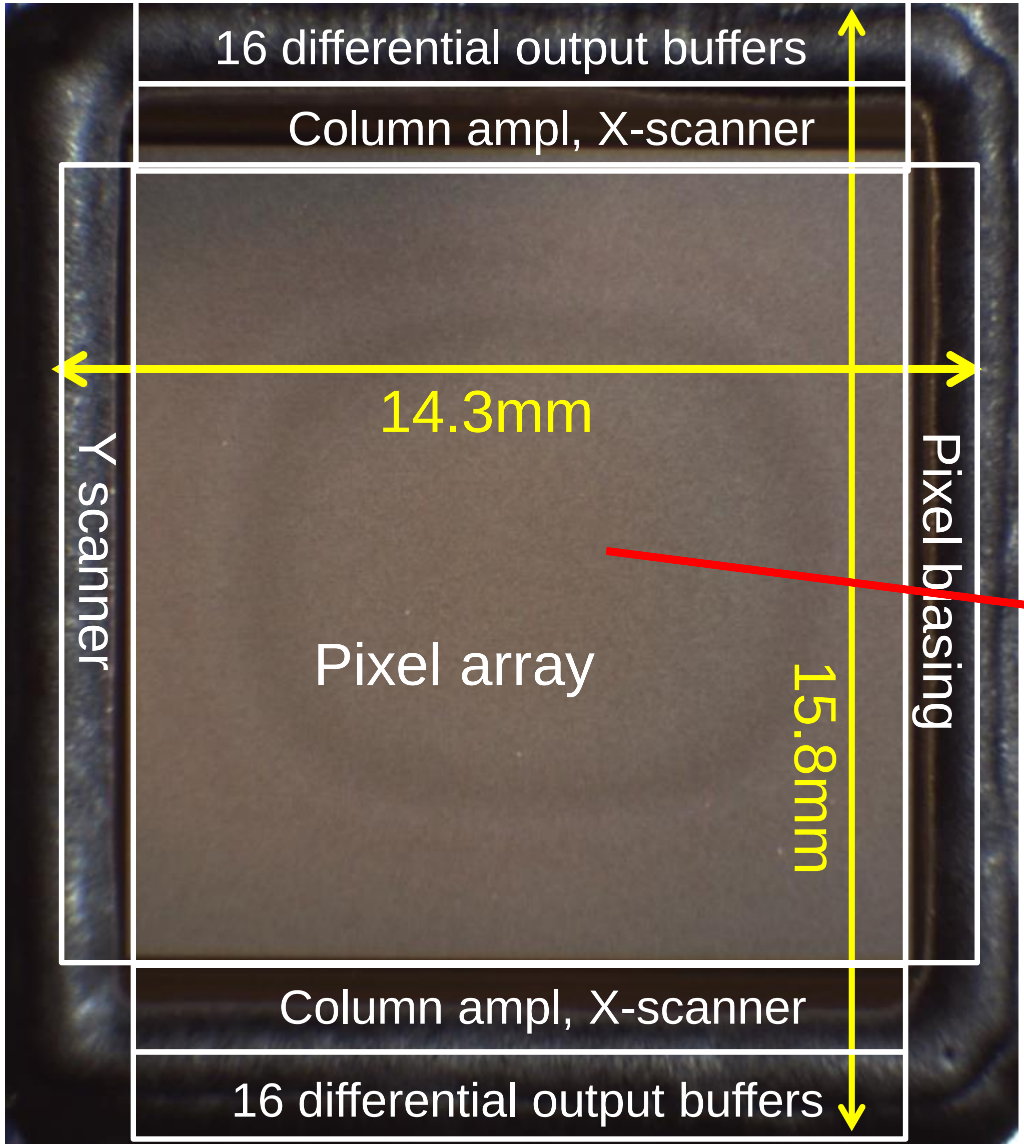
Bundle after Pressing

Henry/Argo sensor array

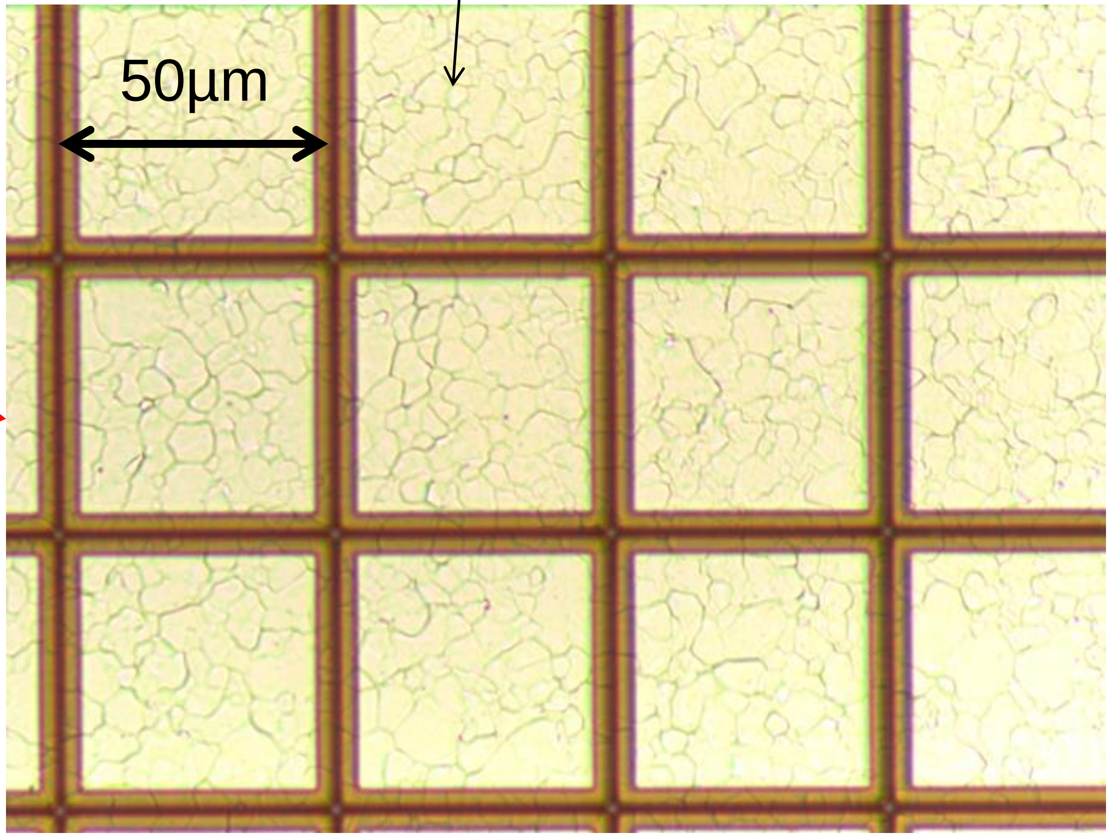


Parameters	Specifications
# of neural sensors	65,536 (256x256)
Full frame readout	up to 39,000 frames/s on 32 analog outputs
Input referred noise	< 10 µVrms (100 Hz- 20 kHz)
Voltage gain	100 – 800 V/V
Input impedance	> 1 TΩ
Pixel pitch	50 mm

Henry



Top electrode to be hybridized to the microwire electrode

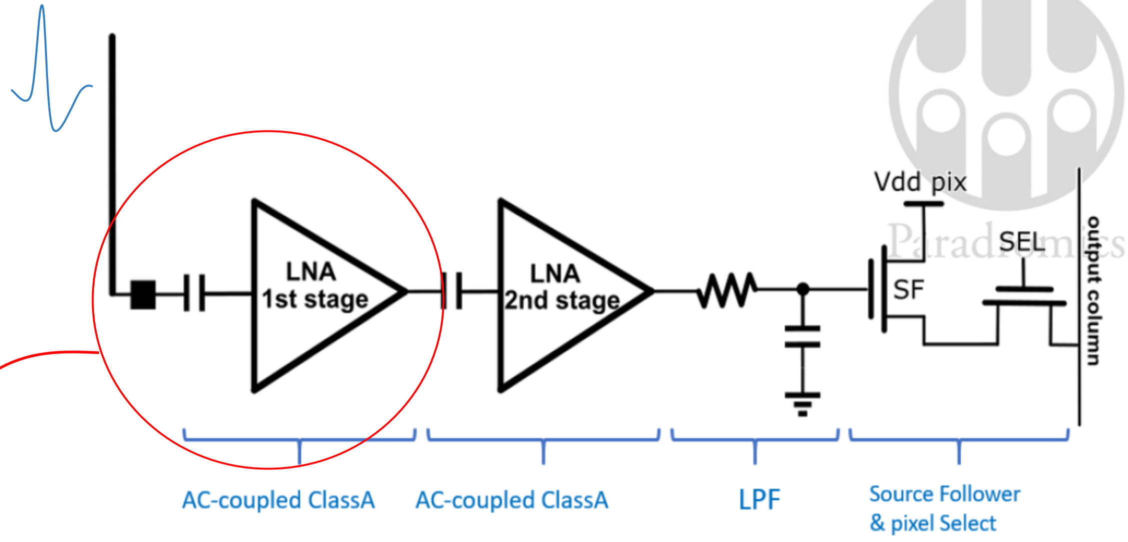


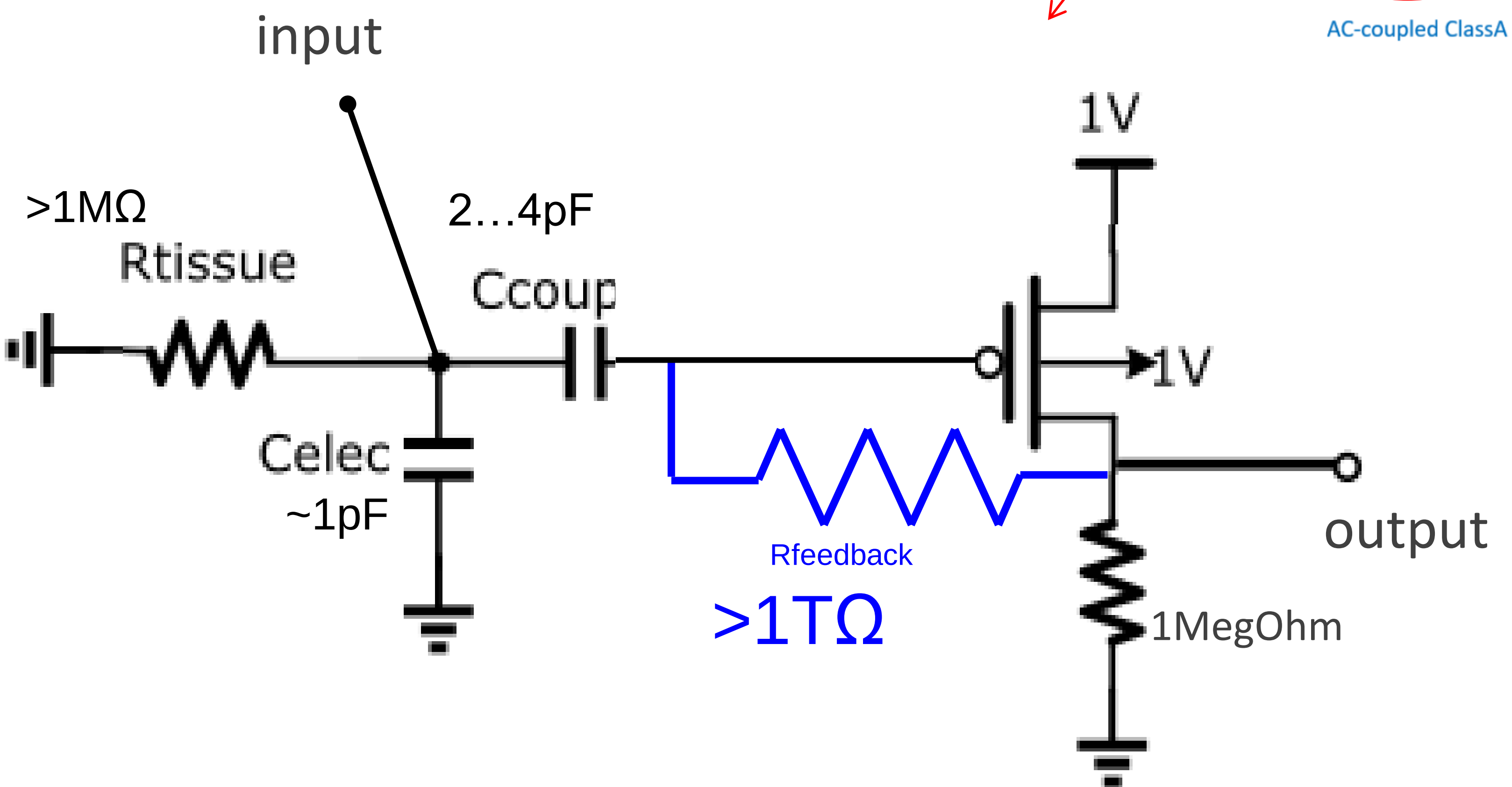
2. Pixel design & performance

→ overall pixel topology
→ design for compactness & for low noise
→ sense amplifier
→ pixel layout
→ measured performance in the array

Class-A amplifier with resistive self-biasing

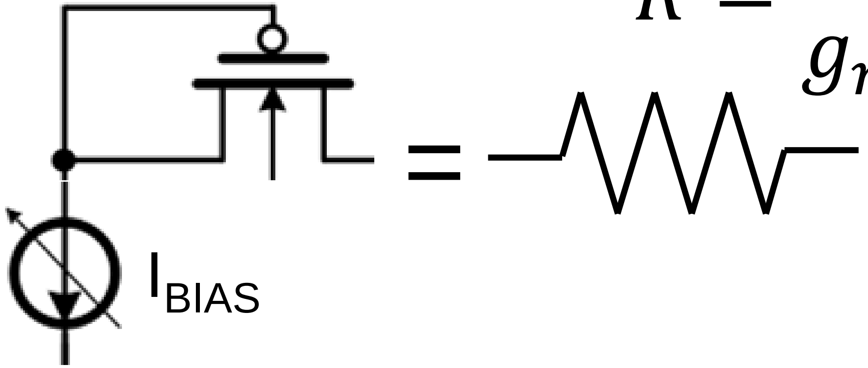
Optimized for 1/f noise: single PMOSFET

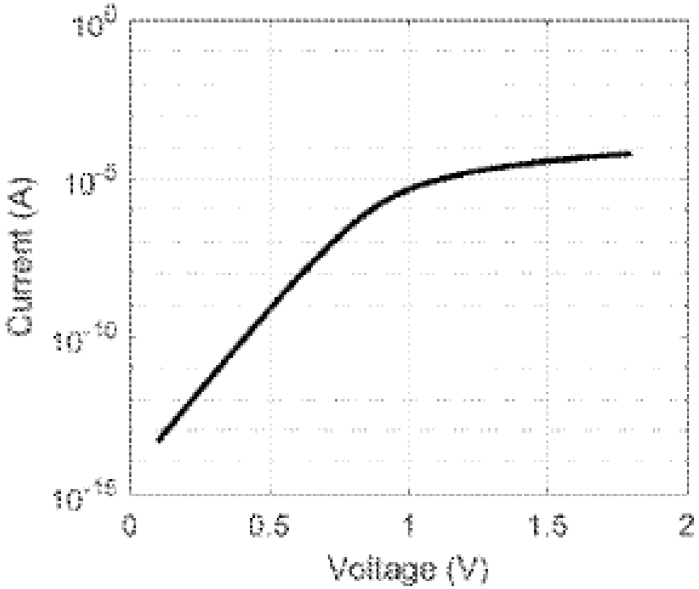


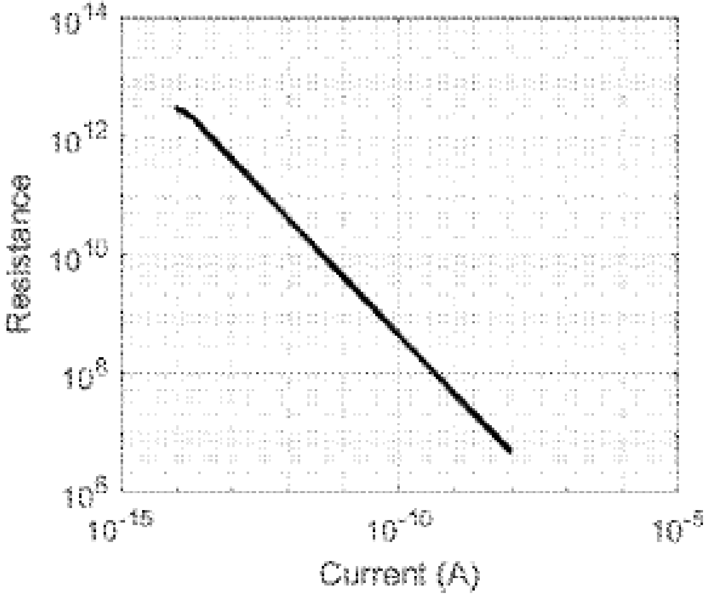


Compact high value resistor

$$R = \frac{1}{g_m} = \frac{kT}{q.I_{BIAS}}$$







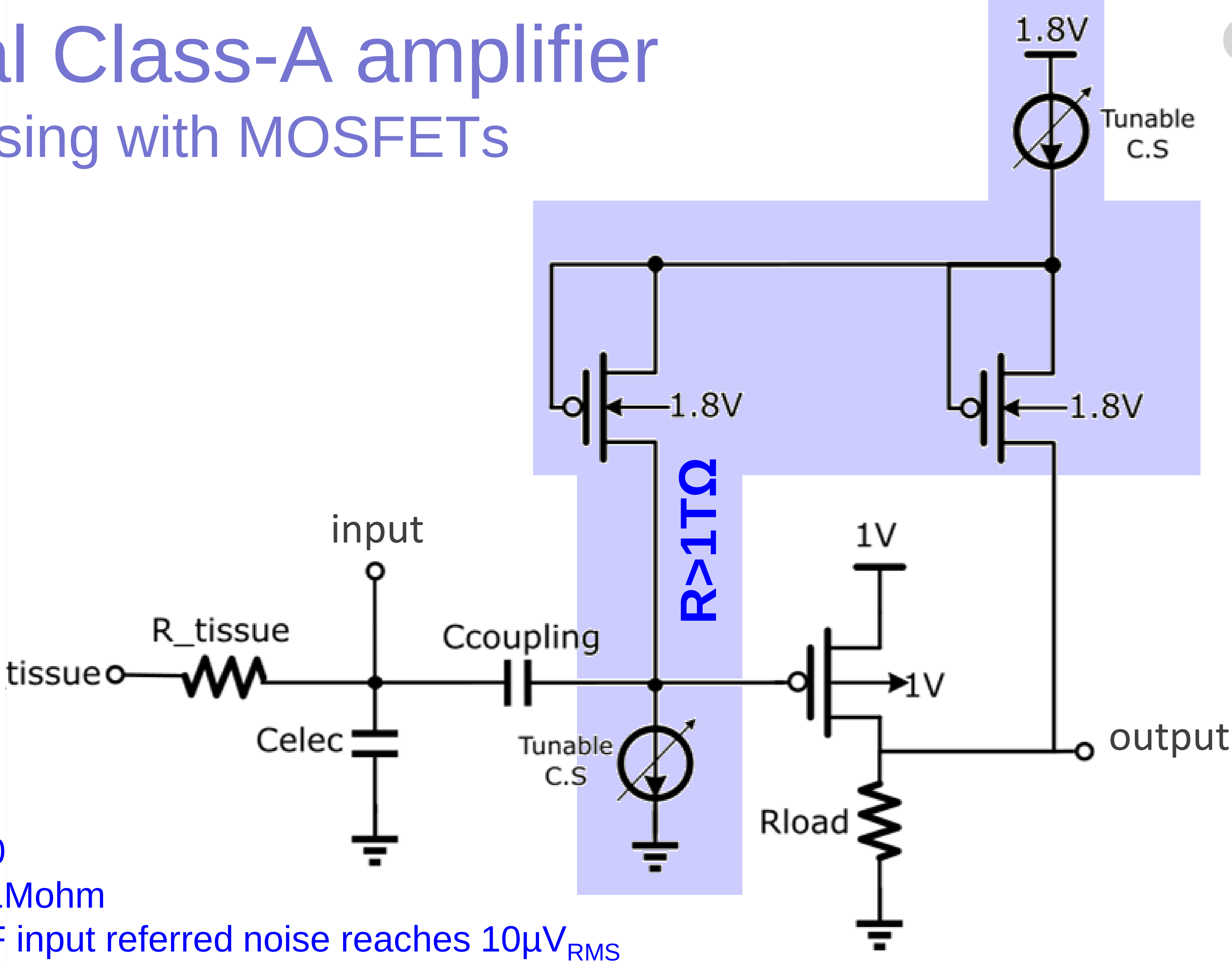
PRO

- Compact: a diode-connected MOSFET + a MOSFET bias current source
- $R=1/g_m$ AC value hardly dependent on variability of the 1st MOSFET. Dependent on the variability of the bias
- Can make extremely high R
  e.g. 1TΩ for I_{BIAS}=25fA.
  Needed to make very low RC time:
  1TΩ*100fC=0.1s

CON

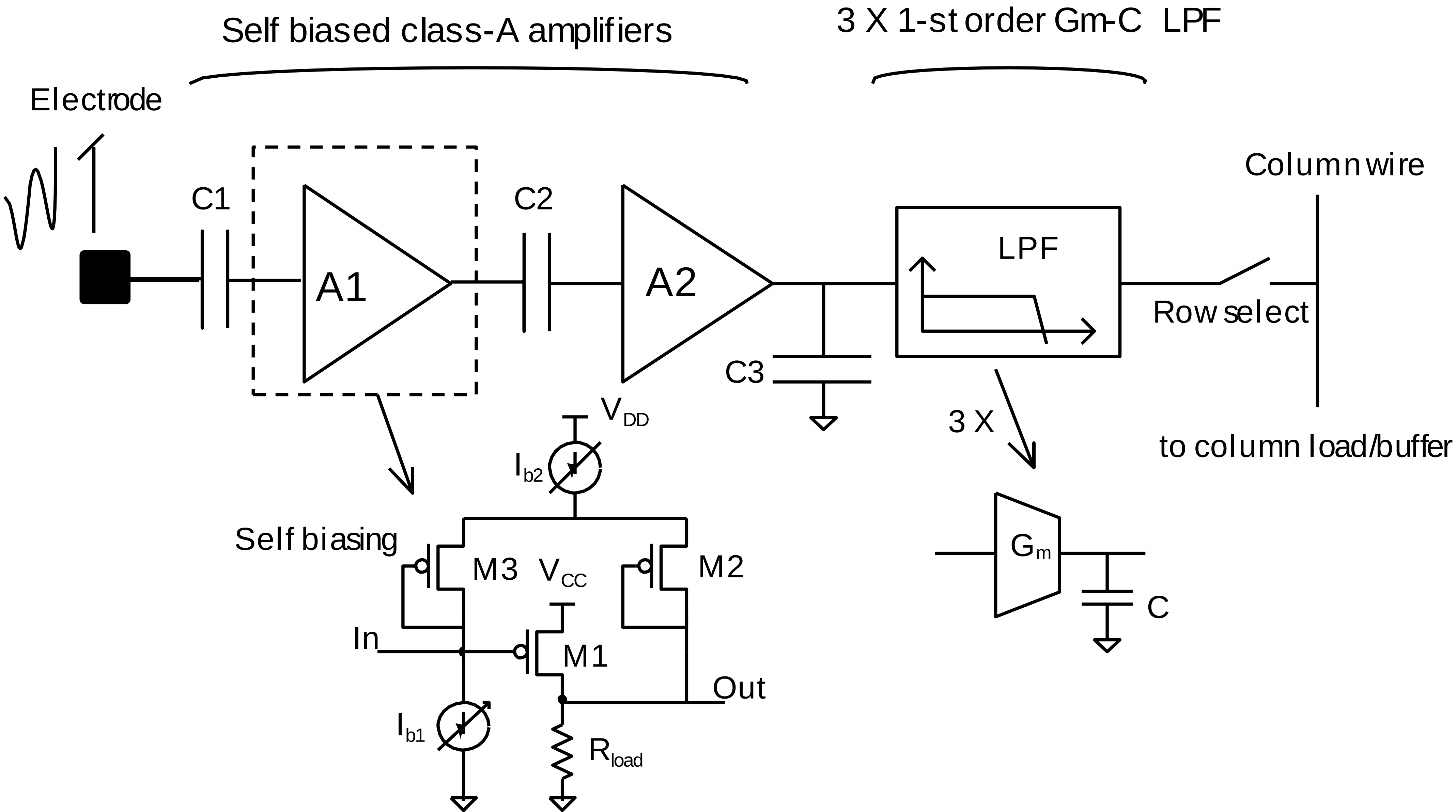
- Needs an exclusive DC path for the I_{BIAS}
- Only AC / small signal: << 100mV
- Not very linear
- Offset must be solved by AC coupling
- 1/f noise

Actual Class-A amplifier
self-biasing with MOSFETs

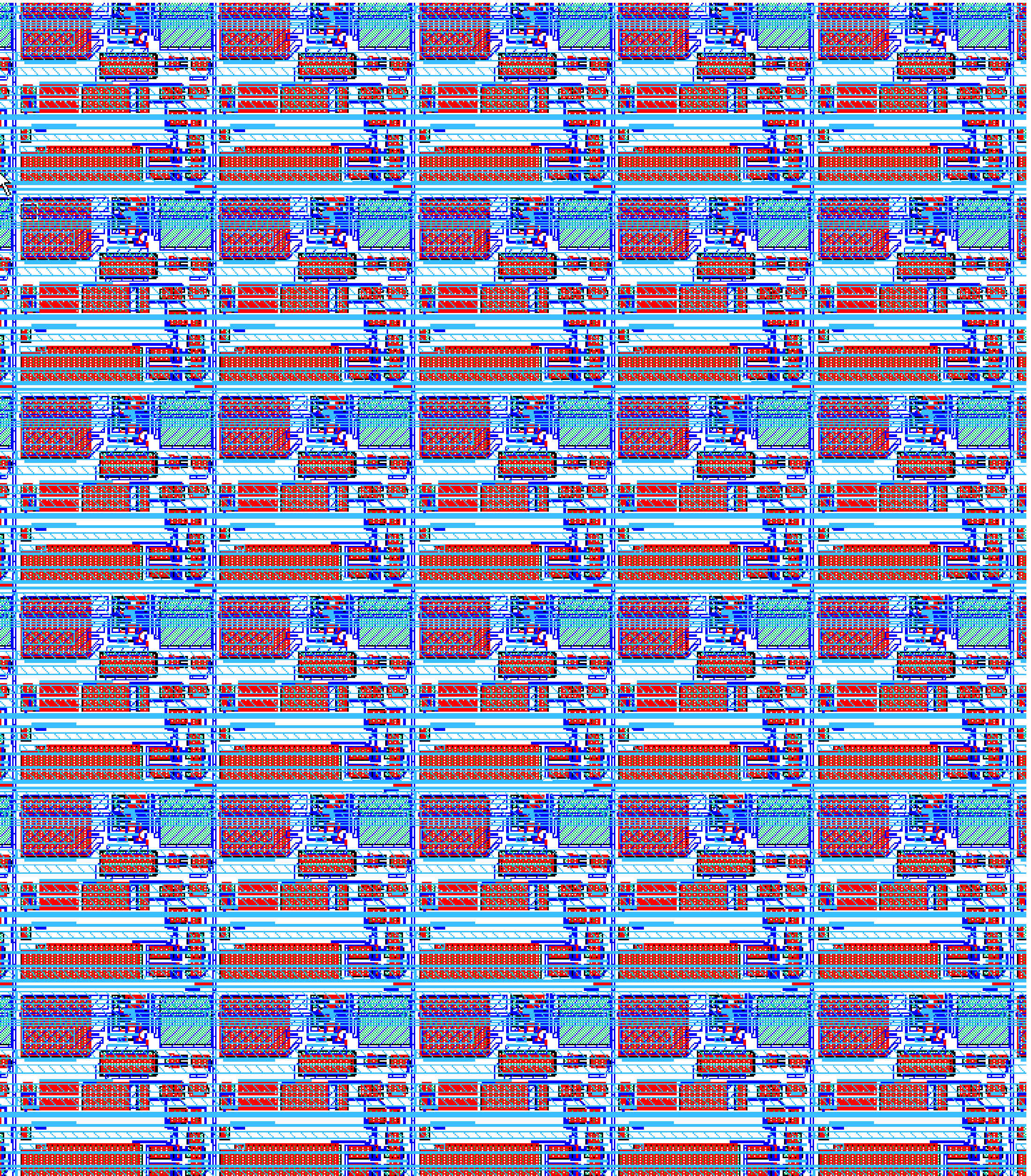


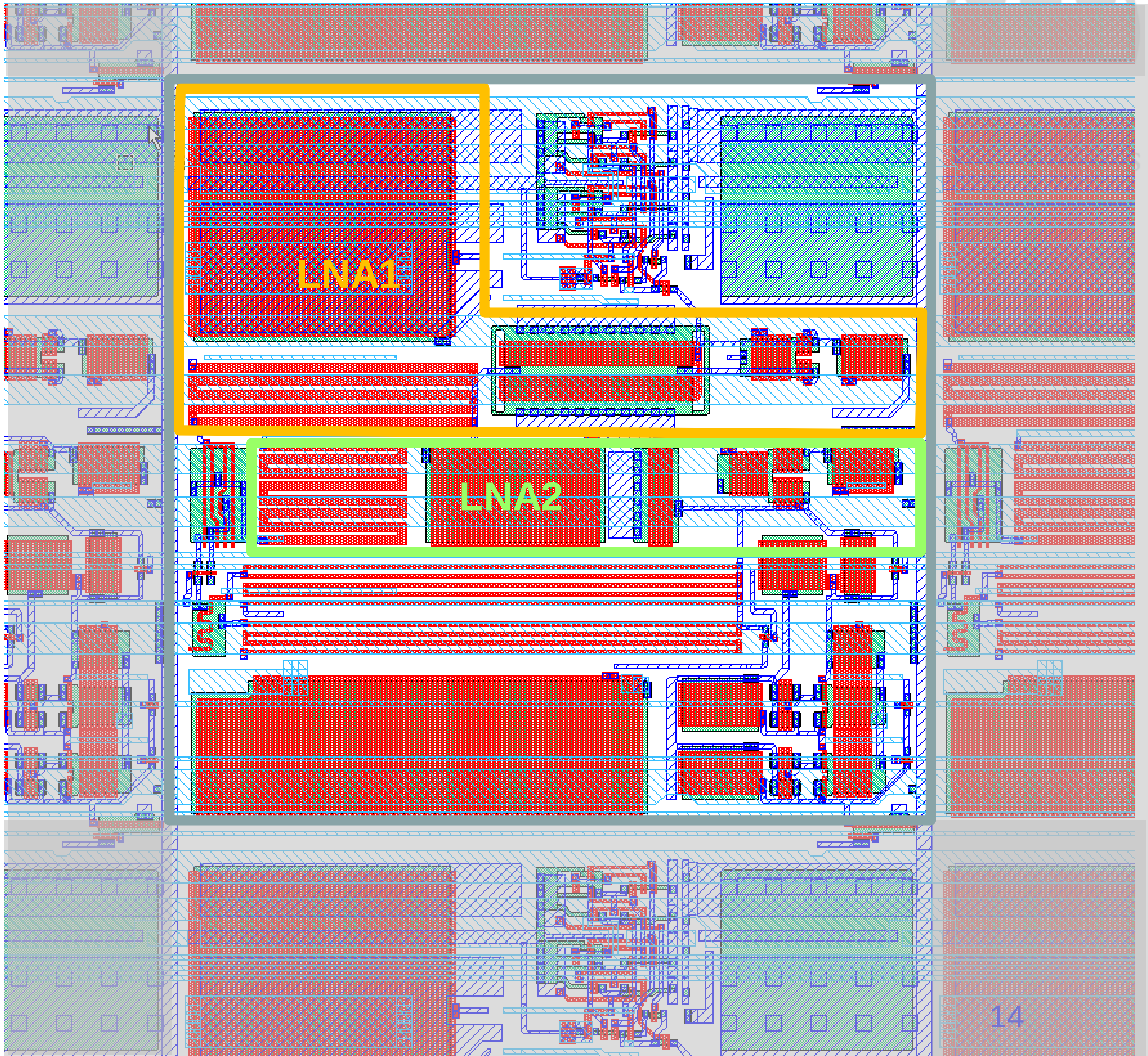
- Gain = 10
- Rload = 1Mohm
- LNA+LPF input referred noise reaches $10\mu V_{RMS}$

Actual Henry pixel topology

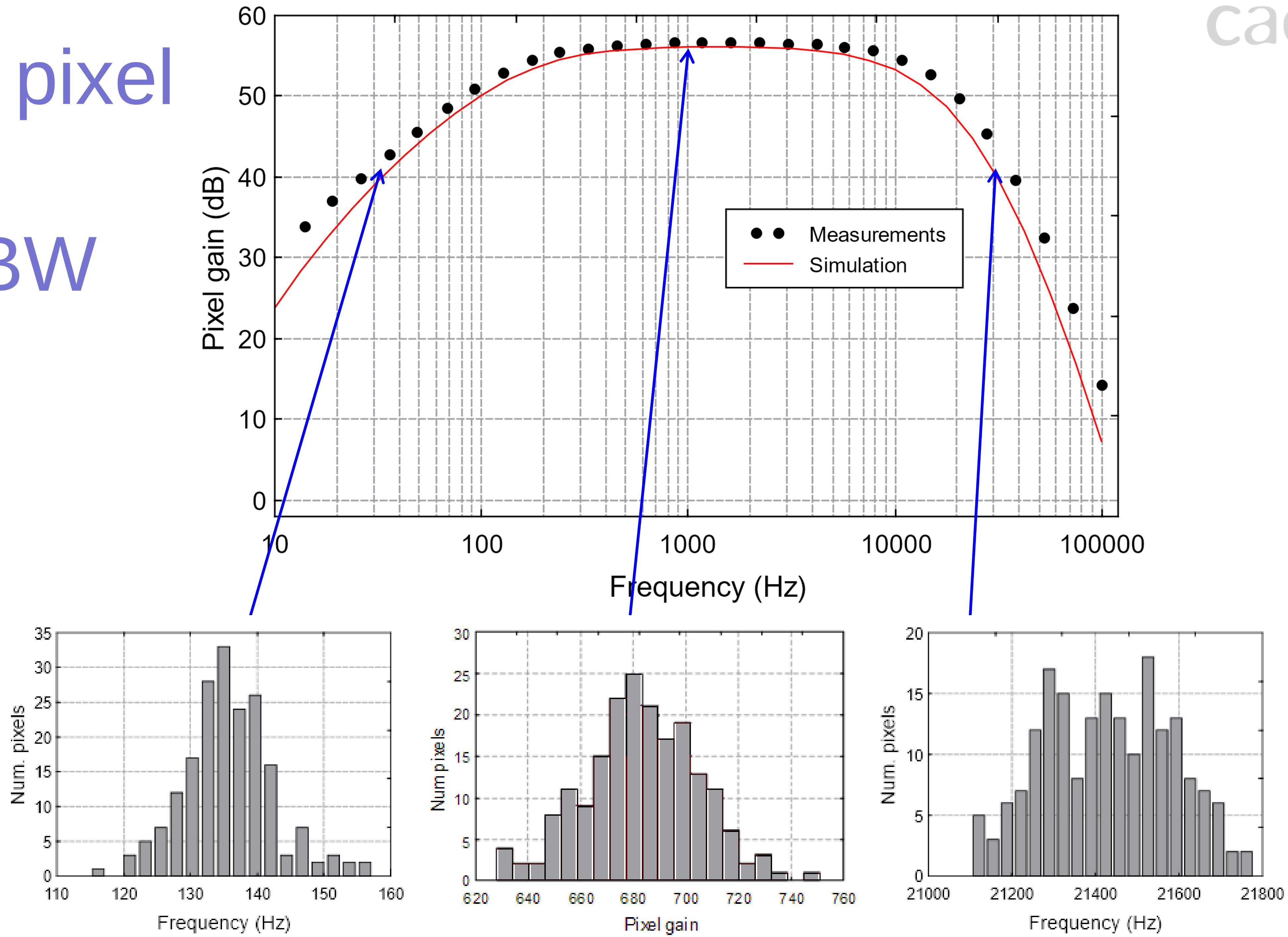


Henry pixel





Total pixel gain and BW



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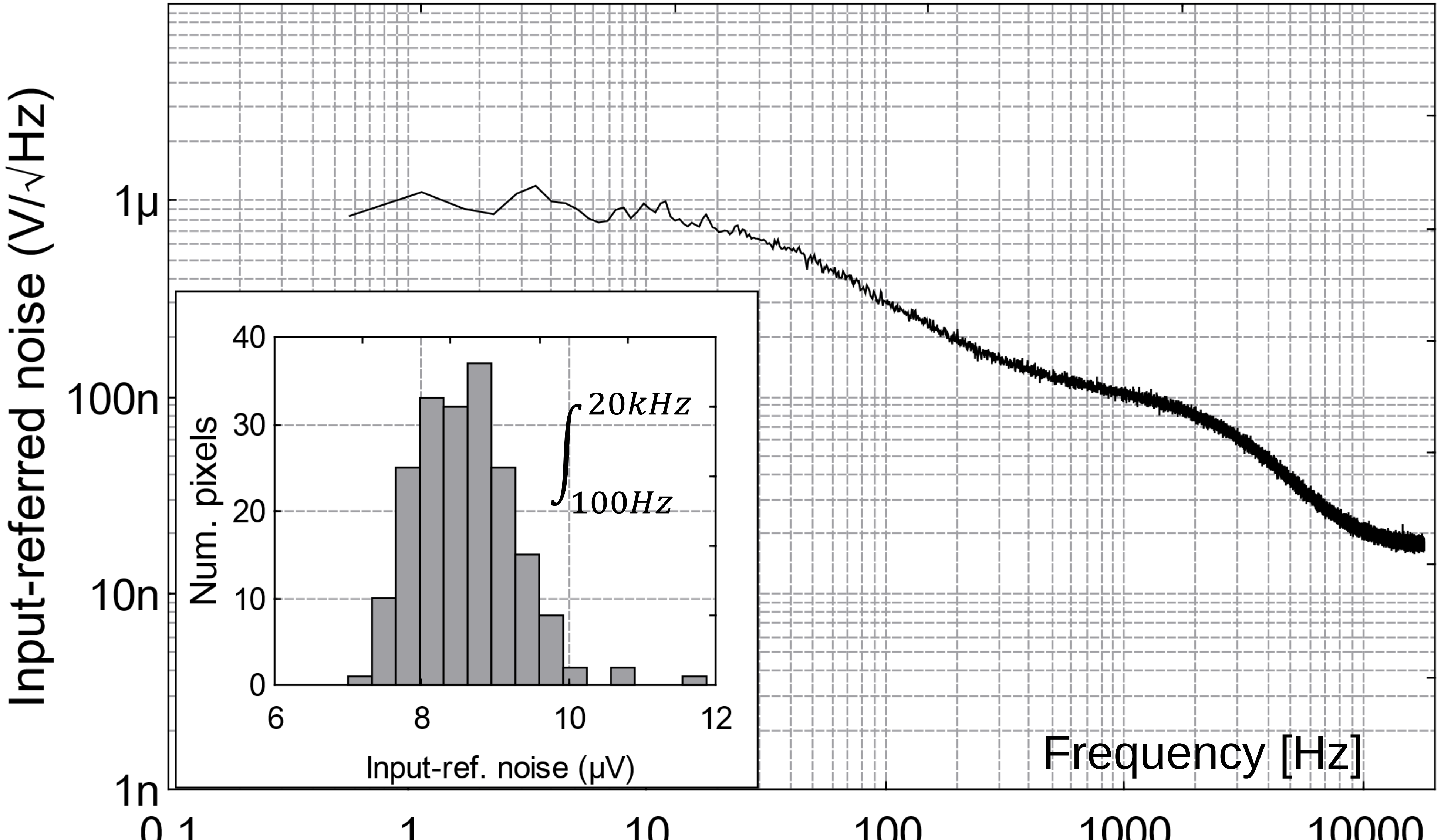
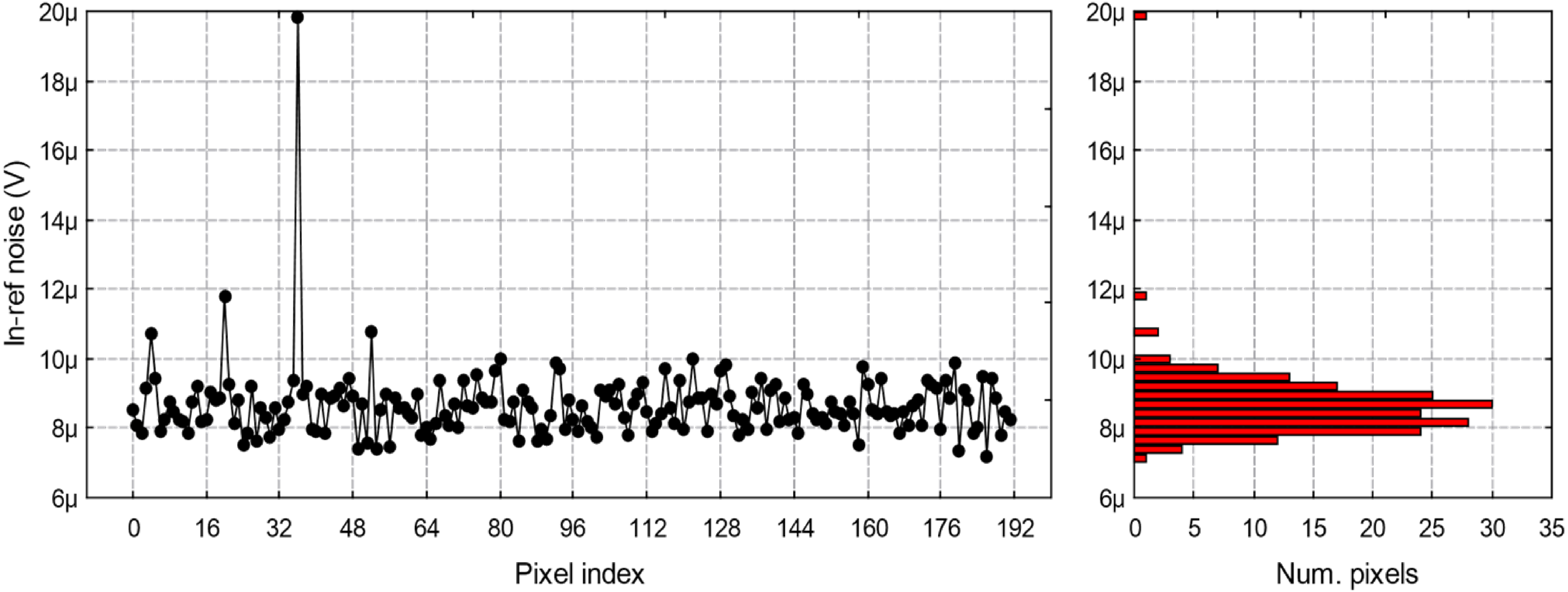
PSD + input noise histogram



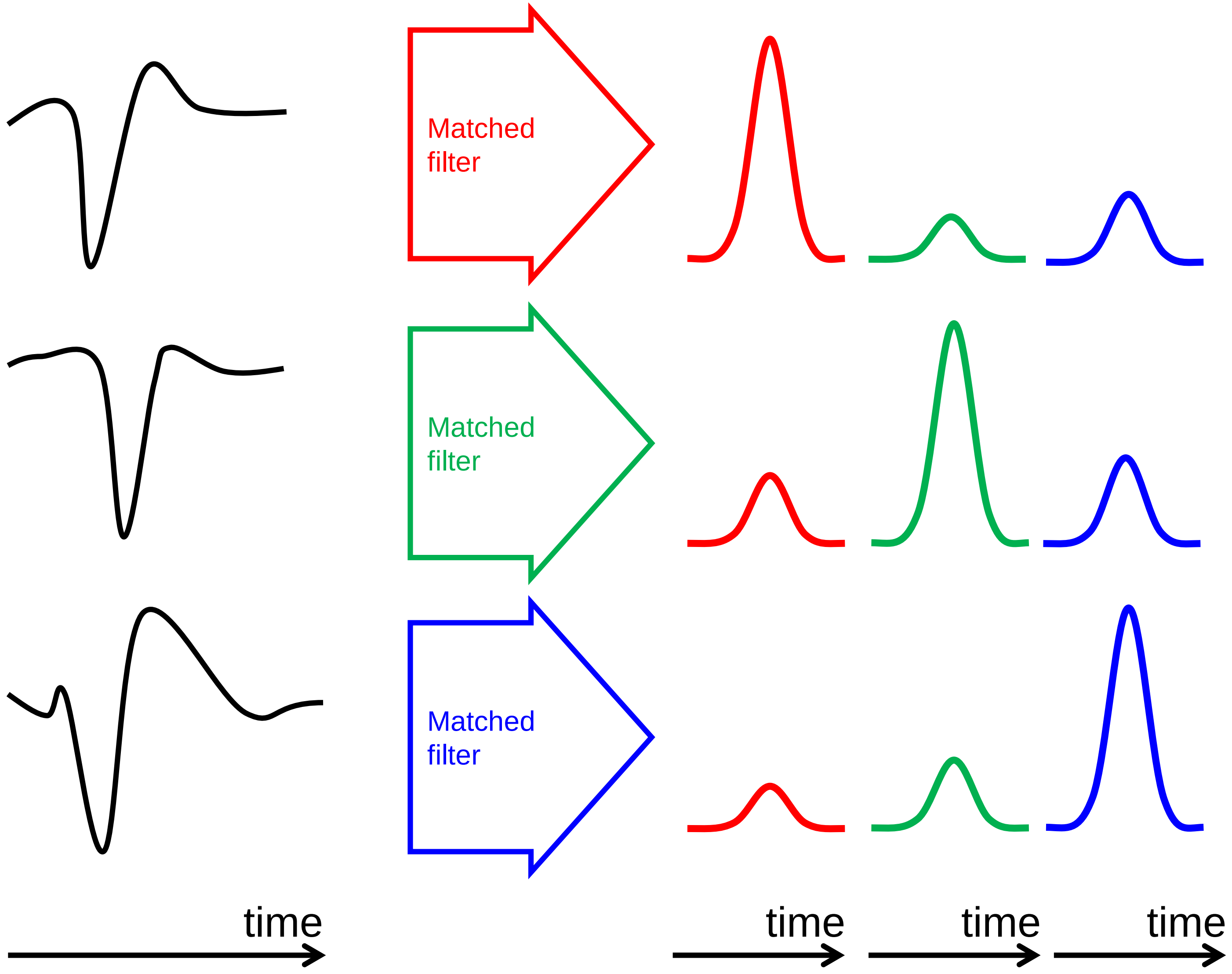
Henry pixel noise
input referred noise of one row of pixels

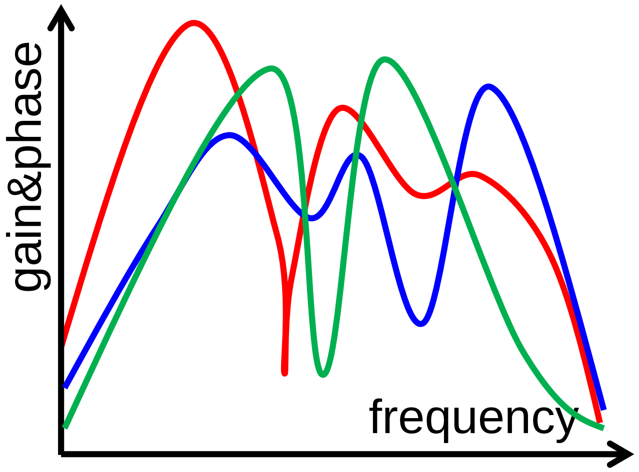


3. Future outlook

→ recognize pulse shapes by matched filters
→ design of programmable filters
→ measured performance of prototypes

Data reduction == recognize these shapes

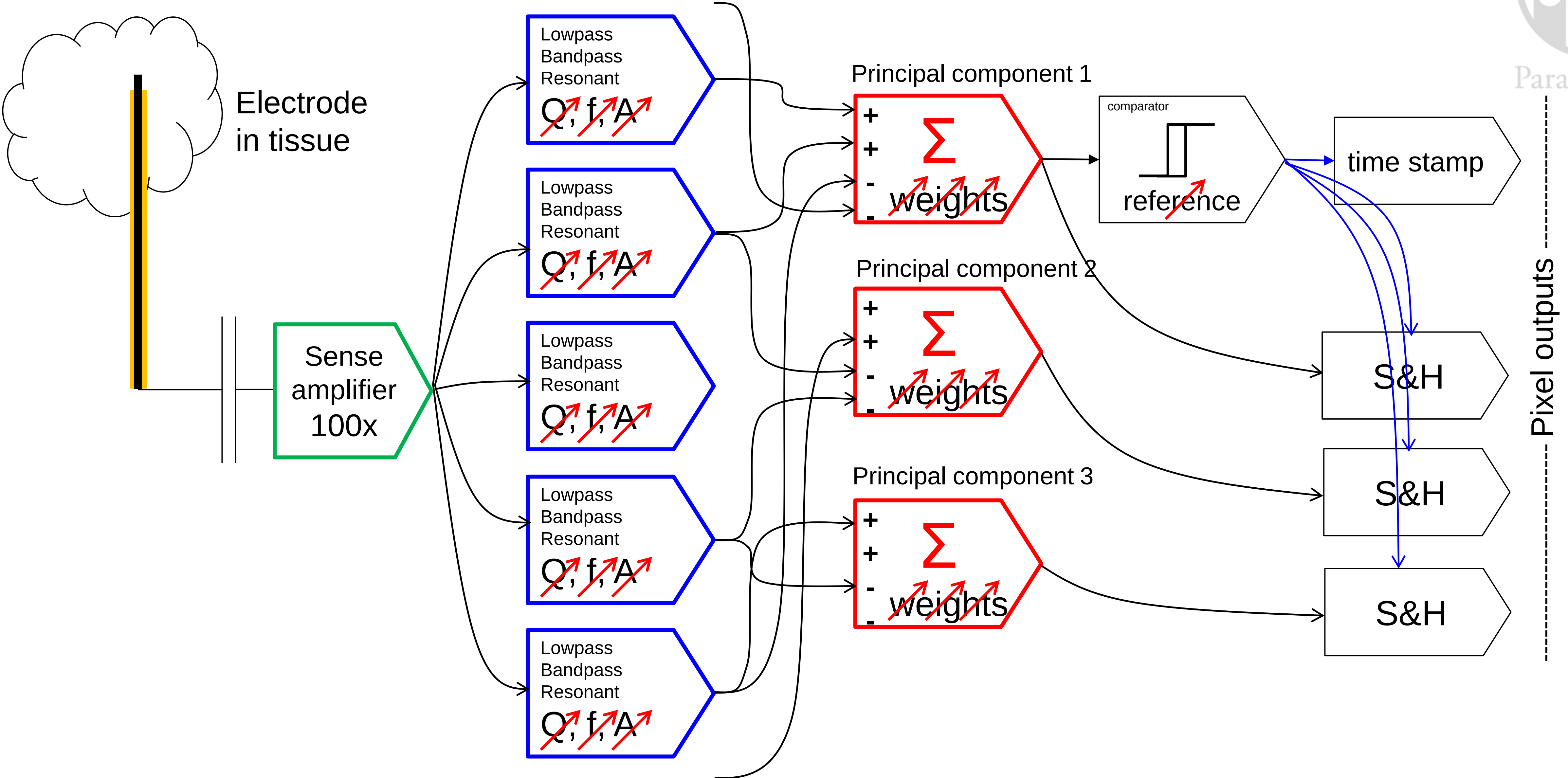




“matched filters”

Approximated by a linear sum of 2nd order filters

Pixel topology



Programmable filters

Filters

- (resonant) bandpass filter
- (resonant) lowpass filter
- summator

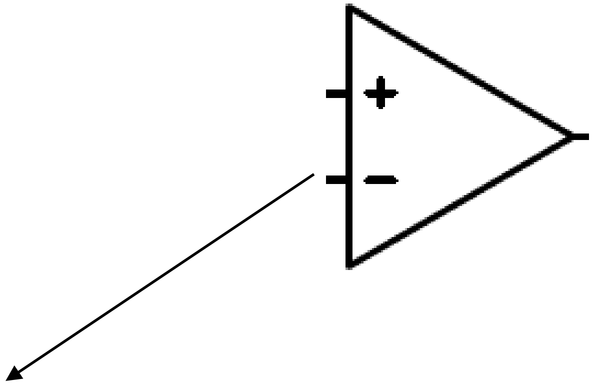
Based on “ideal” R+C active filters

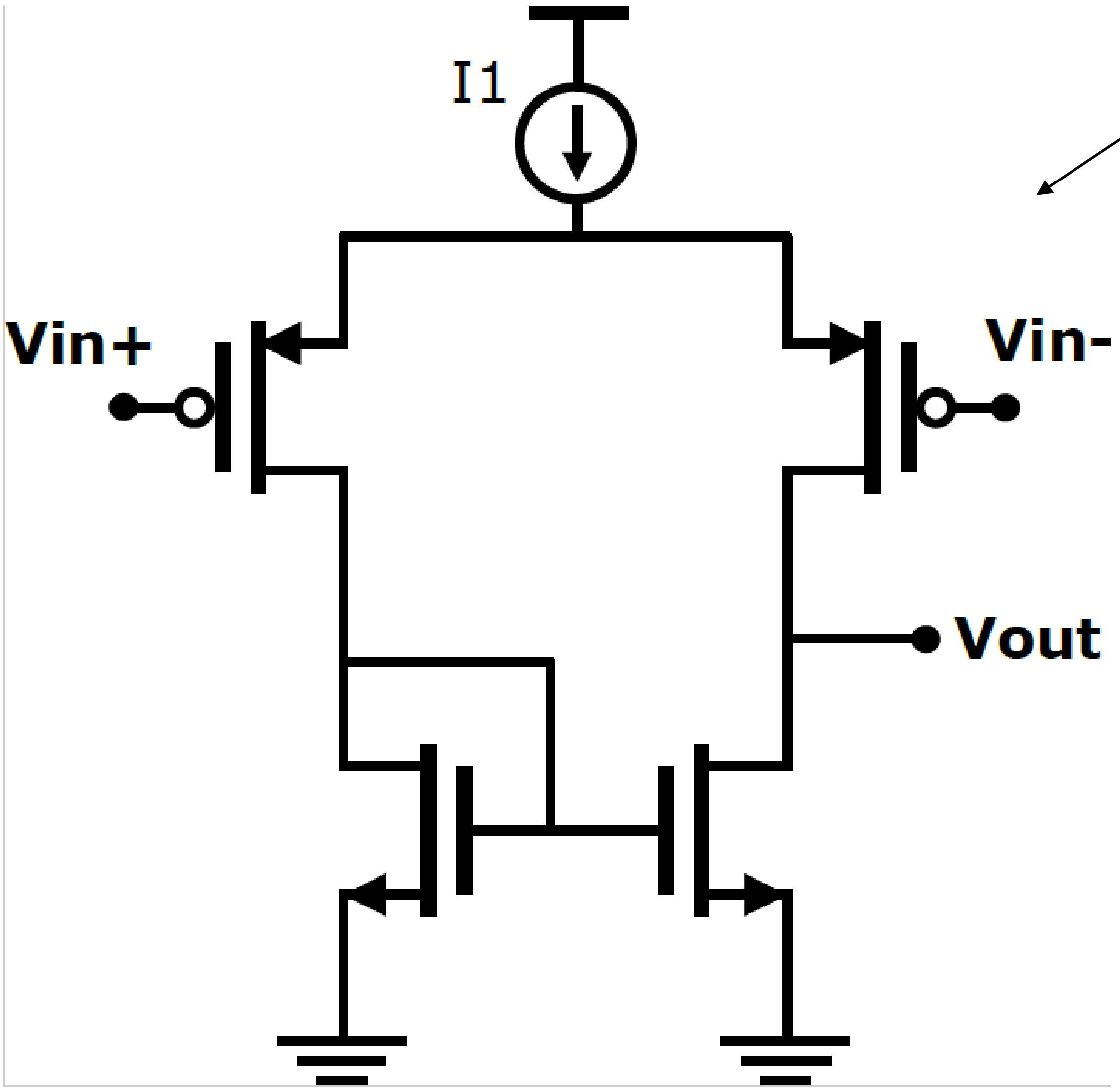
Actually I_{BIAS}/g_m+ C implementations

Continuous programmability of center/lowpass frequency, Q and gain, by programming I_{BIAS}

Patent WO 2018/191725 pending

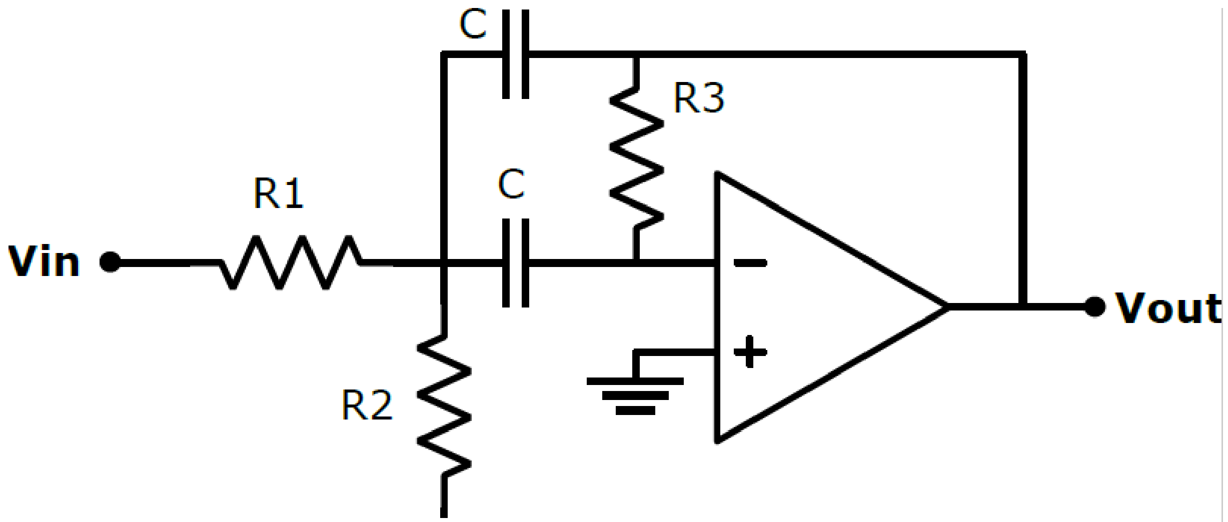
The OTA

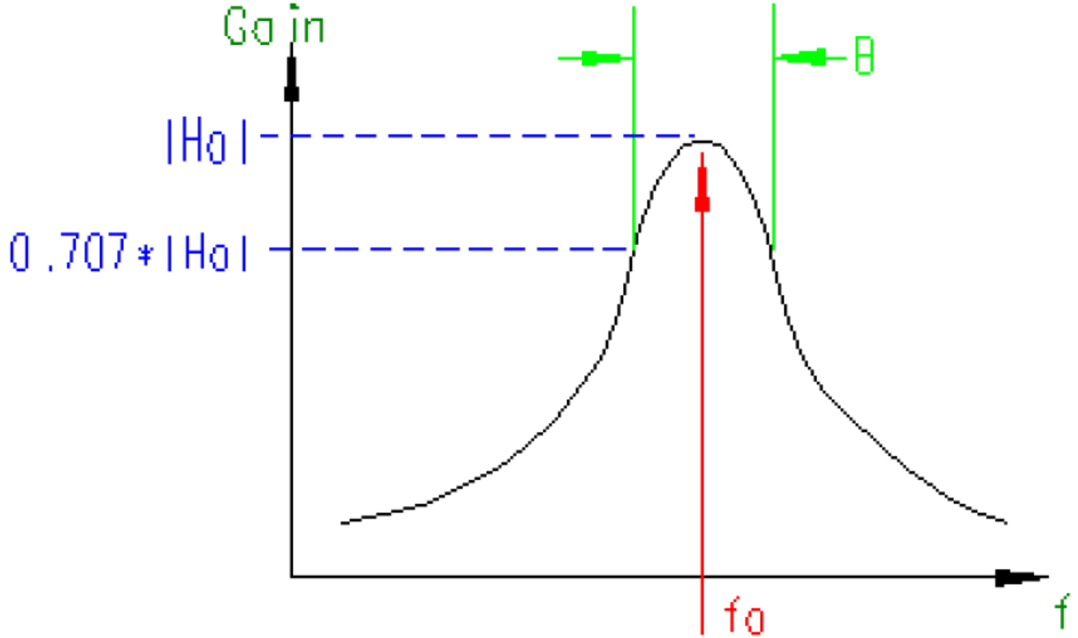




- All transistors are minimum sized, or larger for mismatch
- Tail current can be adjusted between <1fA and >1µA
- Gain = between 100x and 200x

Resonant bandpass filter (ideal)





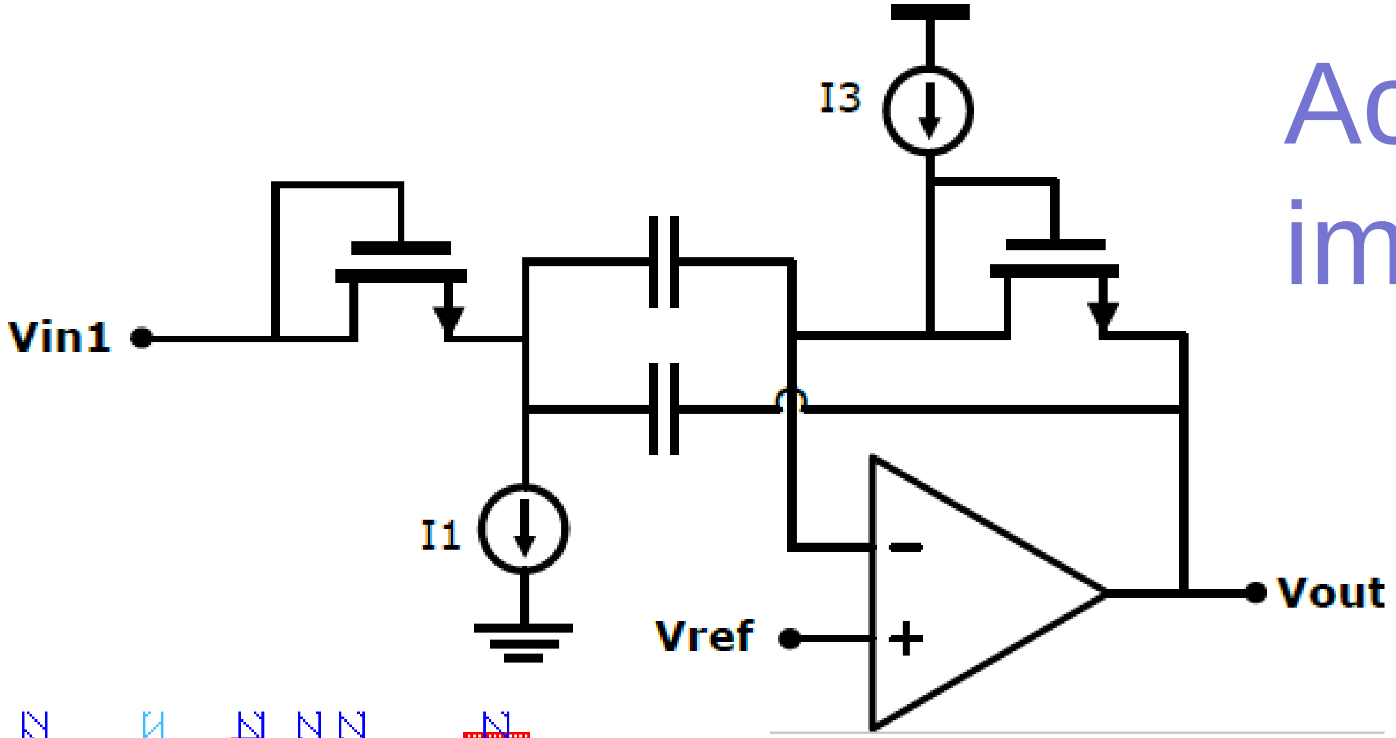
Bandwidth = β

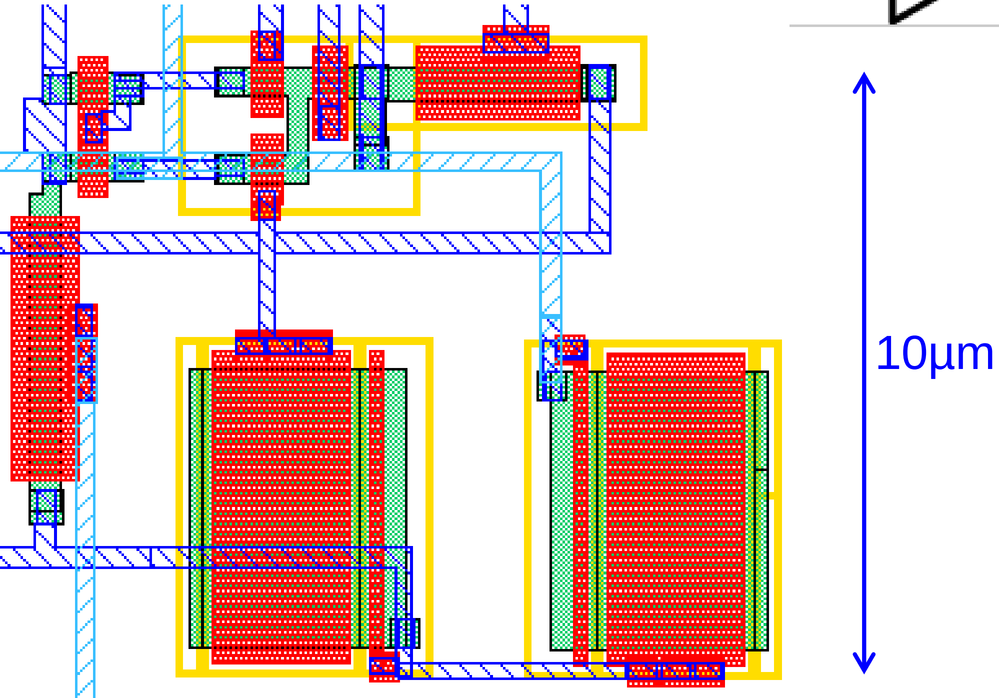
Quality factor = ω0/β

$$H_o = -\frac{R_3}{2R_1}$$

Radian frequency	Hertz
$\omega_o = \dfrac{1}{C\sqrt{(R_1 \| R_2)R_3}}$	$f_o = \dfrac{\omega_o}{2\pi}$
$\beta = \dfrac{2}{CR_3}$	$B = \dfrac{\beta}{2\pi}$

Actual implementation



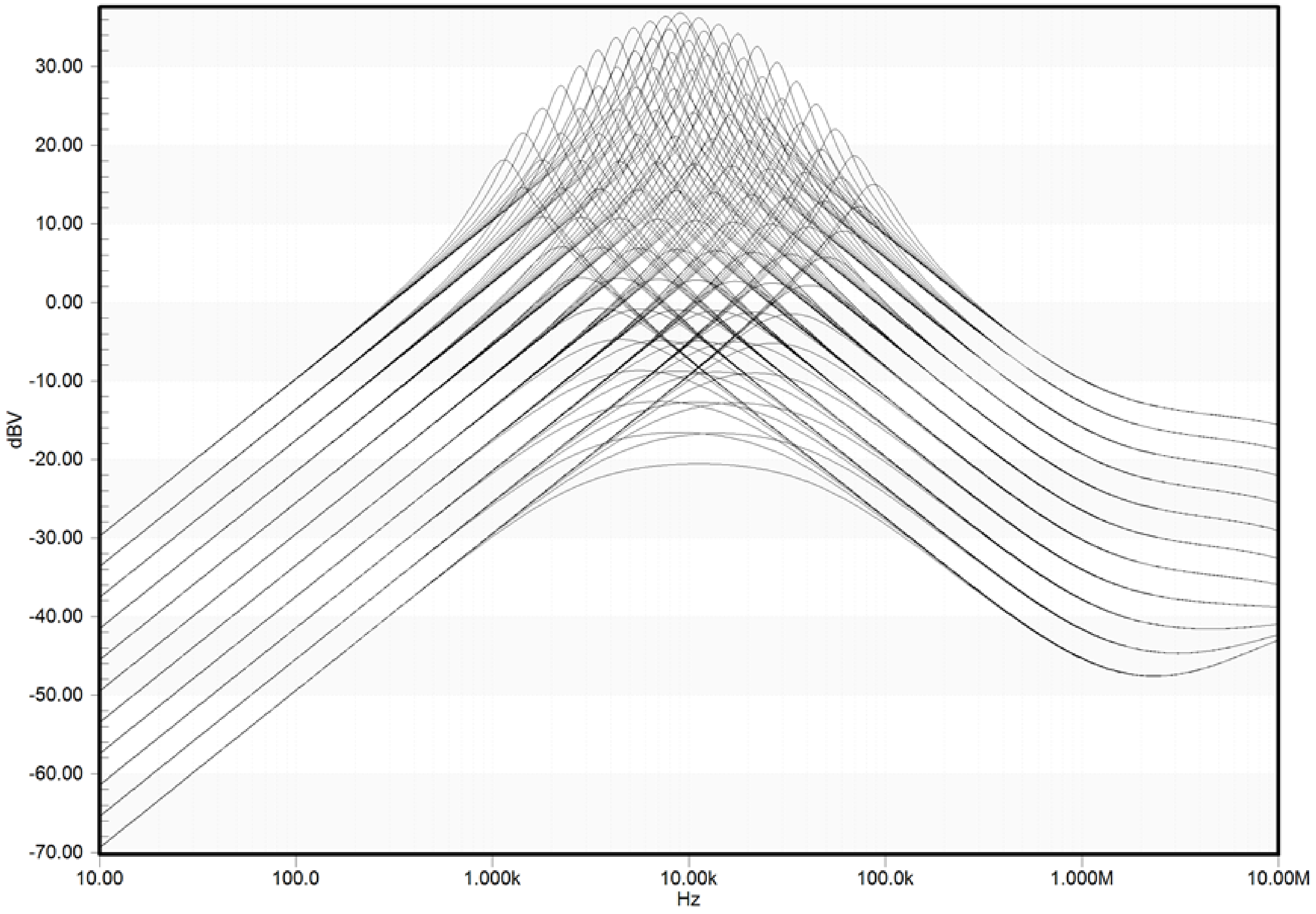


Pro: compact layout
Pro: easy to implement, pure MOS
Pro: input offset free
Pro: programmable by current
Con: one less degree of freedom (R2 absent):

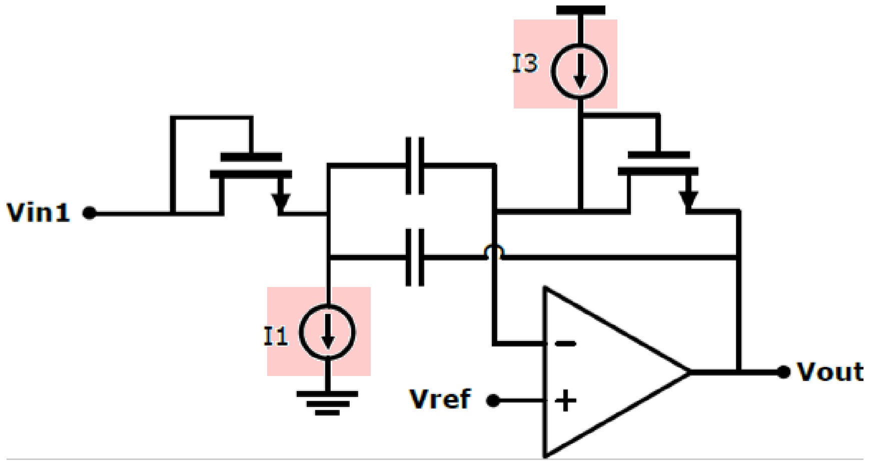
If Q must be large, the difference between the two currents becomes huge.

If Q is too small, the center gain H0 becomes small as well.

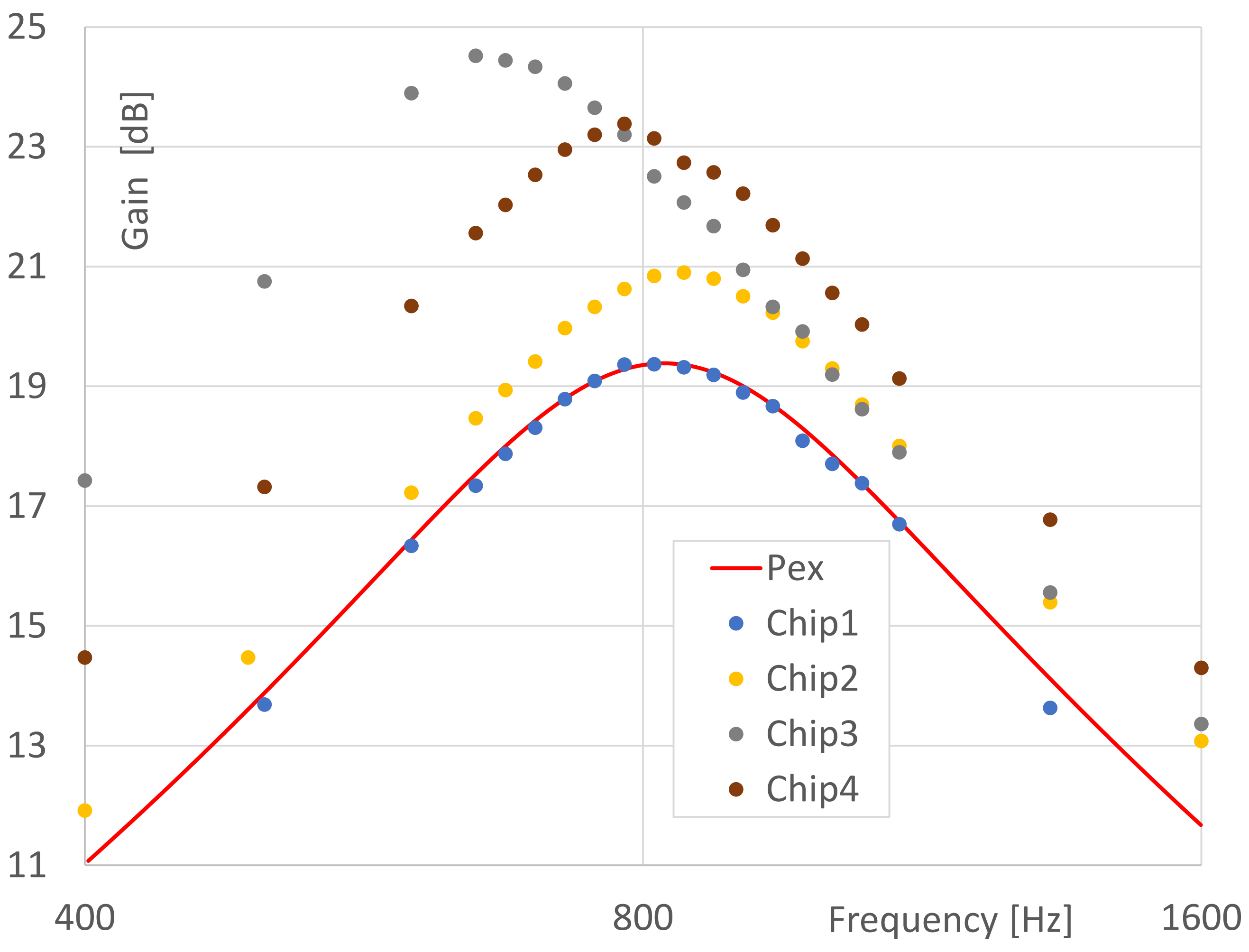
Sweeping both branch currents (simulation)

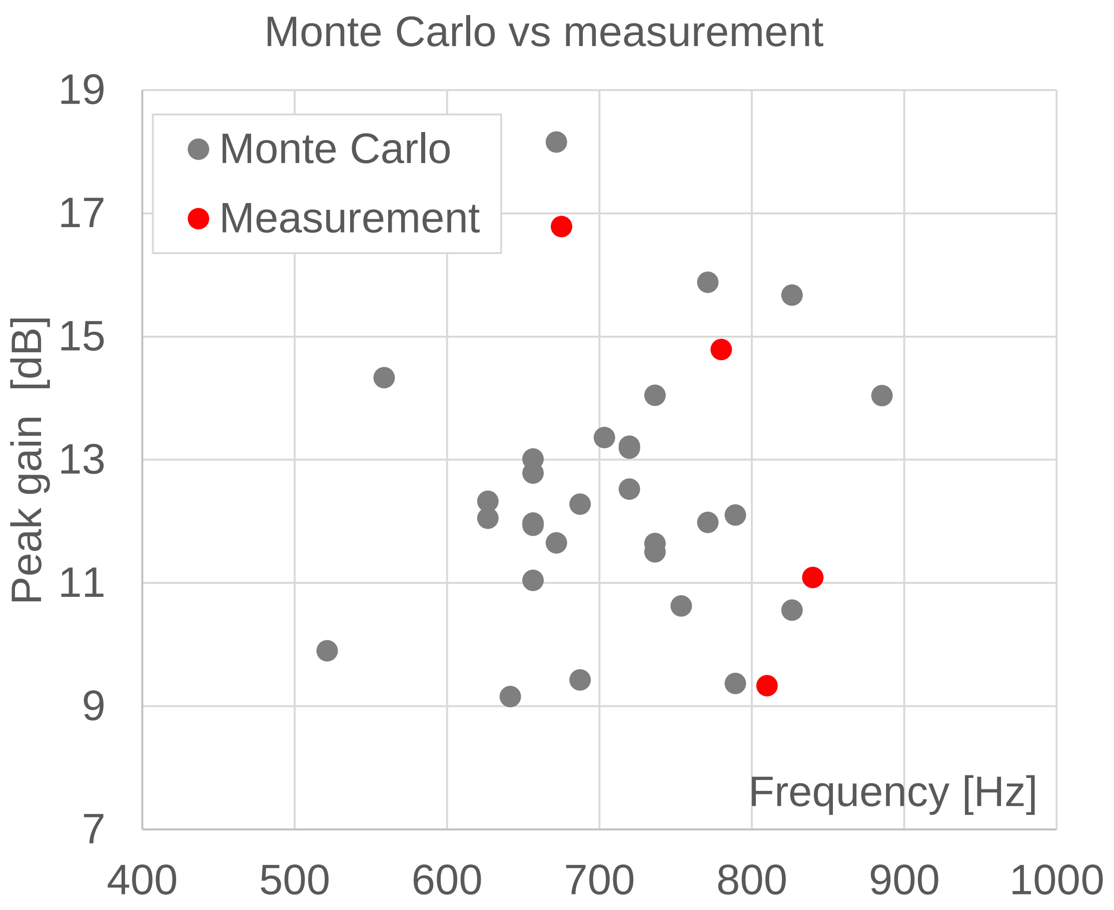


- The two branch currents are adjusted to obtain the desired Q and resonant frequency
- C=100fF

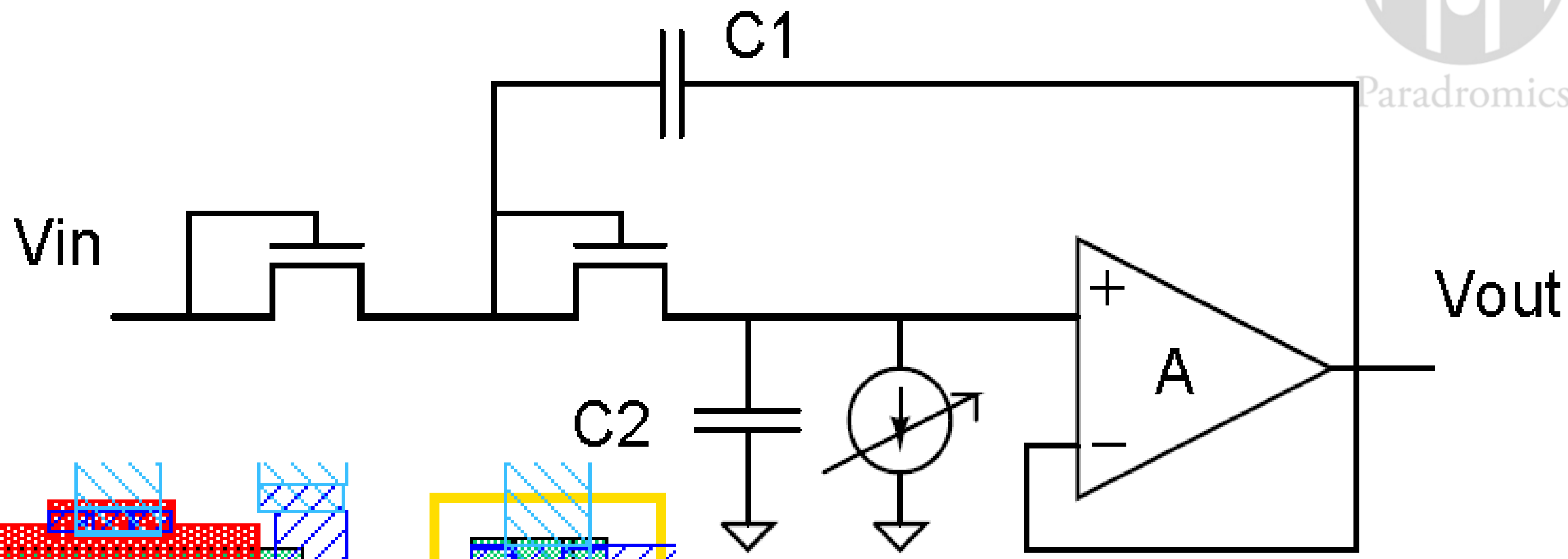


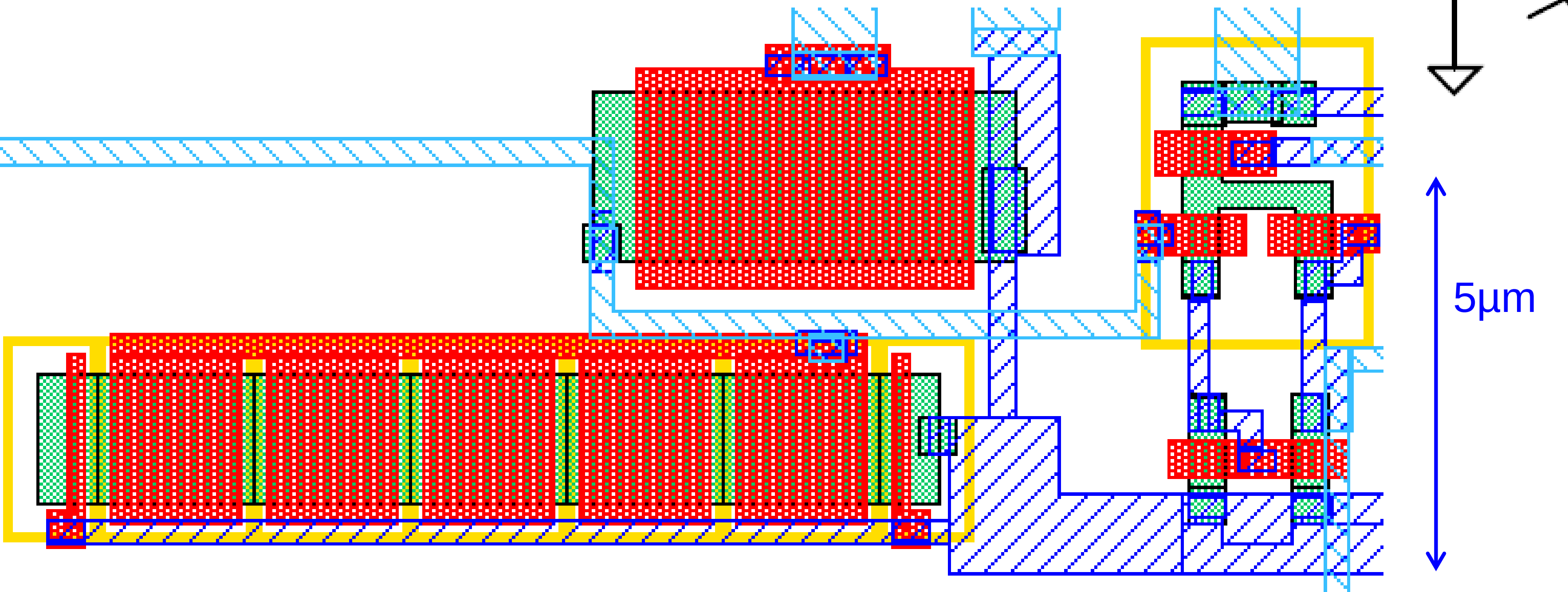
BPF measurement vs simulation



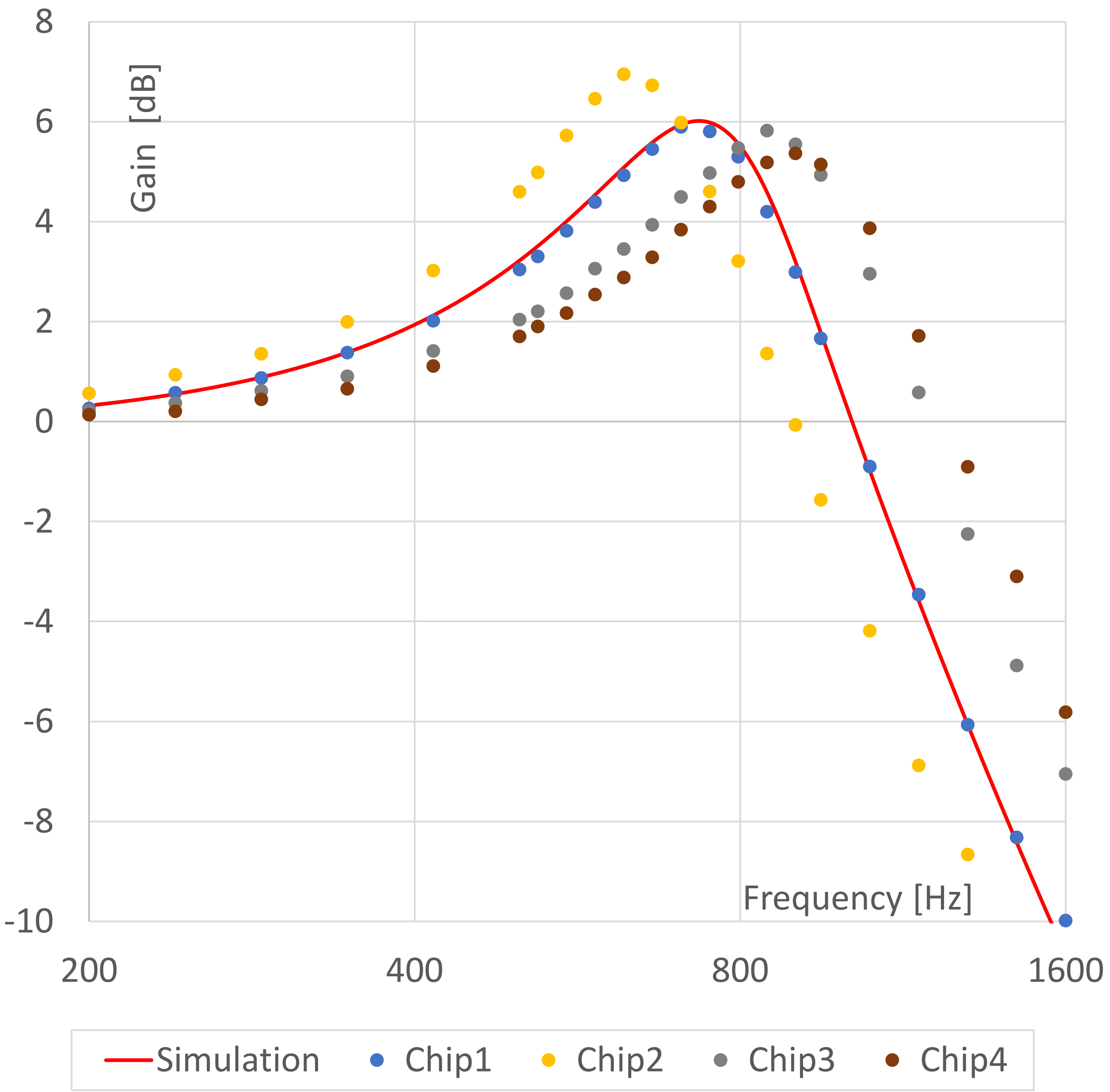


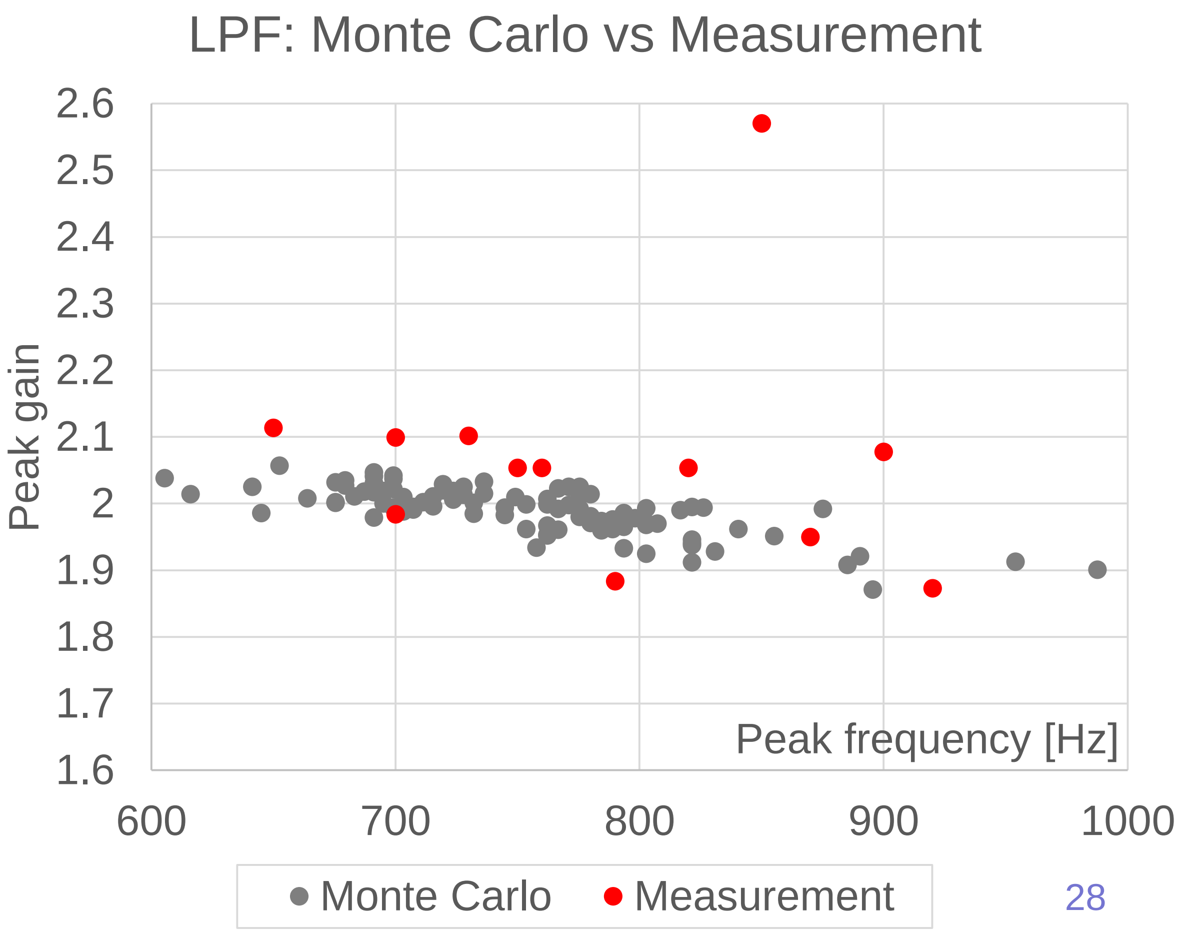
2nd order low-pass filter



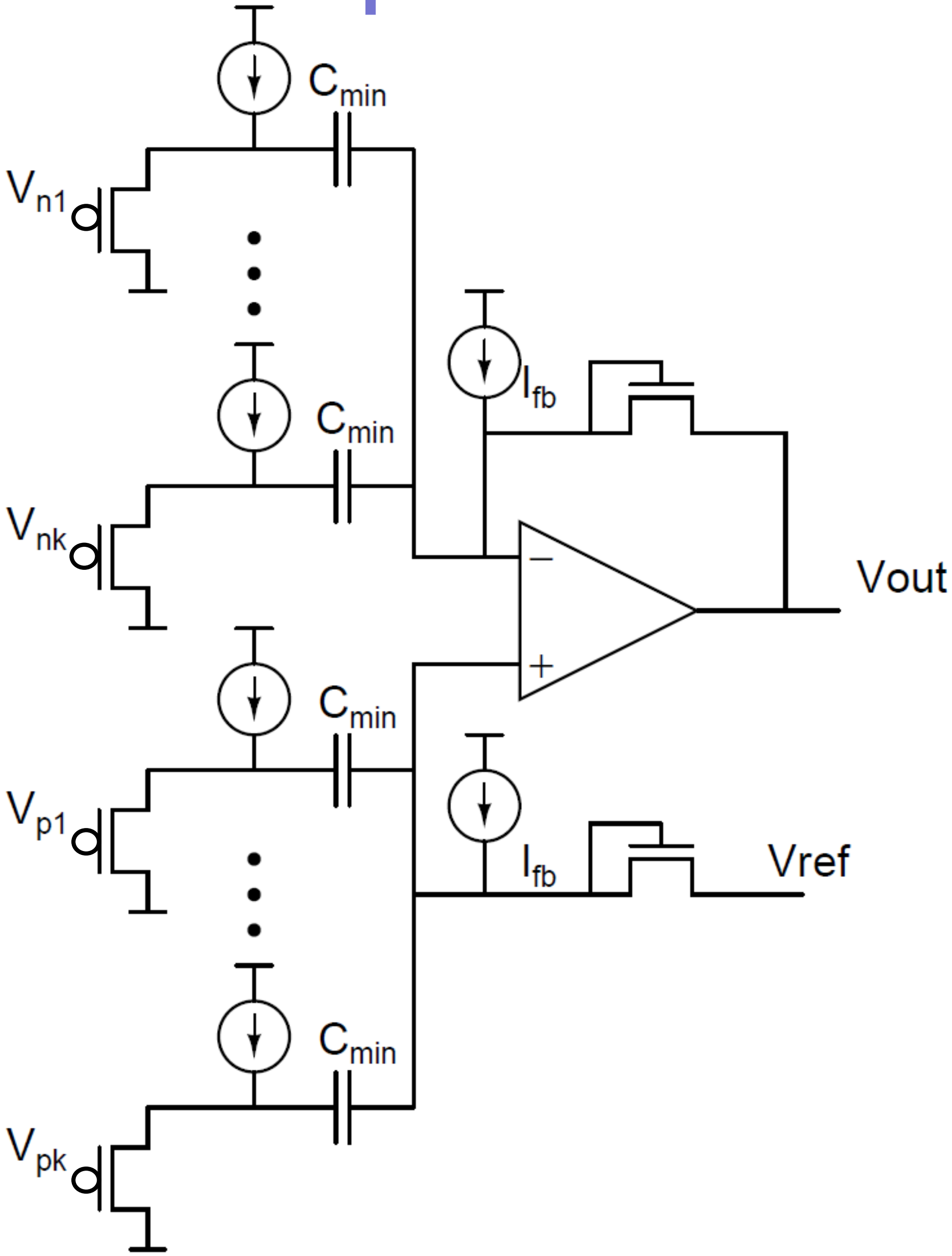


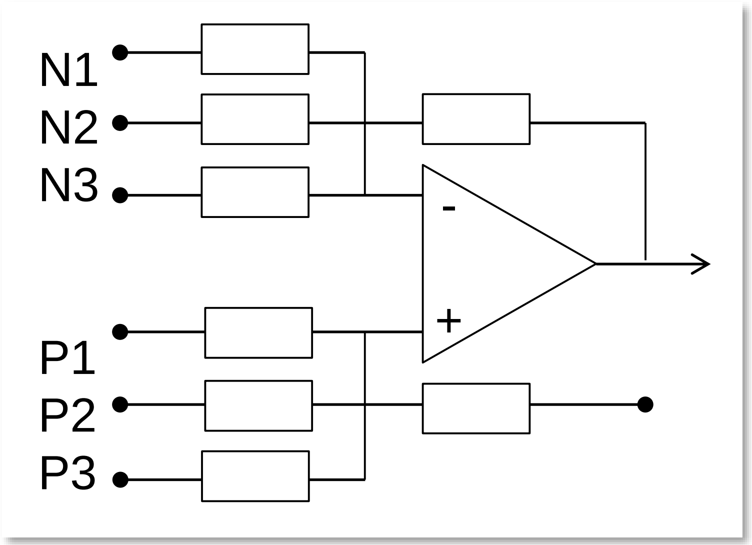
LPF measurement vs simulation





Multi-input differential summator



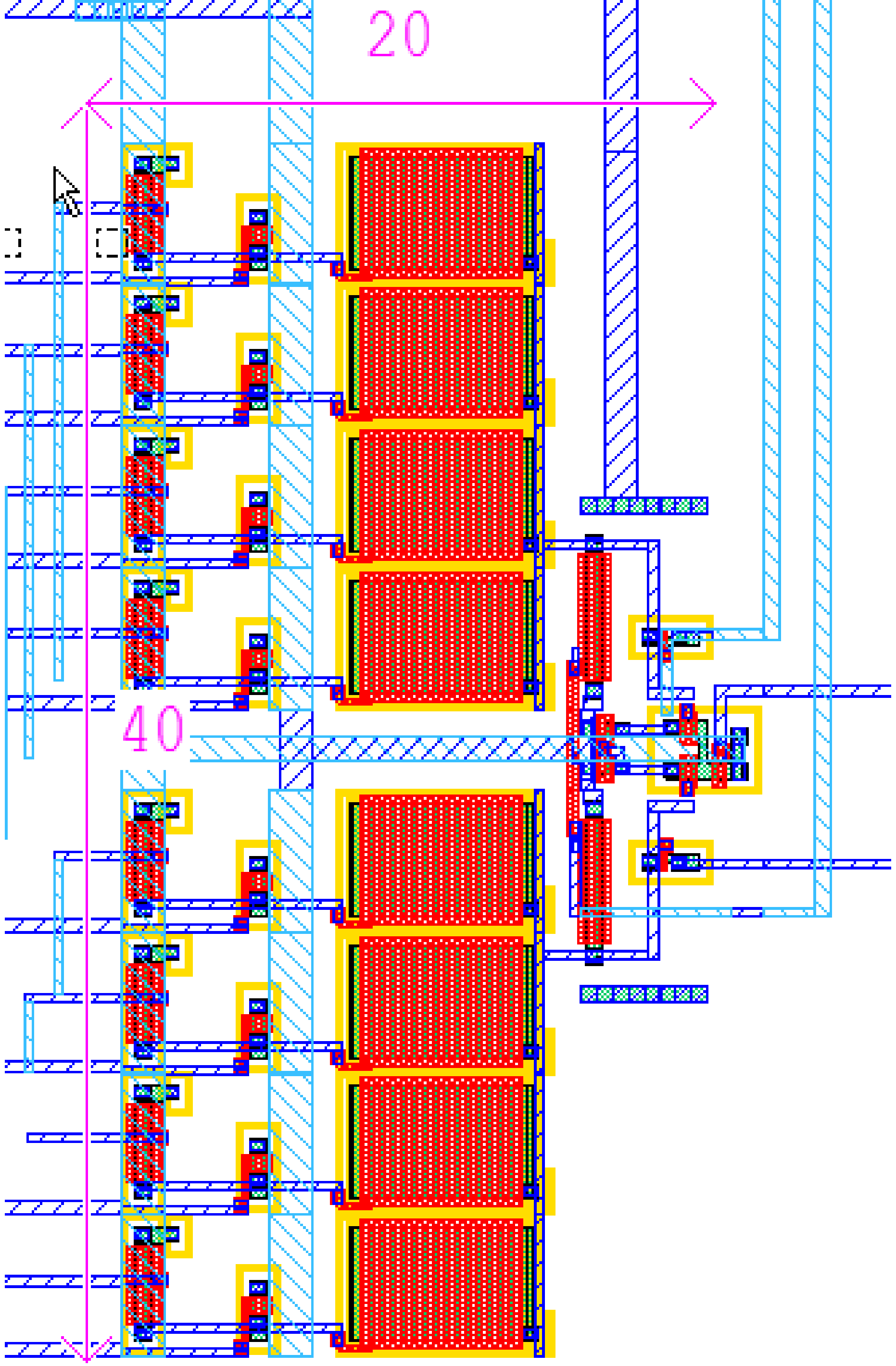


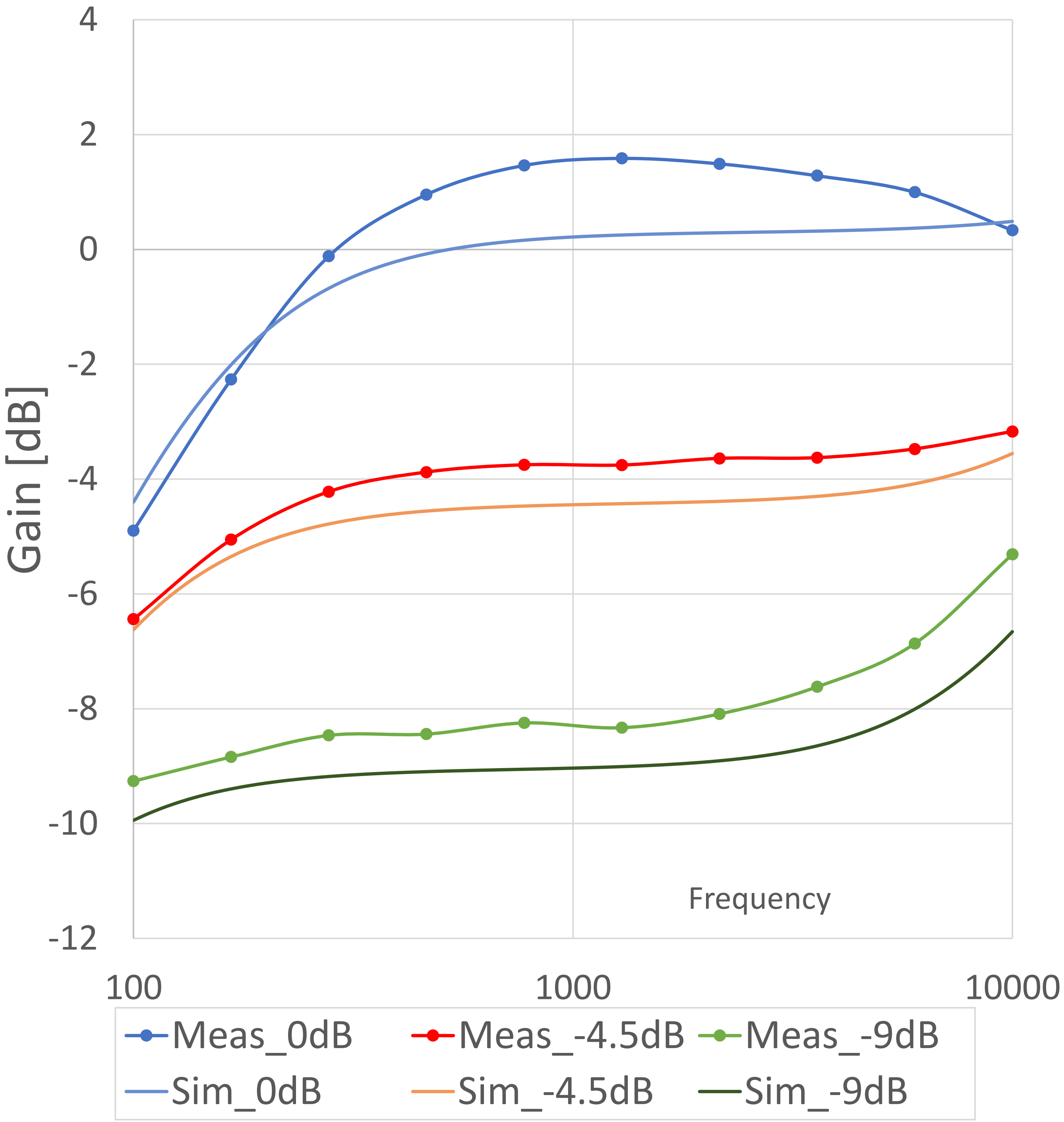
- Pure MOSFET design
  - All transistors have minimum size (except when needed for matching)
  - Capacitors are 100fF MOS
  - Input stages are PMOSFET source followers
- By adjusting the currents one can set the SF's output impedance, hence the gain of each branch

Summator layout

4 + inputs

4 - inputs





Summator: simulation vs. measurement

Three different branches with different gains 0dB, -4.5dB, -9dB

Measurement compared with simulation

4 Conclusions

Conclusions

- Unprecedented massive parallel 256x256, 50µm pitch neural probe ROIC
- 10µV_{RMS} @ 20kHz bandwidth

- Compact, in-pixel analog domain filters demonstrated
- Fully programmable
- Key design issue: mismatch of MOSFETs causes variability of frequency, gain and Q

caeleste

Paradromics

Thank you!

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Co-PIs: Angle and Melosh