Pixel detector R&D for the Compact Linear Collider (CLIC)

Mathieu Benoit, University of Geneva
on behalf of the CLICdp Collaboration
The Compact Linear Collider

- Proposed linear collider with two-beam acceleration
  - $e^+ e^-$ collisions
  - Achieves field gradients of $\sim 100$ MV/m
  - Center of mass energy stages: $380$ GeV $\rightarrow 3$ TeV
  - Physics goals: precision SM Higgs, Top and BSM physics

For the vertex and tracking detector:

- Low Power consumption
  - 50mW/cm$^2$ target in the vertex detector
    - air-flow cooling
    - Power-pulsing
  - Triggerless readout

- Low Mass
  - $0.2\% \chi_0$ per vertex layer
- High Single point resolution
  - Vertex: $\sigma_{SP} \sim 3\mu$m
  - Tracker: $\sigma_{SP} \sim 7\mu$m
- Precise time stamping
  - $\sim 5$ns
- Background reduction

Beams of 312 bunches, 50Hz rate
Spacing between bunches: 0.5ns

Low duty cycle
Power pulsing, see poster by E. Perez Codina:
Timepix3 performance in pulsed power operation
The CLIC vertex and tracking detector

A light weight vertex detector

- **Pixel size**: 25 x 25 µm², $\sigma_{SP} \sim 3\mu$m
- **Timing resolution**: < 5 ns
- **Material**: 0.2 % $X_0$ / layer
- **Moderate radiation exposure**: 
  - NIEL: $< 10^{11}n_{eq}/cm^2/\text{y}$
  - TID: $< 1$ kGy / year

A large area tracker (140m²)

- **Pixel size**: 50 µm x O(mm), $\sigma_{SP} \sim 7\mu$m
- **Timing resolution**: < 5 ns
- **Material**: 1-2 % $X_0$ / layer
- **~140m² of instrumented surface**
Vertex and tracking R&D cycles

- Design and preliminary studies
- Detailed TCAD and Monte-Carlo Simulation
- Lab and test-beam characterization

**Our toolbox**

**Timepix3 Telescope @ SPS**

and **Caribou universal readout**
Tools: The CLICdp Timepix3 Telescope and Caribou readout

The CLICdp Timepix3 telescope

- 7 x Timepix3 telescope planes
- Continuous readout
- ~1.2ns time resolution on tracks
- ~2 µm resolution at the DUT
- Flexible mechanics with rotation stages for angle study

The CaRIBOu universal readout framework

- Multi-chip modular r/o framework
- Stand-alone system based on Zynq SoC running YOCTO Linux
- Peary generic DAQ software
- Generic CaR board for powering and monitoring of DUT
- Implementation for CLICPix, CCPDs, ATLASPix, FEI4, H35DEMO and more …
Tools : Allpix\textsuperscript{2}

CERN.CH/allpix-squared

- A Modular, Generic Simulation Framework for pixelated Detectors
  - Generic simulation of pixel, strip detectors
  - Simple text base description of the geometry, simulation parameters
  - Charge transport and TCAD Electric Field import facilities
  - Visualisation and digitisation
  - Output in popular formats (EUDET, PROTEUS, Corryvreckan, etc.)
  - Provided pre-compiled, via CVMFS, Docker
  - Continuous integration and unit test

CLIC Vertex and tracker technologies

**Hybrid planar sensors**

- Collection diode
- Electronics
- Readout chip
- Sensor
- High Voltage

**ELAD planar sensors**

- Collection diode
- Electronics
- Readout chip
- Sensor
- Charge Sharing implants
- High Voltage

**CCPD sensors**

- Collection diode
- Electronics
- Readout chip
- Sensor
- High Voltage

**Sensor-ASIC integration**

- Lower material
- Large area production possible
- Trade-off between performance and integration

**Hybrid sensors**

- SOI CMOS sensors
- Burried oxide
- Collection diode
- Sensor + readout chip
- High Voltage

**Monolithic sensors**

- Large Fill-Factor CMOS
  - Deep collection diode
  - Sensor + readout chip
  - High Voltage

- Small Fill-Factor CMOS
  - Collection diode
  - Shielded electronics
  - Sensor + readout chip
  - High resistivity substrate

See presentation by A. Velyka in previous session for details on ELAD

See presentation by M. Idzik in previous session for more details
Hybrid planar sensors

The CLICPix2 ASIC
- Timepix/Medipix chip family
- \textbf{65nm} CMOS Technology
- 128x128 pixels, \textbf{25x25 µm}²
- \textbf{5 bit TOT and 8 bit TOA} for each pixels
- Shutter based readout with data compression
- \textbf{Power Pulsing} of matrix and readout block

Hybridization and testing
- FBK and Advacam Active edge sensors produced with CLICPix2 footprint
- Bumping performed by IZM using \textbf{SnAg} bumps and handle wafers -> Challenging !
- Best assemblies with \textbf{<0.5%} of unresponsive or disconnected bumps
- Test beam characterization ongoing

See A. Nürnberg 2016 JINST 11 C11039 for testbeam results on CLICPix
Capacitively-Coupled Pixel Detectors (CCPD)

(CCPOv3)C3PD+CLICPix(1)2

- 2 sensors, CCPDv3 and CLIC CCD (C3PD) were designed in ams aH18 HV-CMOS technology
  - (64x64) 128x128, 25x25 μm² pixels
  - Substrate resistivity from 20 to 200 Ωcm
- First amplification layers integrated in sensors to provide large signal at output
- I²C 2-wire slow-control interface (C3PD)
- Coupling with ASIC done through a very thin layer of glue forming a capacitor (Low mass!)
  - Glueing method developed to using flip-chip assembly to acheive down to 100 nm glue layers
  - Fast prototyping method wrt planar sensors

Also demonstrated on large (2x2 cm²) area: 2018 JINST 13 P12009

I. Kremastiitis 2017 JINST 12 C12030
M Vicente et al., CLICdp-Note-2017-003
Capacitively-Coupled Pixel Detectors (CCPD)

Tracking performance and energy resolution (C3PD)

Tracking performance versus track angle of incidence (CCPDv3)

CERN-THESIS-2018-114
Small-Fill factor CMOS sensors

CMOS electronics integrated in p-well separated from collection electrode:
• Minimisation of diode size
• Minimisation of sensor capacitance down to ~ fF (large S/N)
• Process modifications to achieve full lateral depletion (W. Snoeys et. al)
• Further modifications proposed to improve timing and radiation hardness, see Monday presentation by M. Munker

Investigator analogue test-chip:
• Analogue test-chip developed for ALICE ITS upgrade, produced in 180 nm CMOS imaging process
• Various pixel layouts implemented in different pixel layouts, electrode to pwell spacings

Test-beam results for both process variants:
• Spatial resolution ~ 7 μm for threshold values of ~400e
• Fully efficient operation to threshold values below ~400e
• Timing resolution ~ 6 ns (limited by readout)

Small-Fill factor CMOS sensors: CLICTD

Promising results of 180 nm HR CMOS imaging process trigger design of fully monolithic CLIC tracker chip:

- **Super-pixel segmented in high granular collection diodes** to maintain fast charge collection while reducing digital logic
- Super pixel size of **30 μm x 300 μm**
- Diode size of **30 μm x 37.5 μm**

Diode discriminator outputs combined in ‘OR’ gate:
- 8-bit ToA and 5-bit ToT measurements
- Storage of **hit-pattern**
- 100 MHz clock for **10 ns time binning**

Different operation modes:
- 8 bits time stamping information (ToA) + 5 bits energy information (ToT)
- 13 bits time stamping information (ToA)
- 13 bits photon counting (number hits that are above threshold)

Design completed, UVM Verification ongoing
Large Fill-Factor CMOS sensors

Implementation of fully monolithic sensors in ams aH18 process using high-resistivity wafers

- 180nm HV-CMOS Engineering run on 20-200 Ω cm substrate
- Thinned down to 60 µm
- 130x40 µm² pixels, 25x400 pixels
- 6 bit TOT and 10 bit TOA (up to 16 ns)
- Uniform breakdown across wafers at 60-85V
- Threshold down to 600e, 120e dispersion
- Full length column sensor (1.9cm)
- Trigger-less readout
- Serializer, PLL, High-Speed data transmission (1.25Gbps, aurora 8b/10b)
- Initially design for ATLAS, Radiation hard up to >1x10¹⁵nₑq/cm², 100MRad
- Close to CLIC Requirements

Large Fill-Factor CMOS sensors

- ATLASPix was tested in beam at FNAL, CERN SPS using the FEI4 and Timepix3 telescopes
  - Operated with 16 ns timestamp granularity
  - Known row delay dependence corrected
  - Timing resolution ~ 7ns measured
  - Spatial resolution: ~12µm in row direction
  - Efficiency at 0º >99.5%, no pixel masked
  - Noise << 10⁻⁶/25ns

Threshold = 800 e
Noise = 120e (untuned)
Large Fill-Factor CMOS sensors

Following promising results, a CLIC compatible chip with modified pitch ans 10 ns timestamp to be submitted in 2019!
Conclusion

• The CLIC accelerator and the proposed physics measurements impose strict requirements on the vertex and tracking detector:
  • good single point resolution, low material budget
  • High occupancy requiring fine timestamping of hits

• The CLICdp vertex and tracking R&D focus on studying the available pixel detector technologies through simulation and characterization
  • Allpix\textsuperscript{2} and TCAD simulation tools used to gain understanding of the devices
  • The Timepix3 telescope is used to characterize existing devices and evaluate their performances
  • Many devices studied: Planar sensors with fine pitch, ELAD Sensors, CCPDs, SOI pixel detectors, and CMOS sensors with small and large fill factor
  • Our device study allowed to identify promising technologies for CLIC vertex and tracker
backup
depletion
Enhanced Lateral Drift sensors (ELAD)

Concept to improve spatial resolution for thin sensors, H. Jansen (DESY/PIER):
- Deep implants to shape electric field lines in sensor
- Suggestive epitaxial layer grow and implantation
- Increased “linearised” charge sharing

Results of TCAD simulations show increased charge sharing for given pitch & thickness
-> Production of wafer with various deep implant doping ongoing

TCAD simulations for p-type ELAD:

Allpix² validation

290V

See presentation by A. Velyka in previous session for details

Patent DE102015116270B4
SOI sensors

- **Monolithic integration** with sensor electronics separated from high-resistivity substrate by Oxide layers

- Cracow SOI test chip in **200nm LAPIS SOI process**, different parameters:
  - >= 30 x 30μm² pixels
  - single-SOI and double-SOI wafers
  - different readout schemes implemented

- First test beam results for 500 μm thickness
  - SOI HR-CMOS: 30x30 μm² pitch, **Efficiency > 97%, σ_sp = 2μm**

**CLIPS : CLICPixel SOI in production**

- 4.4 × 4.4 mm (previous 2.9 mm)
- Targets
  - spatial resolution <3 μm
  - time resolution <10 ns
- Analog charge and time information in **storage capacitors in each pixel**
  --> no need for fast clock distribution into matrix
- Snapshot analog readout between bunch trains with external ADC
- Timing reference base on **tuned current source**

See [presentation](#) by M.Idzik in previous session for more details
CCPD Assembly process

CCPD + FEI4 unwrapping in clean room, Visual inspection

Surface cleaning of chip with IPA/DI water to remove macro-dust elements

CCPD + FEI4 Plasma cleaning with Argon plasma

CCPD + FEI4 Flip-chip alignment

Glue pattern dispensed on chip using translating stages and time-pressure dispenser inside the flip-chip

Bonding: 2kg for 4 cm², 6 min at 100°C, 1 min for irradiated + 24h at RT
CCPD Assembly process (In parallel)

Araldite 2011 Two-component mixing → Injection of glue in syringe

Centrifugation of glue to remove aire bubbles → Installation of syringe in Flip-Chip machine

Alignment of syringe tip to machine coordinates (need to dispense one drop of glue) → Ready for glue dispense for 100min
CCPD Assembly process
CCPD Assembly process

After assembly, we achieve routinely glue thickness of < 500nm with a variation of 100nm across 2cm

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Glue layer thickness

Energy Dispersive X-Ray Spectroscopy was used to investigate which material are present in the cross section

- Aluminium
- Copper
- Silicon

Glue
Glue layer thickness

Energy Dispersive X-Ray Spectroscopy was used to investigate which material are present in the cross section:
- Aluminium
- Copper
- Silicon
- Glue

Thicknesses:
- 2.42 µm (Glue)
- 1.85 µm (Aluminium)
- 0.57 µm (Silicon)