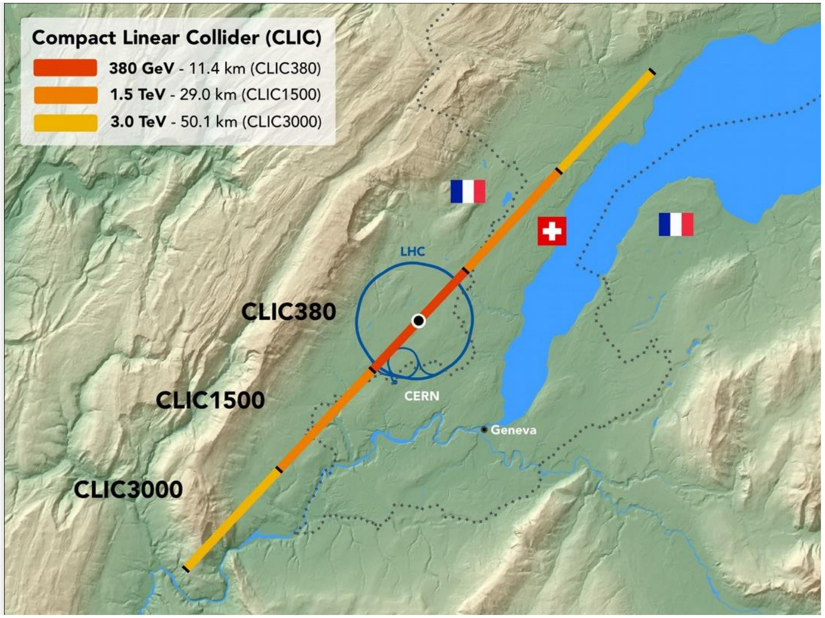
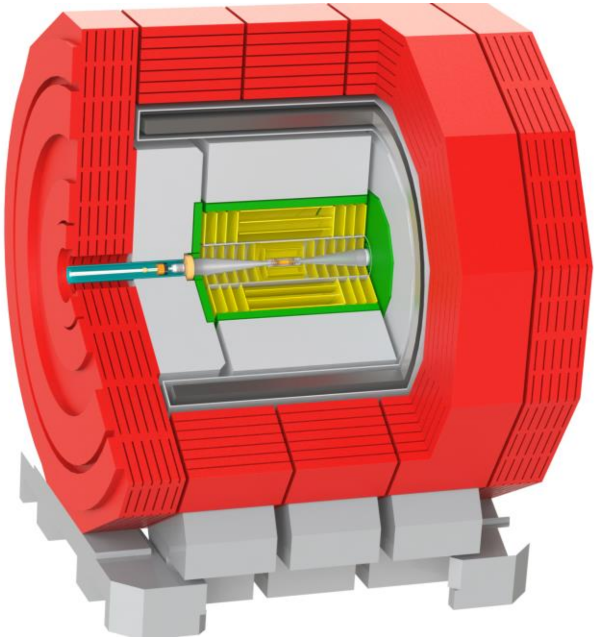




Pixel detector R&D for the Compact Linear Collider (CLIC)

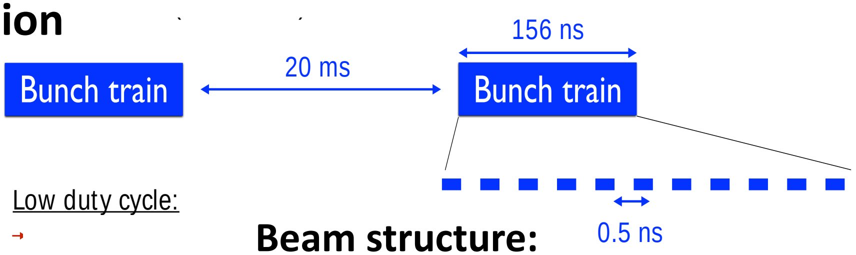
Mathieu Benoit, **University of Geneva**

on behalf of the CLICdp Collaboration

UNIVERSITÉ
DE GENÈVE

The Compact Linear Collider

- **Proposed linear collider with two-beam acceleration**
  - e+ e- collisions
  - Achieves field gradients of ~100 MV/m
  - Center of mass energy stages: 380 GeV → 3 TeV
  - Physics goals: precision SM Higgs, Top and BSM physics



Beam structure:

Trains of 312 bunches, 50Hz rate
Spacing between bunches: 0.5ns

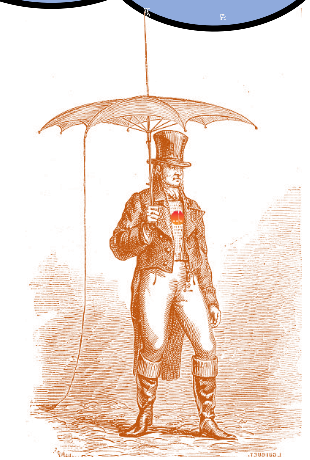
For the vertex and tracking detector:

50 Hz trains, Low radiation damage

High Precision physics measurements
Physics goals: precision SM Higgs, Top and BSM physics

High occupancy and pile-up
Large background from
γ γ → hadrons
and incoherent pairs

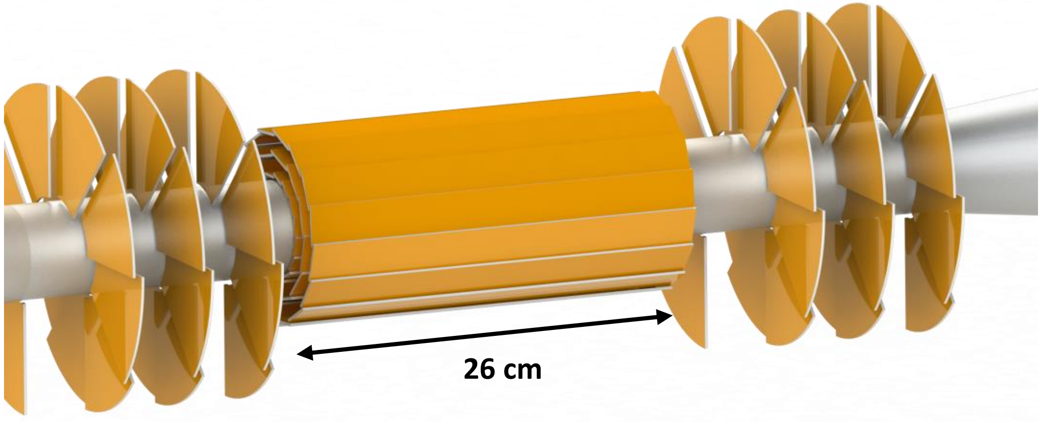
- **Low Power consumption** 50mW/cm^2 target in the vertex detector
  - air-flow cooling
  - Power-pulsing
- **Triggerless readout**



- **Low Mass** – 0.2% X_0 per vertex layer
- **High Single point resolution**
  - Vertex : σ_{SP} ~ 3µm
  - Tracker : σ_{SP} ~ 7µm
- **Precise time stamping** ~ 5ns
  - Background reduction

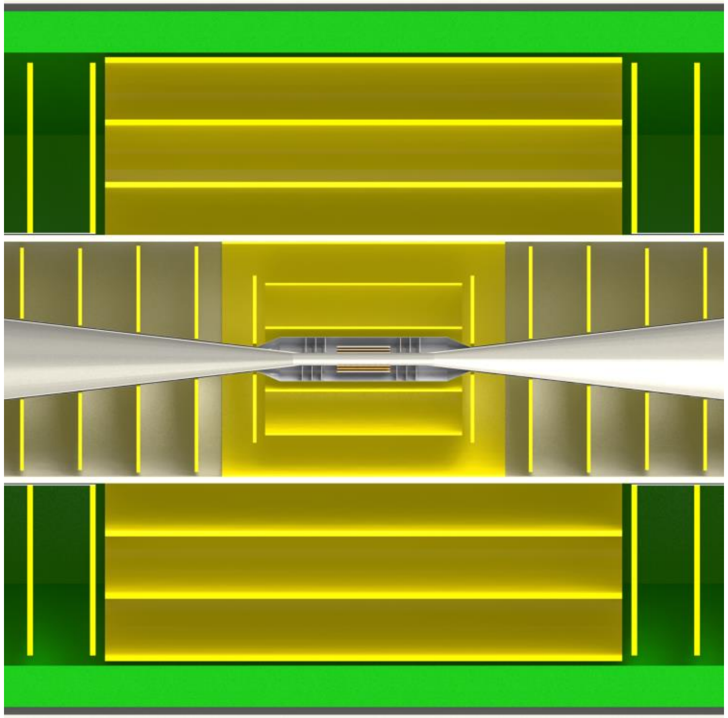
The CLIC vertex and tracking detector

A light weight vertex detector



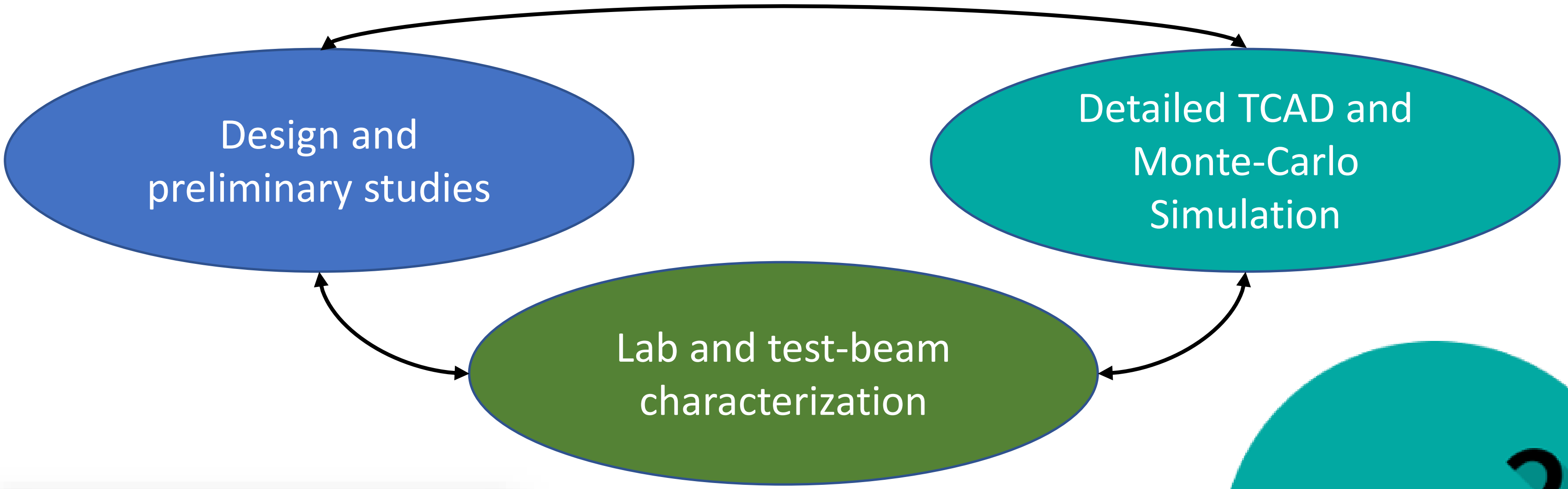
- **Pixel size** : 25 x 25 μm^2, σ_{SP} ~ 3μm
- **Timing resolution** : < 5 ns
- **Material**: 0.2 % X_0 / layer
- Moderate **radiation exposure** :
  NIEL: < $10^{11} n_{eq}/cm^2/y$
  TID: < 1 kGy / year

A large area tracker (140m^2)



- **Pixel size** : 50 μm x O(mm) , σ_{SP} ~ 7μm
- **Timing resolution** : < 5 ns
- **Material**: 1-2 % X_0 / layer
- **~140m^2** of instrumented surface !

Vertex and tracking R&D cycles

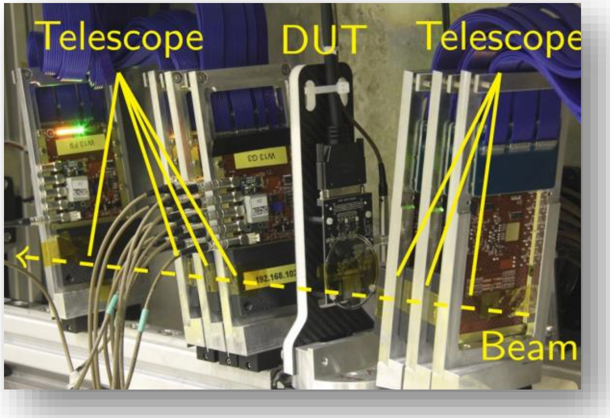


Design and preliminary studies

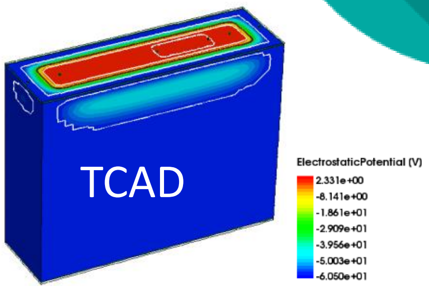
Detailed TCAD and Monte-Carlo Simulation

Lab and test-beam characterization

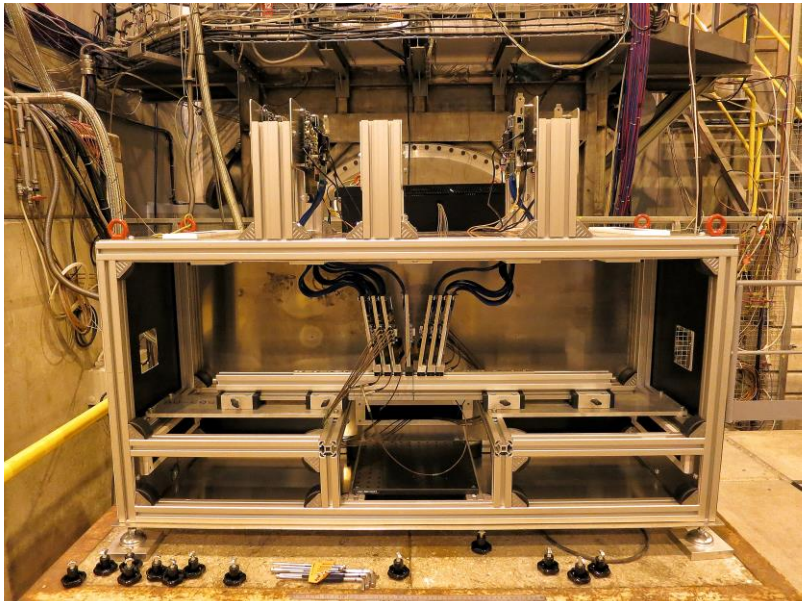
Our toolbox



Timepix3 Telescope @ SPS
and **Caribou universal readout**

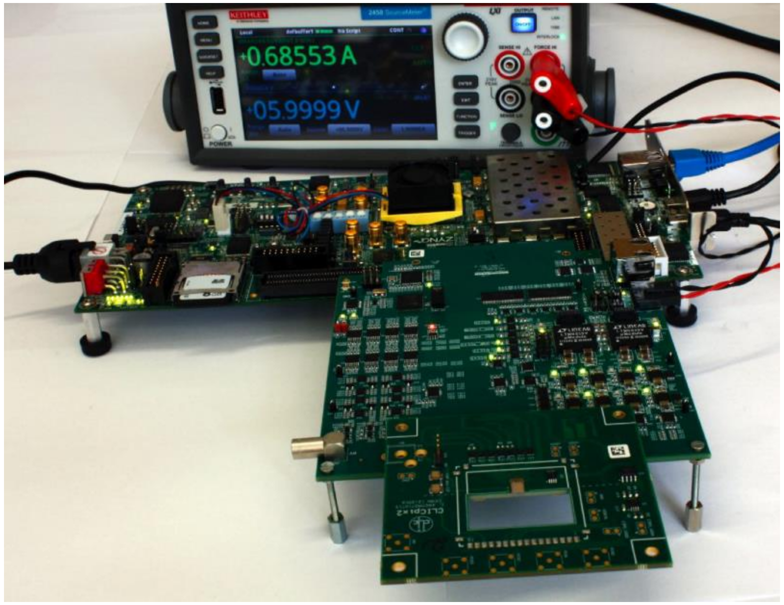


Tools: The CLICdp Timepix3 Telescope and Caribou readout



The CLICdp Timepix3 telescope

- 7 x Timepix3 telescope planes
- Continuous readout
- ~1.2ns time resolution on tracks
- ~2 µm resolution at the DUT
- Flexible mechanics with rotation stages for angle study



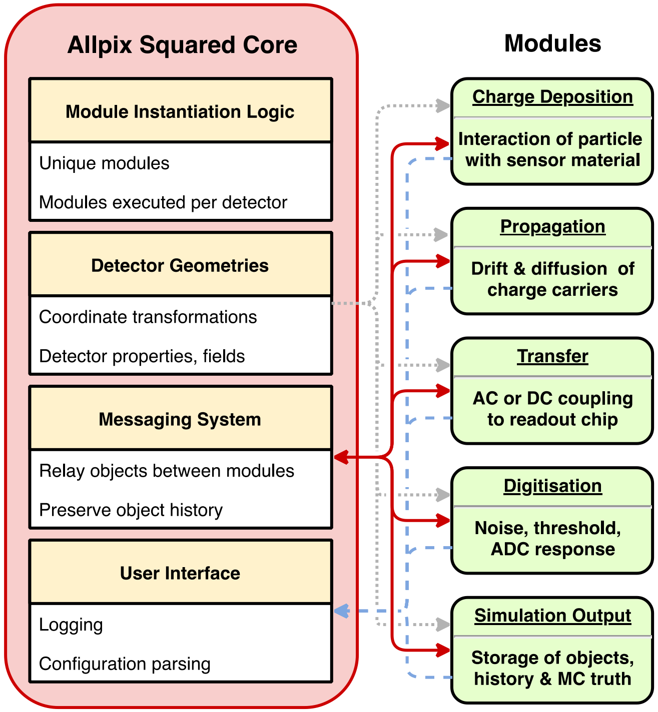
The CaRIBOu universal readout framework

- Multi-chip modular r/o framework
- Stand-alone system based on Zynq SoC running YOCTO Linux
- Peary generic DAQ software
- Generic CaR board for powering and monitoring of DUT
- Implementation for CLICPix, CCPDs, ATLASPix, FEI4, H35DEMO and more …

Tools : Allpix^2

CERN.CH/allpix-squared

- A **Modular, Generic** Simulation Framework for pixelated Detectors
  - Generic simulation of pixel,strip detectors
  - Simple text base description of the geometry, simulation parameters
  - Charge transport and TCAD Electric Field import facilities
  - Visualisation and digitisation
  - Output in popular formats (EUDET,PROTEUS, Corryvreckan, etc..)
  - Provided pre-compiled,via CVMFS, Docker
  - Continuous integration and unit test



Allpix Squared Core

Module Instantiation Logic
Unique modules
Modules executed per detector

Detector Geometries
Coordinate transformations
Detector properties, fields

Messaging System
Relay objects between modules
Preserve object history

User Interface
Logging
Configuration parsing

Modules

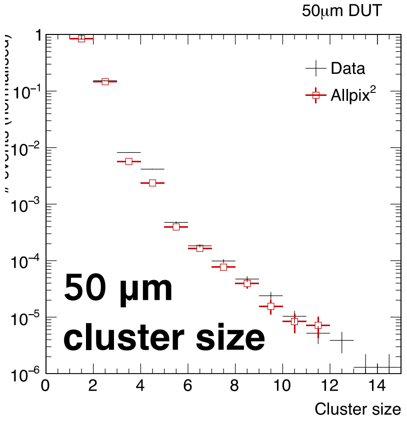
Charge Deposition
Interaction of particle with sensor material

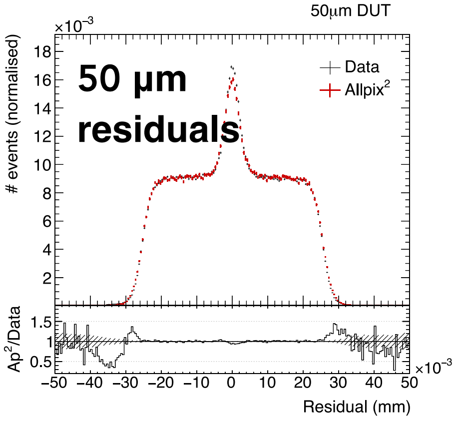
Propagation
Drift & diffusion of charge carriers

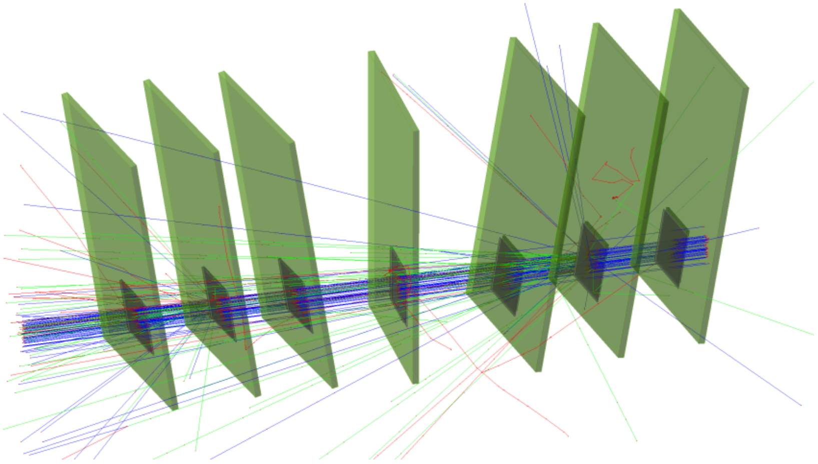
Transfer
AC or DC coupling to readout chip

Digitisation
Noise, threshold, ADC response

Simulation Output
Storage of objects, history & MC truth



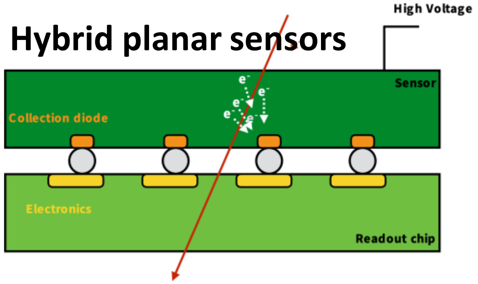




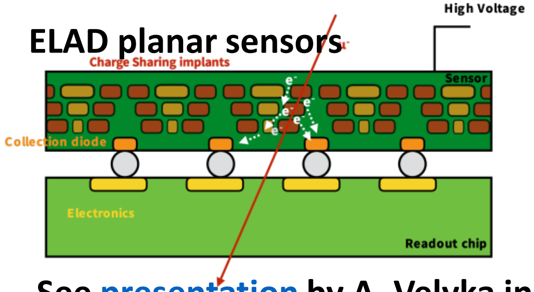
Nuclear Inst. and Methods in Physics Research, A 901 (2018) 164–172

CLIC Vertex and tracker technologies

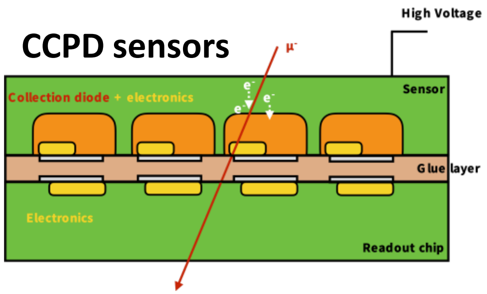
Hybrid planar sensors



ELAD planar sensors



CCPD sensors

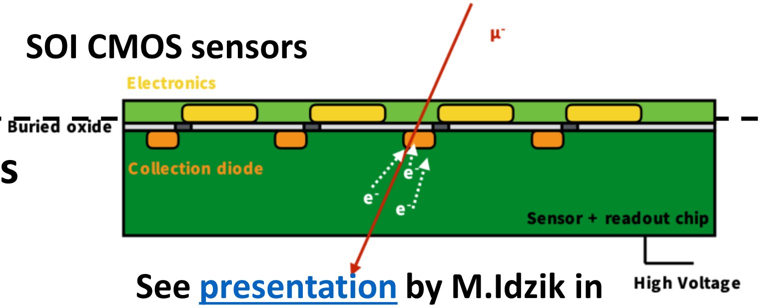


See [presentation](#) by A. Velyka in previous session for details on ELAD

Hybrid sensors

Monolithic sensors

SOI CMOS sensors

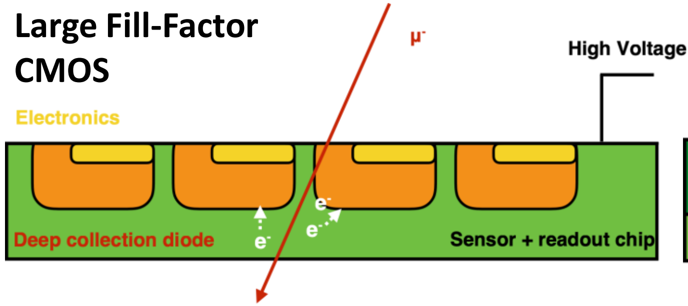


See [presentation](#) by M.Idzik in previous session for more details

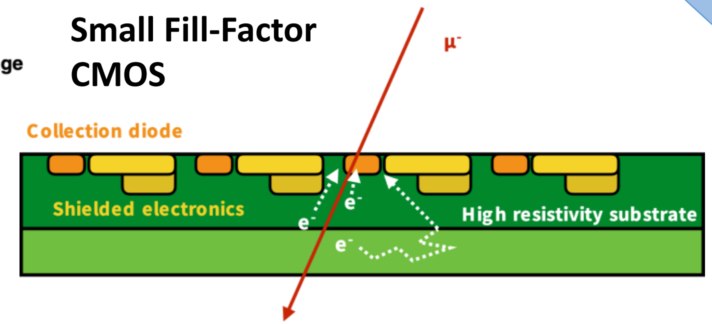
Sensor-ASIC integration

- Lower material
- Large area production possible
- Trade-off between performance and integration

Large Fill-Factor CMOS



Small Fill-Factor CMOS



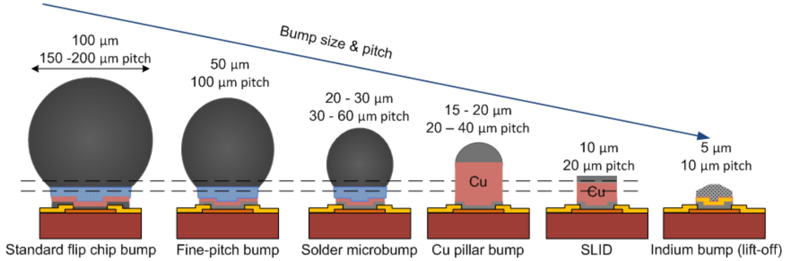
Hybrid planar sensors

The CLICPix2 ASIC

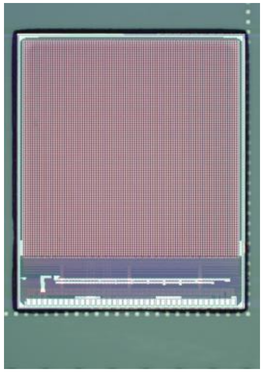
- Timepix/Medipix chip family
- **65nm** CMOS Technology
- 128x128 pixels, **25x25 µm^2**
- **5 bit TOT and 8 bit TOA** for each pixels
- Shutter based readout with data compression
- **Power Pulsing** of matrix and readout block

Hybridization and testing

- FBK and Advacam Active edge sensors produced with CLICPix2 footprint
- Bumping performed by **IZM** using **SnAg** bumps and handle wafers -> Challenging !
- Best assemblies with <**0.5%** of **unresponsive or disconnected** bumps
- Test beam characterization ongoing



See A. Nürnberg 2016 JINST 11 C11039 for testbeam results on CLICPix



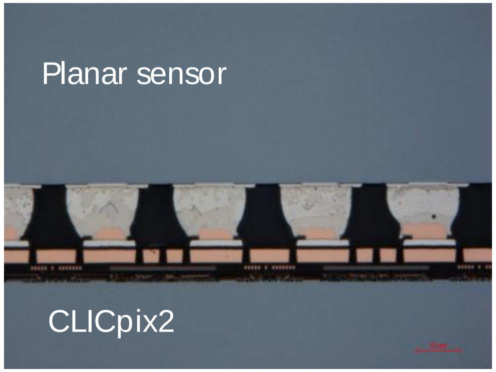
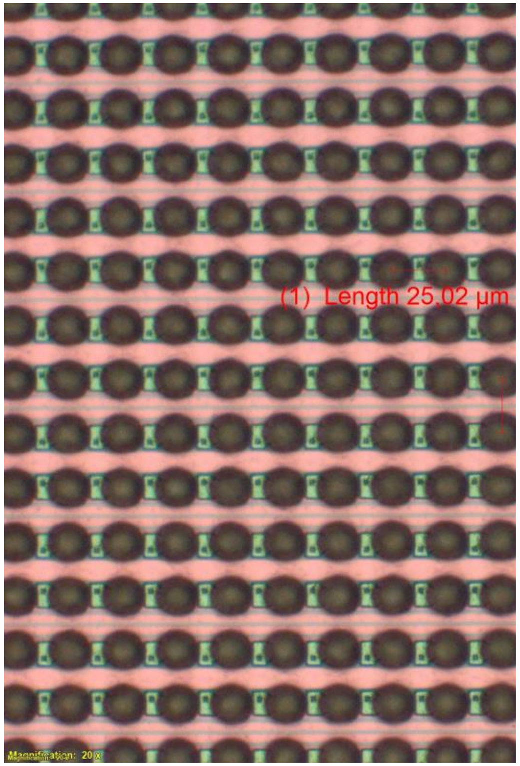


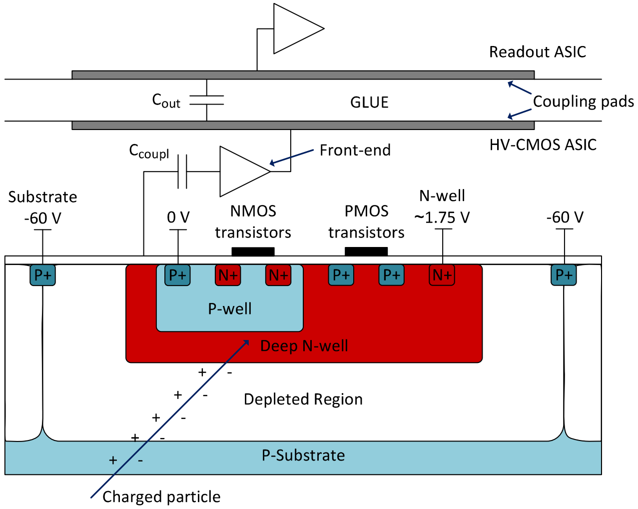
Image of a bumped CLICpix2 ASIC from IZM:



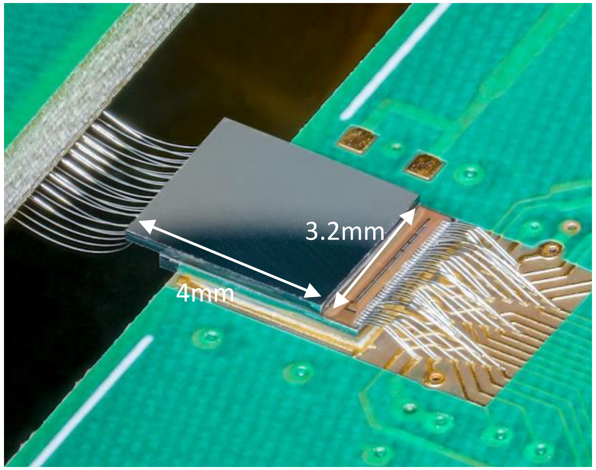
Capacitively-Coupled Pixel Detectors (CCPD)

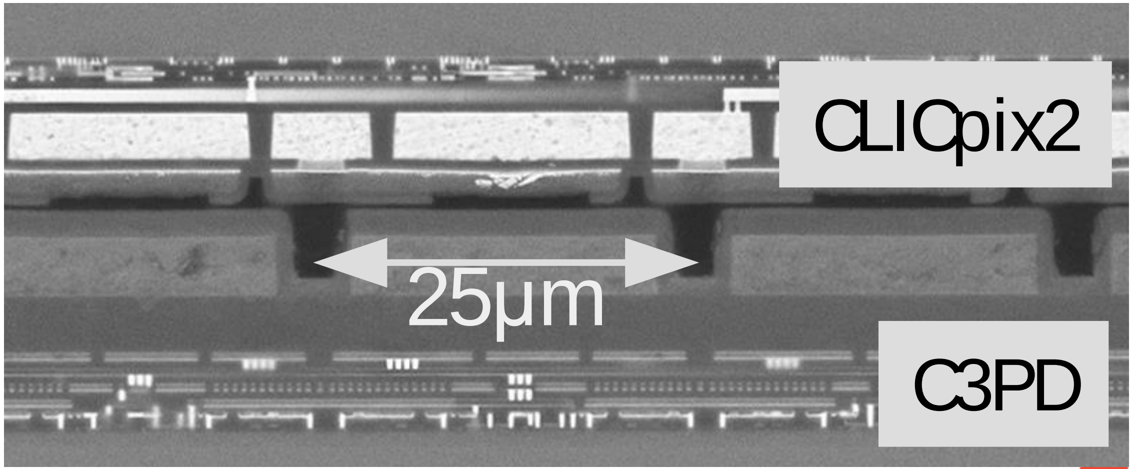
(CCPDv3)C3PD+CLICPix(1)2

- **2 sensors, CCPDv3 and CLIC CCPD (C3PD)** were designed in ams aH18 HV-CMOS technology
  - (64x64) 128x128, 25x25 μm^2 pixels
  - Substrate resistivity from **20 to 200 Ωcm**
- First **amplification layers integrated in sensors** to provide large signal at output
- **I^{2}C 2-wire slow-control** interface (C3PD)
- Coupling with ASIC done through a **very thin layer of glue** forming a capacitor (Low mass!)
  - Glueing method developed to using **flip-chip** assembly to acheive down to **100 nm glue layers**
  - **Fast prototyping method** wrt planar sensors



Nucl. Instrum. Methods Phys. Res., A 823 (2016) 1-8
PhD Thesis M. Buckland CERN-THESIS-2018-114
I. Kremastiotis 2017 JINST 12 C12030
M Vicente et al., CLICdp-Note-2017-003

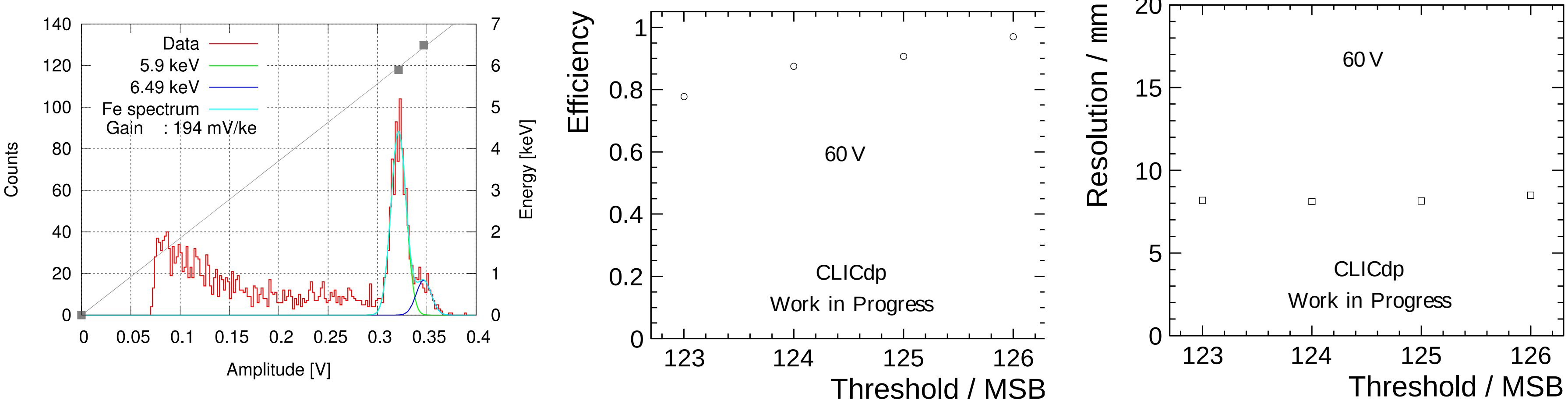




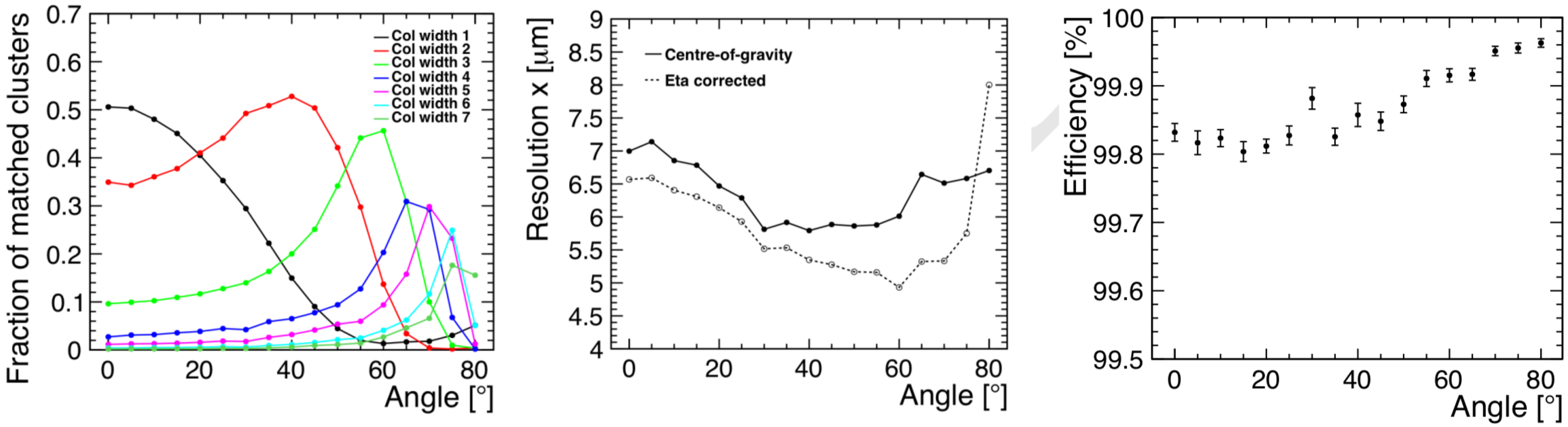
Also demonstrated on large (2x2 cm^2) area : 2018_JINST_13_P12009

Capacitively-Coupled Pixel Detectors (CCPD)

Tracking performance and energy resolution (C3PD)



Tracking performance versus track angle of incidence (CCPDv3)



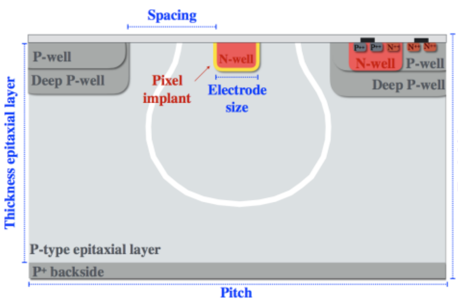
CERN-THESIS-2018-114

Small-Fill factor CMOS sensors

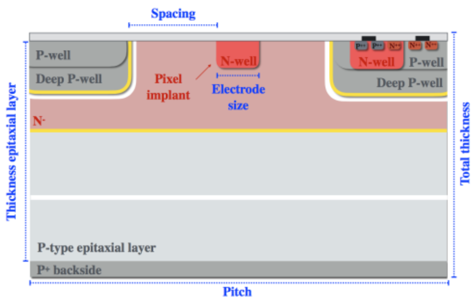
CMOS electronics integrated in **p-well separated from collection electrode**:

- Minimisation of **diode size**
- Minimisation of **sensor capacitance** down to ~ fF (large S/N)
- Process modifications to achieve **full lateral depletion** (W. Snoeys et. al)
- Further modifications proposed to improve timing and radiation hardness, see Monday presentation by M. Munker

HR CMOS standard process:



HR CMOS modified process:

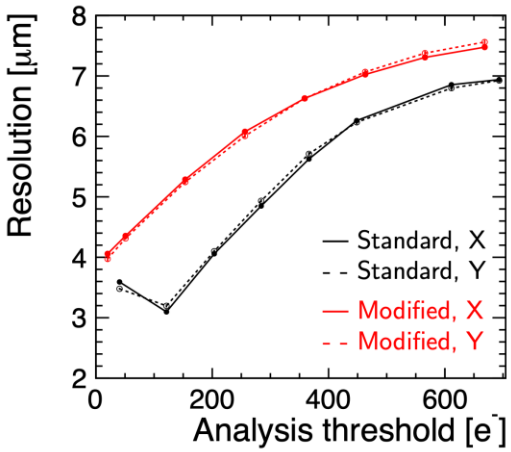


Investigator analogue test-chip:

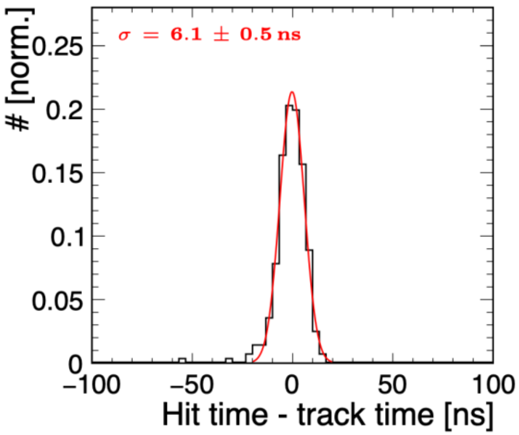
- Analogue test-chip developed for ALICE ITS upgrade, produced in 180 nm CMOS imaging process
- Various pixel layouts implemented in different pixel layouts, electrode to pwell spacings

Test-beam results for both process variants:

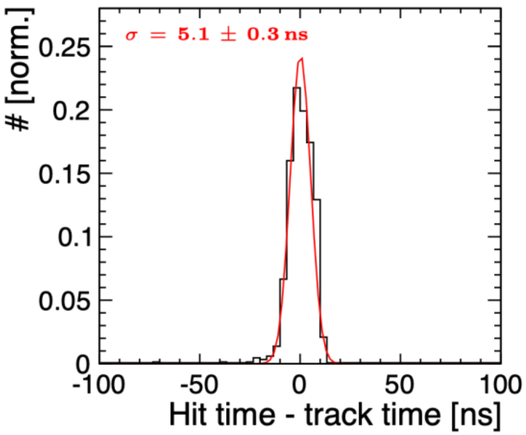
- **Spatial resolution ~ 7 µm** for threshold values of ~400e
- **Fully efficient operation** to threshold values below ~400e
- **Timing resolution ~ 6 ns** (limited by readout)



Standard process:

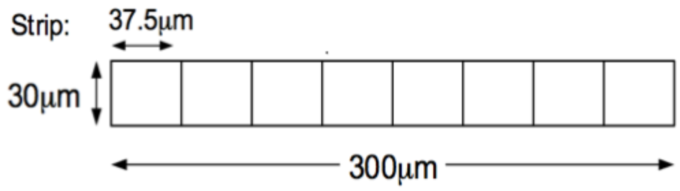


Modified process:



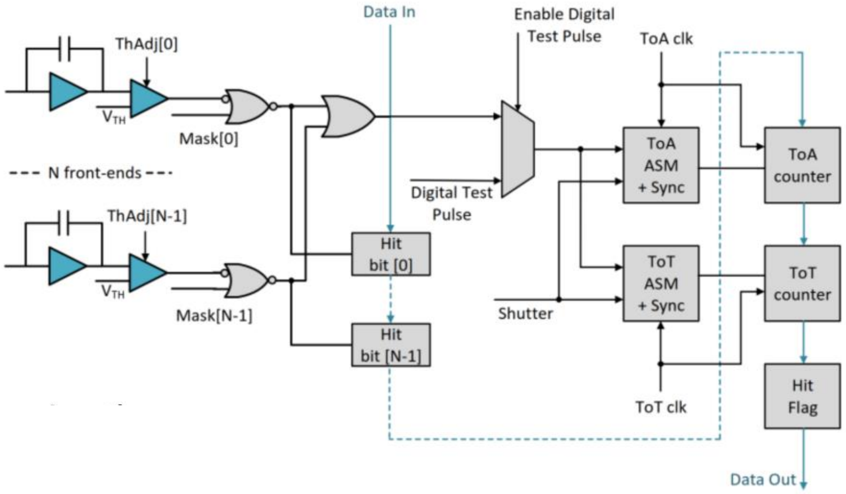
PhD Thesis M. Munker CERN-THESIS-2018-202

Small-Fill factor CMOS sensors: CLICTD



Promising results of 180 nm HR CMOS imaging process trigger design of fully monolithic CLIC tracker chip:

- **Super-pixel segmented in high granular collection diodes** to maintain fast charge collection while reducing digital logic
- Super pixel size of **30 µm x 300 µm**
- Diode size of **30 µm x 37.5 µm**



Diode discriminator outputs combined in 'OR' gate:

- 8-bit ToA and 5-bit ToT measurements
- Storage of **hit-pattern**
- 100 MHz clock for **10 ns time binning**

Different operation modes:

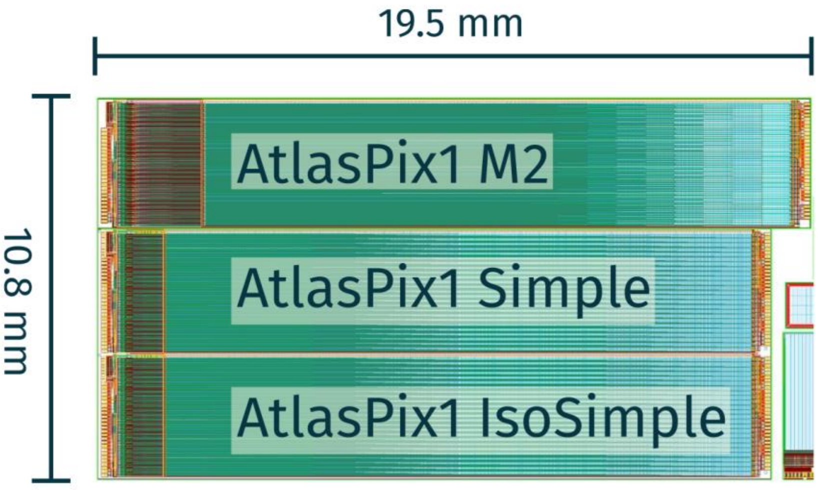
- 8 bits time stamping information (ToA) + 5 bits energy information (ToT)
- 13 bits time stamping information (ToA)
- 13 bits photon counting (number hits that are above threshold)

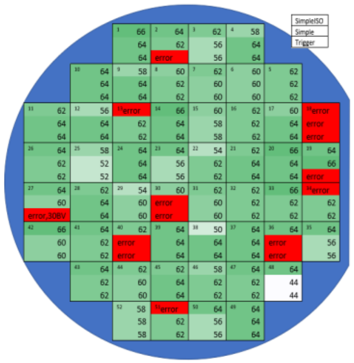
Design completed, UVM Verification ongoing

Large Fill-Factor CMOS sensors

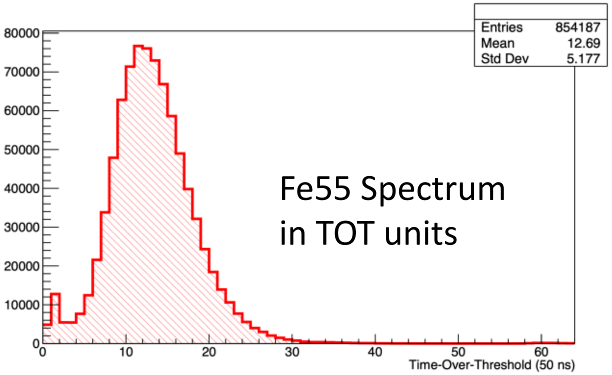
Implementation of fully **monolithic** sensors in ams aH18 process using high-resistivity wafers

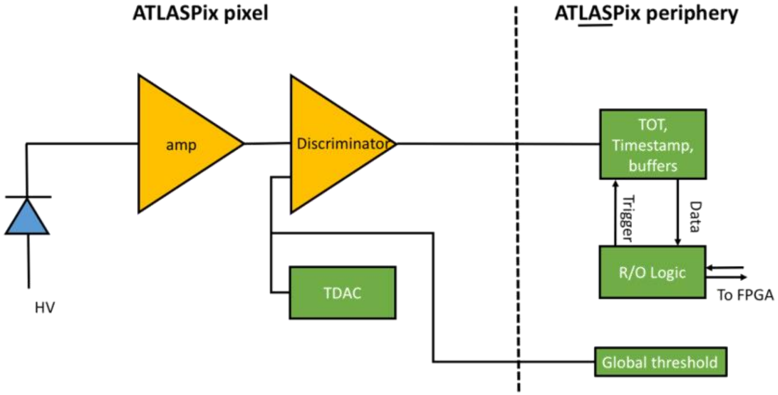
- **180nm HV-CMOS Engineering run** on **20-200 Ω cm substrate**
- Thinned down **to 60 µm**
- **130x40 µm²** pixels, 25x400 pixels
- **6 bit TOT** and **10 bit TOA** (up to 16 ns)
- Uniform breakdown across wafers at **60-85V**
- **Threshold** down to **600e, 120e dispersion**
- **Full length** column sensor (1.9cm)
- **Trigger-less** readout
- Serializer, **PLL**, High-Speed data transmission **(1.25Gbps, aurora 8b/10b)**
- Initially design for ATLAS , **Radiation hard up to >1x10^{15}n$_{eq}$/cm^2, 100MRad**
- **Close** to CLIC Requirements





Breakdown voltage on wafer

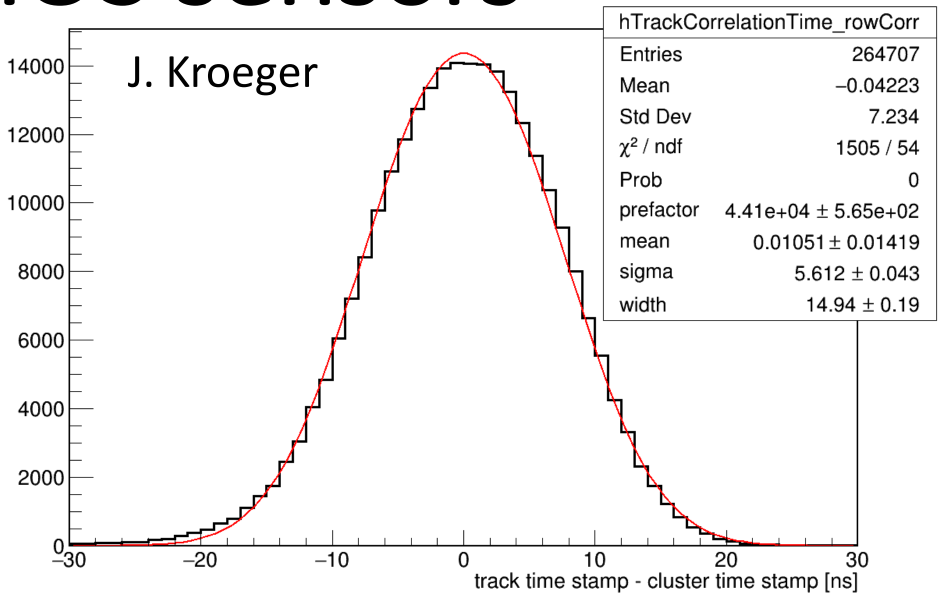


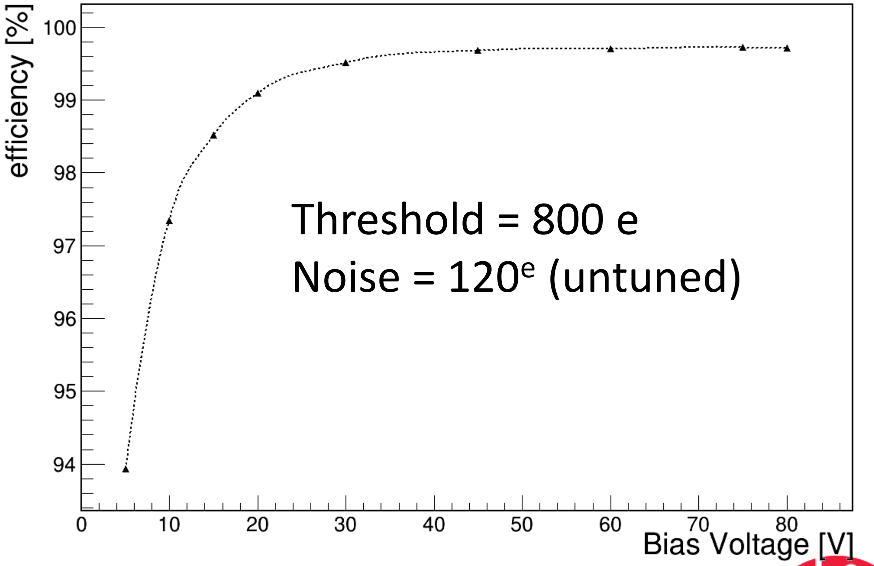


I. Peric et al., A high-voltage pixel sensor for the ATLAS upgrade, Nucl. Instrum. Meth. (2018), in press, DOI: 10.1016/j.nima.2018.06.060.

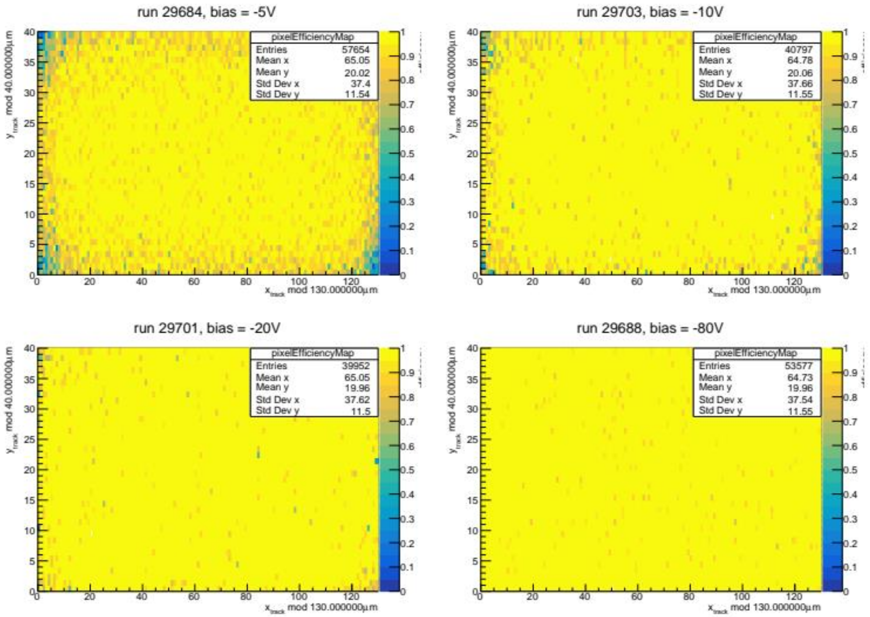
Large Fill-Factor CMOS sensors

- ATLASPix was tested in beam at FNAL, CERN SPS using the FEI4 and Timepix3 telescopes
  - Operated with **16 ns timestamp granularity**
  - Known row delay dependence corrected
  - **Timing resolution ~ 7ns measured**
  - **Spatial resolution : ~12µm in row direction**
  - **Efficiency at 0º >99.5%, no pixel masked**
  - **Noise << 10^{-6}/25ns**


J. Kroeger

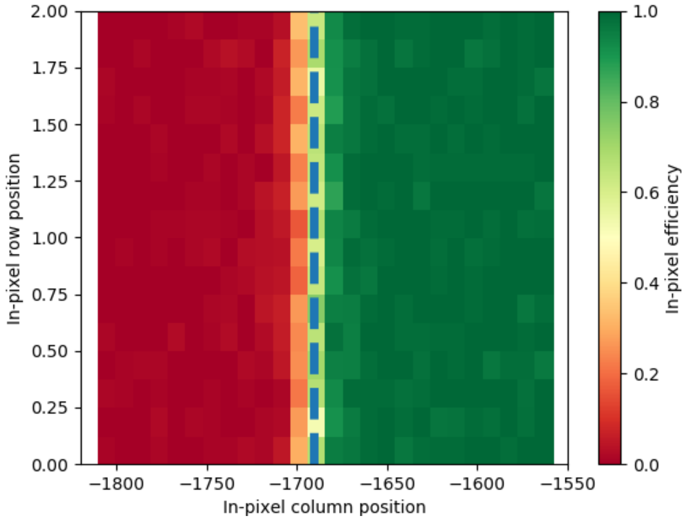

Threshold = 800 e

Noise = 120^{e} (untuned)

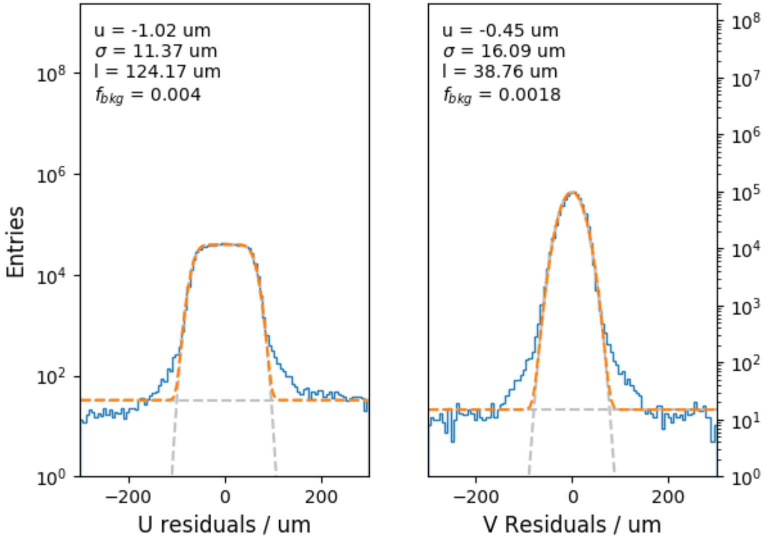


In-pixel efficiency

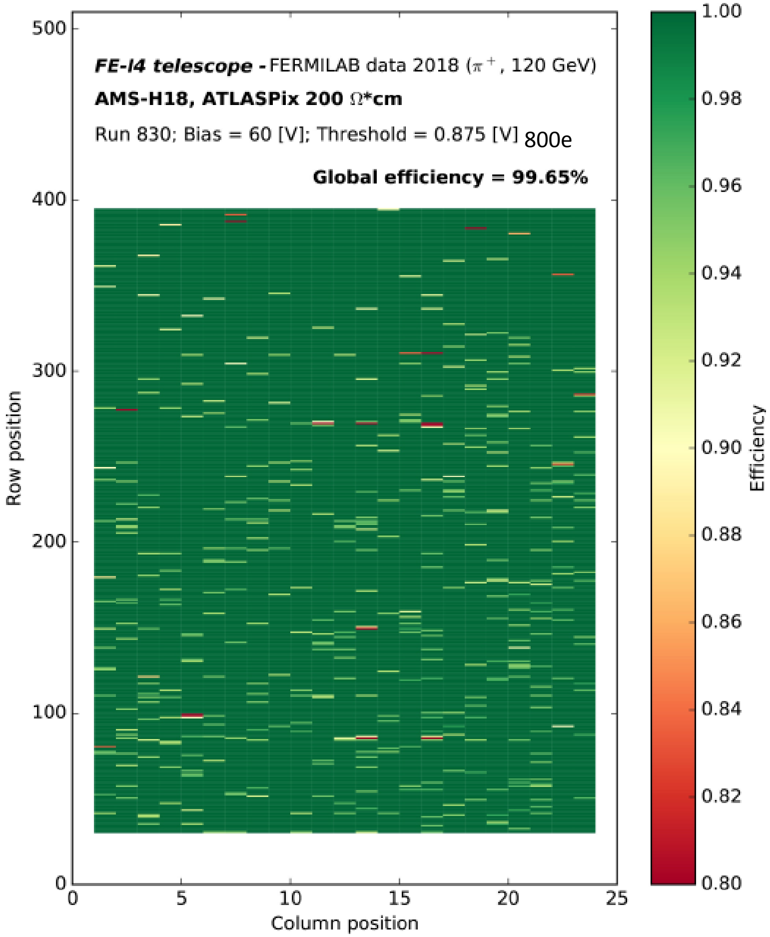
Large Fill-Factor CMOS sensors



Edge efficiency



Residuals



Following promising results, a CLIC compatible chip with modified pitch ans 10 ns timestamp to be submitted in 2019!

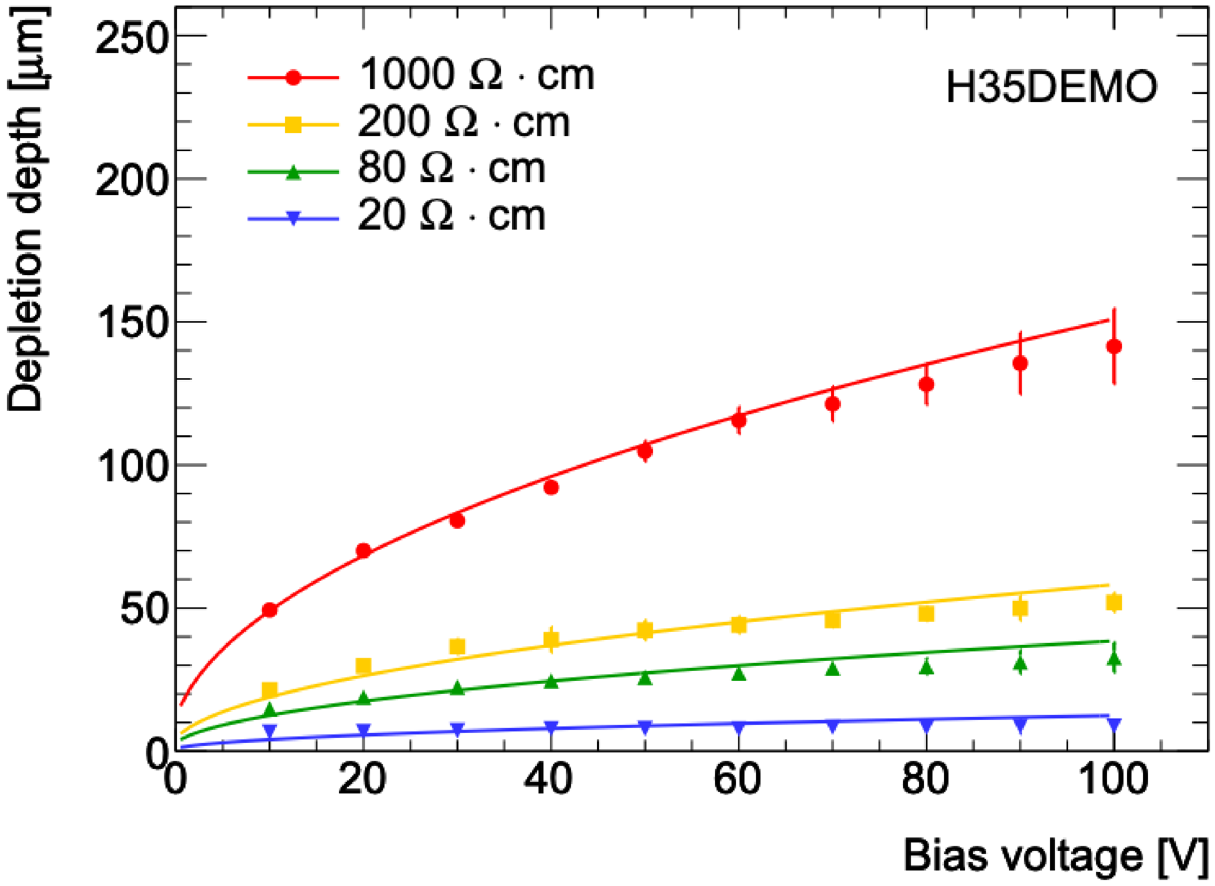
Conclusion

- The CLIC accelerator and the proposed physics measurements impose strict requirements on the vertex and tracking detector:
  - good single point resolution, low material budget
  - High occupancy requiring fine timestamping of hits

- The CLICdp vertex and tracking R&D focus on studying the available pixel detector technologies through simulation and characterization
  - Allpix^2 and TCAD simulation tools used to gain understanding of the devices
  - The Timepix3 telescope is used to characterize existing devices and evaluate their performances
  - Many devices studied : Planar sensors with fine pitch, ELAD Sensors, CCPDs, SOI pixel detectors , and CMOS sensors with small and large fill factor
  - Our device study allowed to identify promising technologies for CLIC vertex and tracker

backup

depletion


Depletion depth [µm]
250
200
150
100
50
0
0
20
40
60
80
100
Bias voltage [V]
1000 Ω · cm
200 Ω · cm
80 Ω · cm
20 Ω · cm
H35DEMO

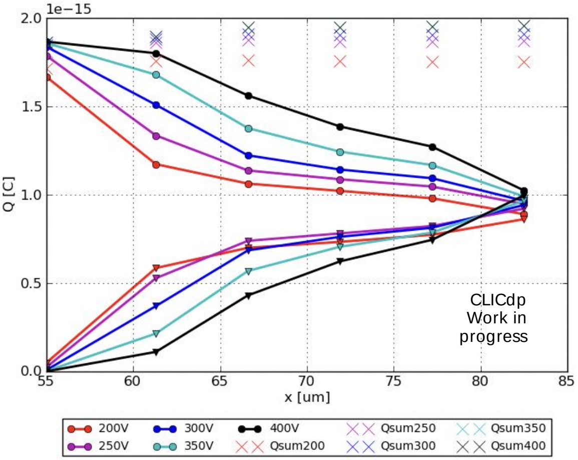
Enhanced Lateral Drift sensors (ELAD)

Concept to improve spatial resolution for thin sensors, H. Jansen (DESY/PIER):

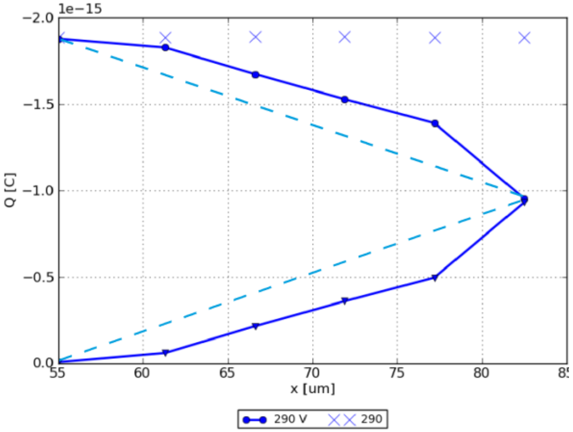
- Deep implants to shape electric field lines in sensor
- Suggestive epitaxial layer grow and implantation
- Increased “linearised” charge sharing

Results of TCAD simulations show increased charge sharing for given pitch & thickness -> Production of wafer with various deep implant doping ongoing

TCAD simulations for p-type ELAD:

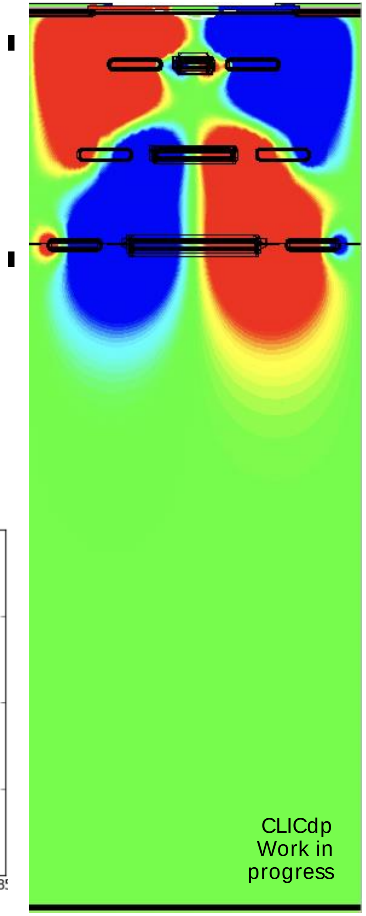


Allpix² validation



290V

Lateral 3lectric field:



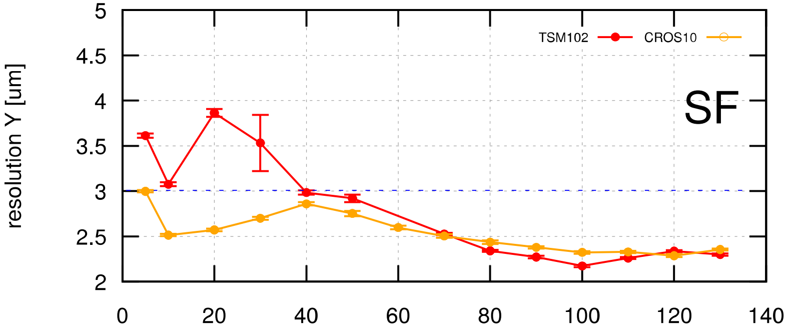
Current from MIP:

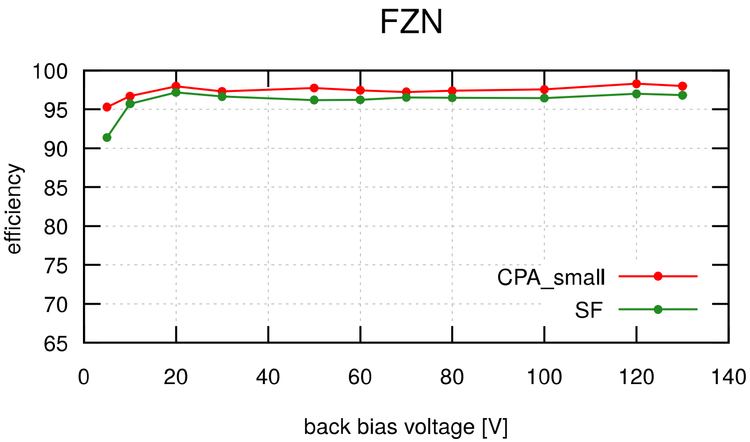
See presentation by A. Velyka in previous session for details

Patent DE102015116270B4

SOI sensors

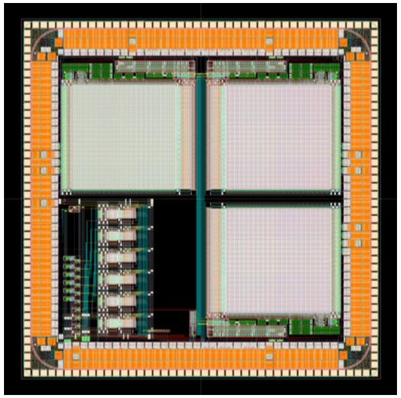
- **Monolithic integration** with sensor electronics separated fr high-resistivity substrate by Oxide layers
- Cracow SOI test chip in **200nm LAPIS SOI process**, different parameters:
  - >= 30 x 30µm^2 pixels
  - single-SOI and double-SOI wafers
  - different readout schemes implemented
- First test beam results for 500 µm thickness
  - SOI HR-CMOS: 30x30 µm^2 pitch, **Efficiency > 97%, σ_{SP} = 2µm**

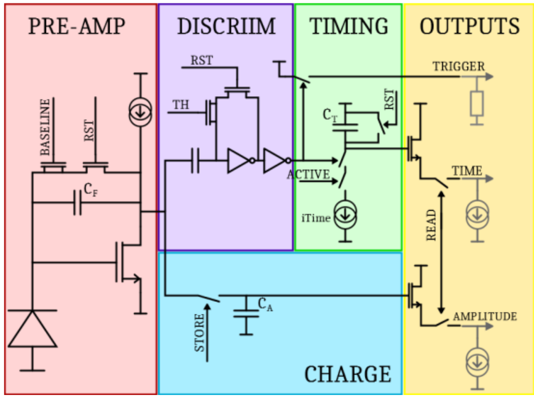




CLIPS : CLICPixel SOI in production

- 4.4 × 4.4 mm (previous 2.9 mm)
- Targets
  - spatial resolution <3 µm
  - time resolution <10 ns
- Analog charge and time information in **storage capacitors in each pixel**
  --> **no need for fast clock distribution** into matrix
- Snapshot analog **readout between bunch trains** with external ADC
- Timing reference base on **tuned current source**





See presentation by M.Idzik in previous session for more details

CCPD Assembly process

CCPD + FEI4 unwrapping in clean room , Visual inspection

Surface cleaning of chip with IPA/DI water to remove macro-dust elements

CCPD + FEI4 Plasma cleaning with Argon plasma

CCPD + FEI4 Flip-chip alignment

Glue pattern dispensed on chip using translating stages and time-pressure dispenser inside the flip-chip

Bonding : 2kg for 4 cm^2, 6 min at 100C, 1 min for irradiated + 24h at RT

CCPD Assembly process (In parallel)

Araldite 2011 Two-component mixing

Injection of glue in syringe

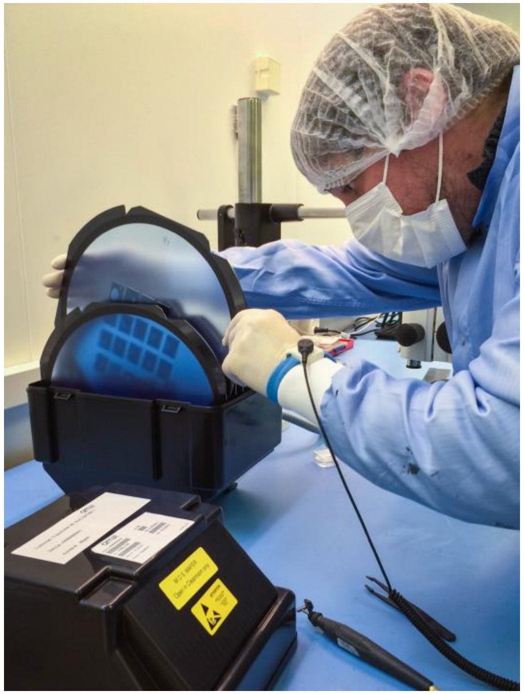
Centrifugation of glue to remove aire bubbles

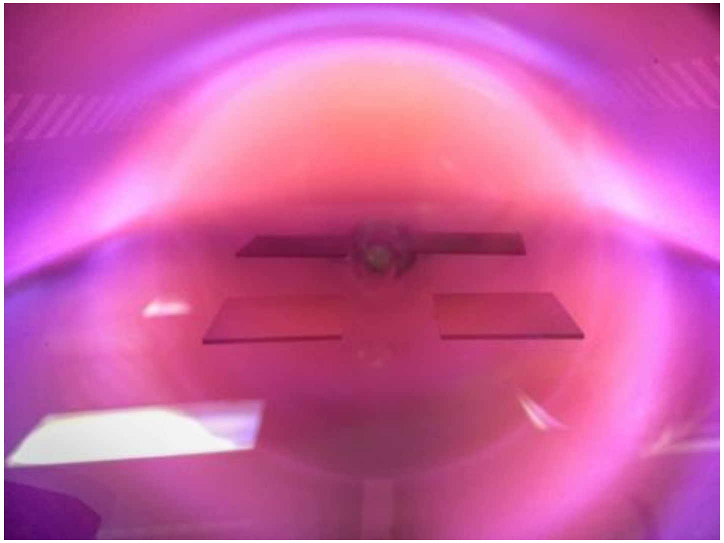
Installation of syringue in Flip-Chip machine

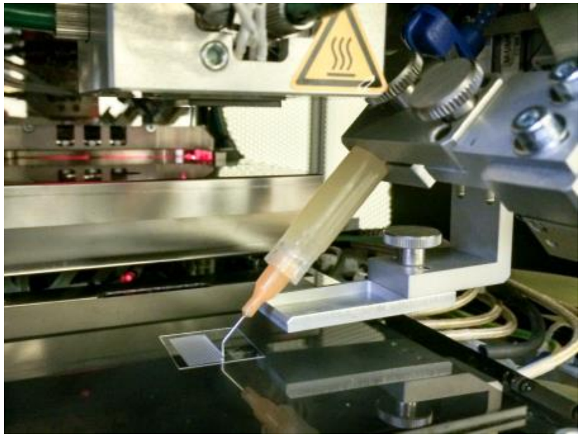
Alignment of syringue tip to machine coordinates (need to dispense one drop of glue)

Ready for glue dispense for 100min

CCPD Assembly process



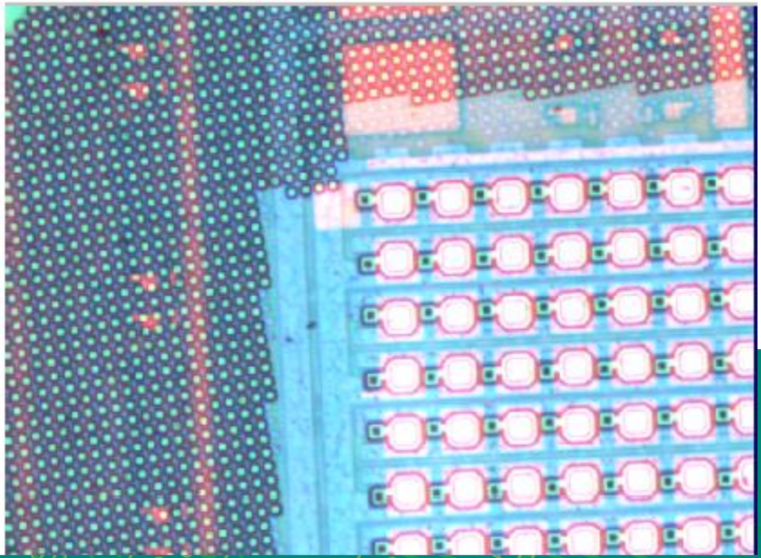


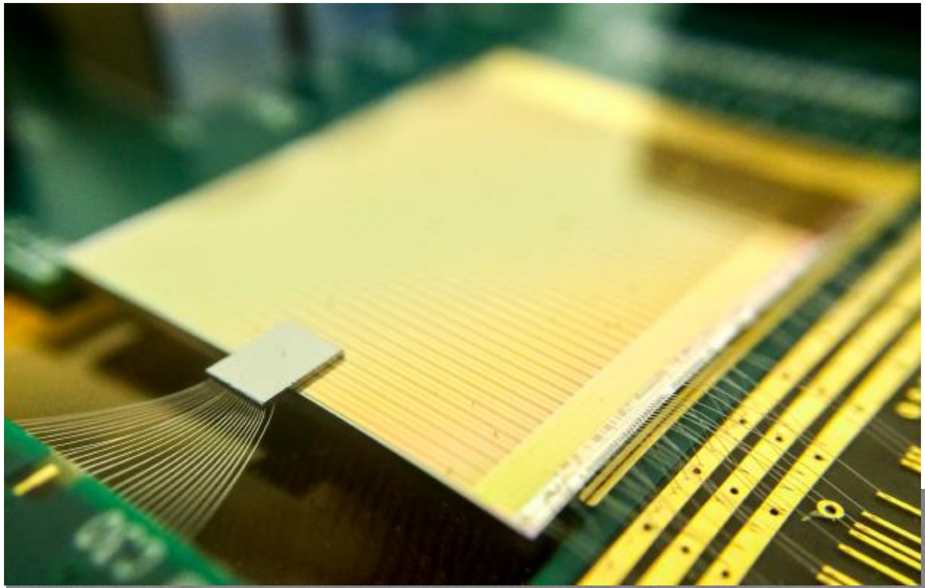


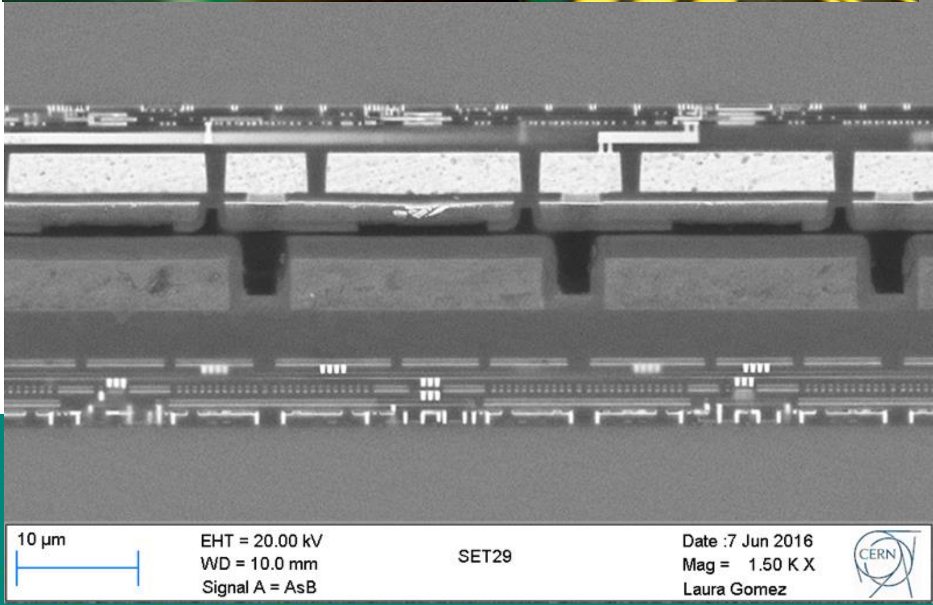
CCPD Assembly process

After assembly, we achieve routinely glue thickness of < 500nm with a variation of 100nm across 2cm

#	*align1* [μm]	*align2* [μm]	*align2 - align1* [μm]
4	2.13	2.13	1.41
5	3.54	2.03	1.57
6	3.77	2.36	1.31
7	3.88	1.85	2.03
8	2.56	3.36	-0.8

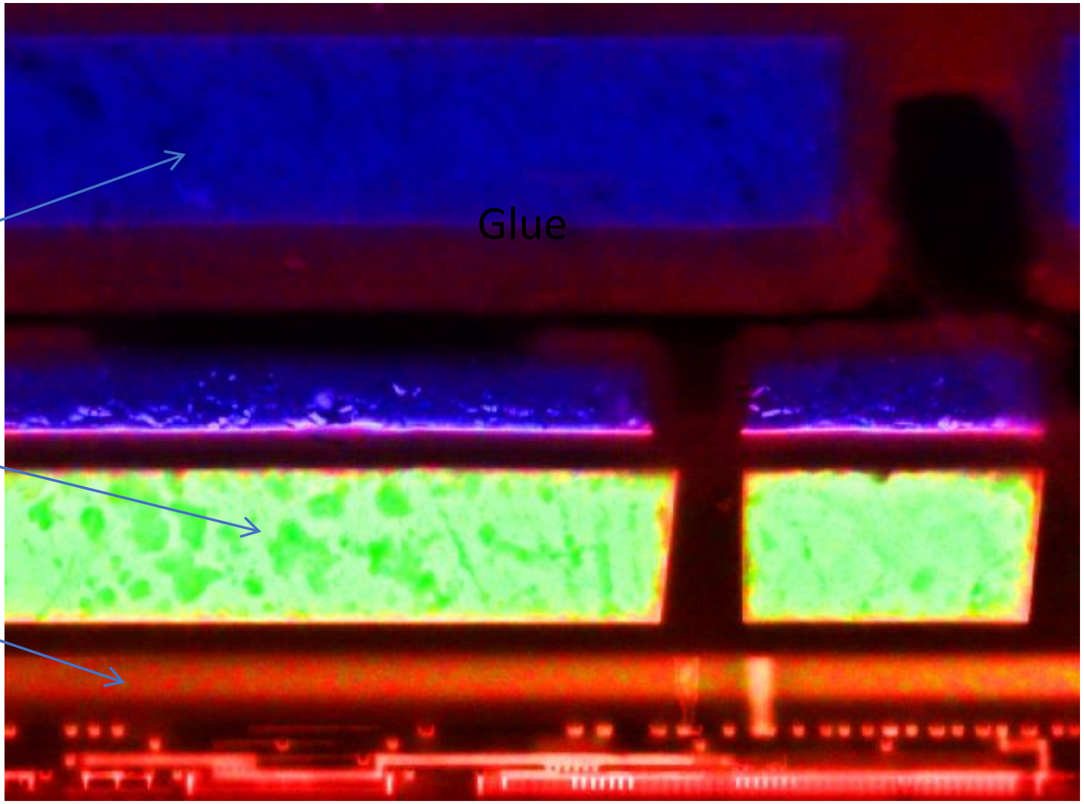






Glue layer thickness

Energy Dispersive X-Ray Spectroscopy was used to investigate which material are present in the cross section



Aluminium

Copper

Silicon

Glue layer thickness

Energy Dispersive X-Ray Spectroscopy was used to investigate which material are present in the cross section

Aluminium

Copper

Silicon