ATLAS ITk Pixel Detector Overview

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Outline

• The case for the ATLAS inner detector upgrade for the HL-LHC
• Pixel detector layout and performance
• Detectors and front-end electronics
• Mechanics and services
• Overall system aspects (Trigger and DAQ) and Outlook

Technical Design Report for the ATLAS Inner Tracker Pixel Detector
ATLAS-TDR-030 / CERN-LHCC-017-01

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ITK REQUIREMENTS AND LAYOUT
The HL-LHC upgrade

LHC / HL-LHC Plan

Current pixel detector
\[ L = 2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \]
\[ \int L = 300 \text{ fb}^{-1} \]

ITk pixel detector
\[ L = 7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \]
\[ \int L = 4000 \text{ fb}^{-1} \]
HL-LHC Physics Goals

- Rich physics program including:
  - Vector Boson Scattering
    - and other precision SM measurements
  - Higgs pair production
    - and precision Higgs boson properties
  - Beyond Standard Model searches

- Many reconstruction challenges:
  - High multiplicity events, highly boosted jets:
    - improve granularity and resolution
  - Rare events
    - improve in coverage and reconstruction efficiency

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ITk requirements

Completely new inner detector
- full silicon tracker (TRT will have 100% occupancy)

- Keep occupancy at few % level
  - Increase granularity by 8× for the pixel, (5× with respect to the insertable B-layer)
  - expand pixels to a larger radius
- Increase data rate capability

- Radiation hardness for 4000 fb⁻¹:
  - Non ionizing energy loss (NIEL) up to \( \Phi_{eq} = (2.5-3)\times10^{16} \text{ n/cm}^2 \).
  - Total ionization dose (TID) up to 20 MGy

Average hits / readout chip / event at 200 pile-up

<table>
<thead>
<tr>
<th>(Ring) Layer</th>
<th>Flat Barrel</th>
<th>Inclined Barrel</th>
<th>End-cap</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>223.0</td>
<td>136.7</td>
<td>80.9</td>
</tr>
<tr>
<td>1</td>
<td>26.6</td>
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<tr>
<td>2</td>
<td>19.3</td>
<td>20.1</td>
<td>21.0</td>
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<tr>
<td>3</td>
<td>12.9</td>
<td>12.7</td>
<td>13.3</td>
</tr>
<tr>
<td>4</td>
<td>9.9</td>
<td>9.1</td>
<td>9.3</td>
</tr>
</tbody>
</table>

from 24 Mhits mm⁻²s⁻¹ to 0.1 Mhits mm⁻²s⁻¹
ITk requirements

- Improve resolution and robustness compared to the present detector:
  - track reconstruction efficiency >99% for muons, >85% for electrons and pions
  - fake rate < $10^{-5}$
  - robustness against loss of up to 15% of channels
ITk layout

• Strips at outer radii, pixels near to the interaction region
• Cover with at least 9 measurements tracks up to $|\eta|=4$

• Pixel detector:
  – 12.7 m$^2$, 5×10$^9$ channels
  – 50×50 μm$^2$ or 25×100 μm$^2$
  – **inclined modules** and **individually placed disks**
    • minimize material and maximize resolution while keeping full coverage
  – inner section replaceable after 2000 fb$^{-1}$
The active components

SENSORS AND FRONT-END
Hybrid module structure

• Baseline design mainly consists of $\sim 4 \times 4$ cm$^2$ “quad hybrid” modules:
  – one sensor segmented into either $50 \times 50$ μm$^2$ or $25 \times 100$ μm$^2$ pixels
  – read out by four FE chips, each with $384 \times 400$ channels

A lot of experience from current detectors, but needs to scale up a factor 10 in total production
Sensor technologies

- One front-end for the whole detector
  - RD53 collaboration: joint ATLAS and CMS effort on common 65 nm design
  - Requirements given by the innermost layers

- Sensor technology baseline optimized according to radiation hardness, cost and foundries production capability

![Diagram of ATLAS Simulation](image)

**Inner section:**
- L1+R1 100 µm planar
- L0+R0 3D

**Outer barrel and encaps:**
- L2-4+R2-4
- 150 µm planar

**ATLAS Simulation**
- $\eta = 1.0$
- $\eta = 2.0$
- $\eta = 3.0$
- $\eta = 4.0$
3D Sensors

- Innermost layer: $1.3 \times 10^{16} \text{n}_{eq}/\text{cm}^2$ for 2000 fb$^{-1}$
  - 150 µm thickness + 100 µm support wafer
  - Single-chip dies $\sim 2 \times 2$ cm$^2$
  - Sensor produced at FBK, CNM and Sintef
    - 50×50 µm$^2$ assessed
    - 25×100 µm$^2$ to be verified with RD53A assembly: radiation hardness of 1 Electrode design vs. yield for 2 Electrodes design
Planar sensors

- Use n-in-p technology:
  - One side processing: reduced cost and easier handling
  - HV protection between sensor-edge and FE electronics:
    - BCB or Parylene under evaluation
- Thin sensors in inner section: \(4.5 \times 10^{15} \text{n}_{eq}/\text{cm}^2\) for 2000 fb\(^{-1}\)
  - Hit efficiency saturation at lower bias voltage: smaller leakage current and power consumption
  - Critical point is efficiency loss due to bias structures
  - Many vendors on the market: CiS, FBK, HPK, Lfoundry, Micron, VTT...
Sensor performance

3D CNM, Different Geometries, d=230 μm, 0° tilt

Planar sensor efficiency:
- grounded bias grid
- floating bias grid

$\phi = 1 \times 10^{16} n_{eq}/cm^2$ sensor thickness
- 100 μm (VTT)
- 130 μm (FBK)
- 150 μm (CiS)

Bias voltage [V]

ATLAS

Fluence $[10^{15} n_{eq}/cm^2]$

$V_{97\%}$ [V]
Front-end chip

- **RD53 Collaboration: joint ATLAS and CMS R&D**
  - 65 nm TSMC technology
  - Final size $\sim 2 \times 2$ cm$^2$ with $\sim 160k$ pixels
  - ATLAS version mid 2019, CMS version few months later
  - Heavy use of modern design technologies to implement complex readout logic:
    - Managing $\sim 223$ hits/chip/bunch crossing
    - Local memory for 500 bunch crossing trigger latency
    - $4 \times 1.28$ Gb/s links with data compression

- **RD53A FE demonstrator:**
  - Full width / half depth chip
  - Being used for qualification of:
    - Sensor design
    - Powering scheme and DCS
    - Module assembly and handling
Monolithic CMOS option

- **Depleted CMOS Detectors**
  - Charge collection by drift provides radiation hardness and timing resolution similar to planar sensors
  - Large electrode designs (AMS/TSI, Lfoundry) have consistently shown high efficiency after irradiation
  - Small electrode design (TowerJazz) very promising in terms of noise, time resolution and power consumption

- **Technically feasible for outermost layer**
  - "relaxed" requirements:
    - NIEL: $1.5 \times 10^{15} \text{n}_{eq}/\text{cm}^2$
    - TID: 0.8 MGy
    - ~10 hits/chip/bunch crossing
  - Large saving factor:
    - $L_4$ is 3 m$^2$, 30% of all thick sensor production
The path to performance

MECHANICS AND SERVICES
Material budget

- Reduction of material is the key to:
  - Resolution for low momentum particles
  - Tracking efficiency (dominated by interaction with the detector)

Improved design of services!
Local supports

- Lightweight carbon-carbon structures
- $\text{CO}_2$ evaporative cooling with Ti pipes
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Inner Endcap
Single or coupled disks
Serial powering

- Strong reduction in cable lines and material
- Up to 7A/8W on a quad-module
- Up to 14 modules in a single serial power chain
  - Need to provide a safety mechanism in case of module failure
  - Detector Control System:
    - Hardwired safety interlock
    - PSPP Chip + DCS Controller
    - Diagnostic information from FE

Serial Powering test chain
FE-I4 + PSPP chips
• Considering two trigger schemes:
  – 1 MHz 1-level trigger
    • 12.5 µs trigger latency
    • Fast track reconstruction for HLT
  – 4 MHz 2-level trigger
    • 25 µs readout latency
    • L1 track trigger (outer layers+strips)
Data transmission

- Output links at 5.12 Gb/s, with Aurora 64/62 encoding
- Concentrate the 1.28 Gb/s FE outputs near to modules
  - Position-dependent modularity
- Thin cables (twin-ax) till optoboards
- AC coupling: each FE is at different ground level due to serial powering.
Prototyping

Intense activity to prepare for the detector construction

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Conclusions

• The ITk Pixel Detector project is a non trivial challenge improve the high–performance devices already operating at the LHC:
  – 7× instantaneous luminosity
  – 13× integrated luminosity
  – 99.93% of solid angle coverage

• Innovation is required not only on the detector side, but also on services.

• About one year after the TDR the project is running at full speed to be ready for HL-LHC first collisions!
• Modeling Radiation Damage to Pixel Sensors in the ATLAS Detector
  – Marco Bomben, 11th December 16:20
• Performance of FBK/INFN/LPNHE thin active edge n-on-p pixel detectors for the upgrade of the ATLAS Inner Tracker
  – Giovanni Calderini, 11th December 11:10
• Characterization of RD53A compatible n-in-p planar pixel sensors
  – Anna Macchiolo, 11th December 11:35
• Study of efficiency and noise of fine pitch planar pixel detector for ATLAS ITk upgrade
  – Koji Nakamura, 11th December 12:25
• First CMS results on 3D pixel sensors interconnected to RD53A readout chip after high energy proton irradiation
  – Marco Meschini, 10th December Poster session

• Radiation-induced effects on data integrity and -link stability of RD53A
  – Marco Vogt, 11th December 17:35
• Module Development for the Phase-2 ATLAS ITk Pixel Upgrade
  – Dai Kobayashi, 10th December Poster session

• Results of larger structures prototyping for the Phase-II upgrade of the pixel detector of the ATLAS experiment
  – Susanne Kuehn, 13th December 17:35

• A 5.12 Gbps serial data receiver for active cable for ATLAS Inner Tracker Pixel Detector readout upgrade
  – Le Xiao, 10th December Poster Session
• R&D status of the Monopix chips: Depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS Inner Tracker upgrade
  – Ivan Dario Caicedo Sierra, 13th December 11:10

• MALTA: an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade
  – Roberto Cardella, 11th December 12:00

• Simulations of CMOS sensors with a small collection electrode improved for a faster charge-collection and increased radiation tolerance
  – Ruth Magdalena Munker, 10th December 12:25

• Performance of the ATLASPix1 pixel sensor prototype in ams aH18 CMOS technology for the ATLAS ITk upgrade
  – Moritz Kiehn, 13th December 12:00

• Electrical characterization of AMS aH18 HV-CMOS after neutrons and protons irradiations
  – D M S Sultan, 10th December 12:00

• Developments towards a Serial Powering scheme in a monolithic CMOS technology for the ATLAS pixel upgrade
  – Siddharth Bhat, 10th December Poster session
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