## International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2018)



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## ATLAS ITk Pixel Detector Overview

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For the high luminosity era of the Large Hadron Collider (HL-LHC) it is foreseen to replace the current Inner Detector of the ATLAS experiment with a new, all-silicon detector to cope with the increase in occupancy, bandwidth and radiation damage that result from the increase of the instantaneous luminosity by a factor of 5 to 7.5. The new Inner Tracker (ITk) will consist of an inner pixel and outer strip detector aiming to provide tracking coverage up to  $|\eta|$ =4. The layout of the pixel detector is foreseen to have five layers of pixel silicon sensor modules in the central region and several ring-shaped layers in the forward region. This results in up to 14 m² of silicon depending on the selected layout.

While the outer 3 layers of the Pixel Detector are designed to operate for the full HL-LHC data taking period, the innermost 2 layers of the detector will be replaced around half of the lifetime. The innermost layer of the ITk Pixel Detector will feature 3D silicon sensors, due to their inherent radiation hardness and low power consumption, while the remaining layers will employ planar silicon sensors with thickness ranging from  $100\mu m$  to  $150\mu m$ . All hybrid detector modules will be read out by novel ASICs, implemented in 65nm CMOS technology, which will be connected to the silicon sensors using bump bonding. With about  $4\cdot10^4$  pixels per cm² the bump bond density is a much higher than in previous hybrid detectors.

In order to reduce the amount of services needed, a serial powering scheme for the detector modules will be adopted. The pixel off-detector readout electronics will be implemented in the framework of the general ATLAS trigger and DAQ system with a readout speed of up to 5 Gb/s per data link for the innermost layers. The talk will give an overview of the layout and current status of the development of the ITk Pixel Detector.

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