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Development of a readout system for the pixel detector at HIRFL-CSR Internal Target Facility

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The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, inter-disciplinary science and relative applications. The internal target is built on the experiment ring of the HIRFL-CSR for high precision measurements. Due to the high spatial resolution, a Monolithic Active Pixel Sensor (MAPS) based pixel detector is expected to be a good candidate for the related experiments. In this paper, a versatile radiation-hard readout system has been designed for the tentative MAPS based pixel detector in HIRFL-CSR Internal Target Facility. The readout system consists of the front-end cards and the data aggregator. The front-end card reads data from the customized detector pads, where the MAPS is hosted, processes the data and sends it to the data aggregator through high speed serial link. In addition, the front-end card also provides clocks, power, configurable parameters, debug interface, etc. to the detector pads. To reduce the risk of radiation-induced failures, the Flash-based Microsemi Smartfusion2 FPGA has been chosen as the main FPGA on the front-end card. This FPGA was chosen due to its inherently single event effects tolerant configuration cells. The data aggregator receives data from the front-end cards and ships the data to the data computer through PCIe interface. This paper will present the design, implementation and first test results of this readout system.

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