Microelectronics for readout systems
The potential benefits of early engagement between CERN and the microelectronics industry.

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Abstract

3D electronics are used in the computing industry to improve memory. They could also potentially be used in the microelectronics readout systems in the LHC and HL-LHC. As research is being carried out both in industry and in HEP, it would be mutually beneficial if this research was carried out collaboratively.

1 Introduction

Microelectronics are of high importance in HEP for the readout of signals of recorded events. They are also of vital importance in modern computing, and are used in memory. This report will take a look at the history surrounding the R&D of radiation hard microelectronics for use at CERN, the need for 3D integration in HEP and industry, and will evaluate whether it could be mutually beneficial for academia and industry to carry out the R&D on 3D silicon chips collaboratively.

2 Developing Radiation Hard Electronics for the LHC

Microelectronics are an essential part of the readout systems at the LHC. Silicon-strip detectors, which are used for the accurate tracking of charged particle trajectories in the innermost parts of the detector, require readout electronics that are fast and low noise [1]. The silicon-strip detectors also need to withstand more than 10 Mrad of ionising radiation and a neutron flux of up to 10^{14} neutrons/cm^2 over a period of 10 years [2], hence it is vital that the technology used is radiation-hard.

In 1995, when we first saw the need for radiation hard electronics for the LHC, there were only three sectors that were really interested in radiation hardness: space, the military, and medicine. However, the electronics developed for medicine and space could only withstand up to 100 krad, with no proof that this could be increased to the levels of radiation hardness required. Additionally, whilst space only required a few hundred radiation hard chips, the LHC needed at least one million, which led to problems of scale and cost. Although the military electronics could withstand higher levels of radiation, the technology was heavily protected, and it was also very expensive due to the small market. So CERN had to begin looking at alternative solutions.

One potential solution was to take a look at commercial technology, and modify the manufacturing process to make it radiation hard. This led to the production of DMILL - a radiation hard technology that was developed by a CEA-LETI collaboration, and sold to CERN by Amtel. However, the issue with this special process was that it was very expensive, and eventually it was abandoned in light of an alternative solution: modifying CMOS electronics.

There was already a large-scale, commercial production of CMOS electronics, so the most simple and inexpensive solution was to buy chips from industry and then make modifications to make them radiation hard. Although CERN were using commercial technologies and collaborating with the companies that produced them, no change was made to the chips, so there was no common R&D. Most of the CMOS technology was made by IBM and TSMC [3].

3 Advances in pixel detectors for the HL-LHC

The upgrade to the high luminosity LHC (HL-LHC) is due for completion in the mid 2020s. This should see luminosities of up to 5 x 10^{35} cm^{-2} sec^{-1} with 50 ns bunch crossing and exposure of up to 500 Mrad in the inner parts of the pixel detectors [4]. As such, it is important that the microelectronics used in the readout of the pixel detectors are very radiation hard, are as thin as possible, and have very fast and efficient charge collection in order to maintain the high performance of such detectors.

There are two possible routes to increase circuit density and achieve suitable readout electronics: 3D integration or a planar readout integrated circuits (ROICs) using the 65 nm CMOS process.

3.1 3D Integration

Exposure to large doses of radiation results in defects in the silicon bulk of detectors, which reduces the overall sensor performance as the charge collection efficiency is significantly degraded. However, 3D sensors can tolerate radiation damage much better than planar detectors. The main advantage of using 3D silicon chips for circuit integration is the reduction in power consumption due to the smaller connections and

smaller involved capacitances. 3D chips are made by stacking silicon wafers that can be connected by through silicon vias (TSVs), interposers or solid liquid inter-diffusion (SLID). In pixel detectors, TSVs are usually used as they allow better connectivity between detector modules.

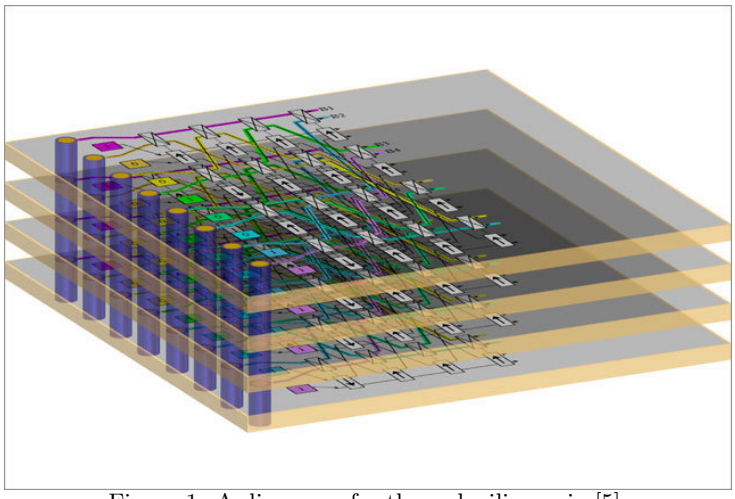

Figure 1: A diagram of a through-silicon via [5].

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The attempts at 3D circuit integration were first carried out by HEP groups at Fermilab in 2006 [6]. However, there problems with radiation hardness and processing, and the chips took over a year to manufacture. The solution was to look to commercial companies to develop the 3D sensors. In the end, the process used for these 3D chips was the Tezzaron/Chartered process in 130 nm feature size [7].

Tezzaron Semiconductor was a leader in 3D technology development and had many commercial customers using their technologies. Chartered Semiconductor (now GlobalFoundries) had a small feature process of 130 nm, which was the same as the CERN 130 nm CMOS process but was low cost. Chartered signed an agreement with Tezzaron to develop 3D technologies for HEP [6].

In 2008, a HEP 3D consortium was formed to submit a project to Chartered/Tezzaron. The initial work was completed in 2009 but there were issues with wafer order, design, submission and processing. The process was also slowed down as it was during this time that Chartered changed its name to GlobalFoundries [6].

The 3D sensors were tested and found to be suitably radiation hard and produced good results. But it was found that in HEP, just as in industry, it is more effective to reduce the feature size than use 3D technology to achieve high density circuits [8]. Research into 3D integration with TSVs is currently being carried out by the RD50 group at CERN.

3.2 Planar 65 nm CMOS

The alternative 3D sensors is to develop planar sensors. Thus far there have been three generations of planar pixel chips that have been developed, and the third generation, which involve the 65 nm CMOS process, are currently under development.

The 65 nm CMOS process is well established in industry, so CERN are able to buy the chips from industry and use their own techniques to make them radiation hard, as was done previously with the CMOS technology used in the LHC. The RD53 collaboration is looking at this radiation hardening process [7].

The 65 nm process is currently used as it works well and comes at an affordable price. There are other advantages to 3D sensors, especially in terms of radiation hardness, but at the moment, they are not needed [7]. However, if suitable 3D technologies were available now at an affordable price, they would certainly replace the 65 nm planar sensors due to their power efficiency.

4 Commercial needs for 3D circuit integration

Industry is very interested in 3D integration as it can be used for memory in complex computing systems. 3D technology offers high bandwidth, low power, high performance, and miniaturisation. It is for this reason that it is highly desired by semiconductor manufacturing companies such as IBM and Intel.

Dynamic random access memory (DRAM) is an area which has seen some of the fastest growth of 3D integration in recent years [8]. By stacking DRAM on top of processors, transfer speed can be increased.

For a number of years, IBM have been developing their own 3D integration using TSVs. IBM's research into 3D microelectronics began in the 1960s, but it wasn't until the 2000s that IBM started developing TSVs [9]. The first manufactured products using TSVs were announced by IBM in 2008. IBM has also investigated interconnection density for silicon layers and the research into 3D silicon integration using TSVs continues to be studied at present [9].

5 Conclusion

Historically, CERN has conducted R&D for fast timing, radiation hard electronics, which are vital to the LHC and HL-LHC. Industry has taken similar approaches to solving similar R&D needs, and have been working on them for some time now with moderate success. From this we can see that there is the opportunity for a collaborative effort to have been put in place. In order to establish such a case, a long-standing relationship with industry is needed together with an earlier engagement on technical requirements.

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