RCE readout interface for RD53A

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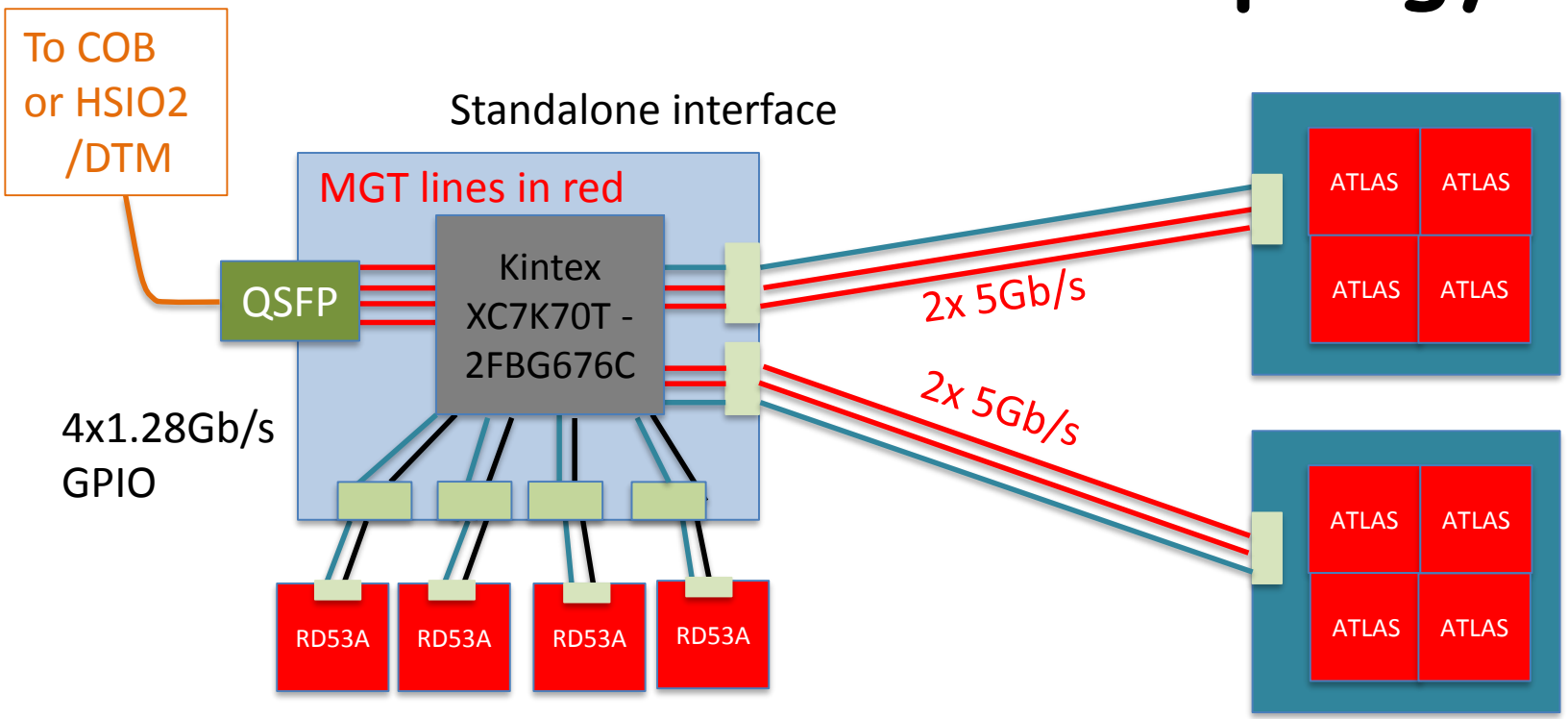
RD53 Readout Interface Requirements

- RD53A data link is 4x1.28 Gb/s (1.25 or even lower on emulator) bonded lane with 64b/66b
- Eventual ATLAS chip data link will be 5 Gb/s
- All flavors of modules in two categories:
  - A: 1xCMD + 1xData: single chip, outer Quad, outer Dual
  - B: 1xCMD + 2xData: inner Dual, high rate inner Quad

  RD53A stage only needs to deal with Type A ?
- Each module test carrier has two DisplayPorts
  - DP1 (RD53A): CMD^{+-},RST(?),$GTX[0:4]^{+-}$,NTC1,NTC2
    (ATLAS): CMD^{+-},RST(?),$GTX[0:1]^{+-}$,NTC1,NTC2
  - DP2: AUX^{+-}, $HitOR[0:3]^{+-}$

Can one interface hardware handle all cases ?

Possible Interface Topology



4 RD53A module DisplayPorts

Additional external clock/trigger not drawn

Is there a clever way to switch to 4 modules of single 5 Gb/s each ?

Single Interface Features

- Selection of DP for different module types
  - 4x RD53A modules using GPIO lines
  - 2x (maybe 4) ATLAS modules using MGT lines
- Interim emulator tests still need passive FMC-DP adaptor
- Generic QSFP output fiber link (any distance) to COB/HSIO2 or other readout
- Additional I/O connections for CMD/clock, trigger
- XC7K70T ~$130 – less than PCB
- Can load XC7K160T FPGA for the same 2FBG676C package if more FPGA resources desired